

SN95176B DIFFERENTIAL BUS TRANSCEIVER

SGLS026A – MARCH 1989 – REVISED JUNE 1995

- Bidirectional Transceiver
- Suitable for Most EIA Standards RS-422-A and RS-485 Applications
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Sensitivity . . . ± 200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements

description

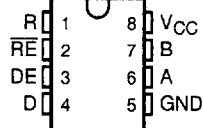
The SN95176B differential bus transceiver is a monolithic integrated circuit designed for bi-directional data communication on multipoint bus transmission lines. The transceiver is suitable for most RS-422-A and RS-485 applications to the extent of the specified data sheet characteristics and operating conditions.

The SN95176B combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC} = 0$. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

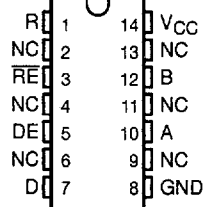
The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k Ω , an input sensitivity of ± 200 mV, and a typical input hysteresis of 50 mV.

The SN95176B is characterized for operation from -40°C to 110°C .

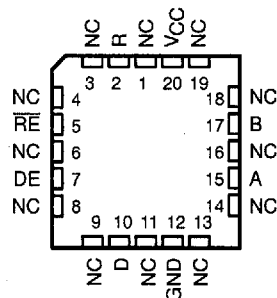
JG PACKAGE
(TOP VIEW)



W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

PRODUCTION DATA Information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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SN95176B

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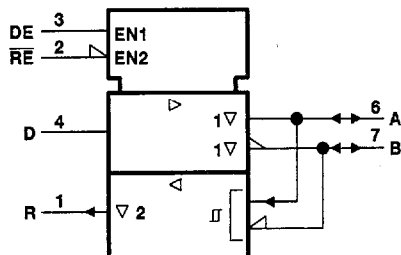
SGLS026A - MARCH 1989 - REVISED JUNE 1995

Function Tables

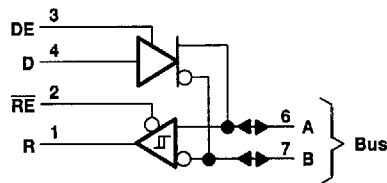
DRIVER				RECEIVER		
INPUT D	ENABLE DE	OUTPUTS		DIFFERENTIAL INPUTS A - B	ENABLE RE	OUTPUT R
		A	B			
H	H	H	L	$V_{ID} \geq 0.2 V$	L	H
L	H	L	H	$-0.2 V < V_{ID} < 0.2 V$	L	?
X	L	Z	Z	$V_{ID} \leq -0.2 V$	L	L
				X	H	Z

H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

logic symbol†

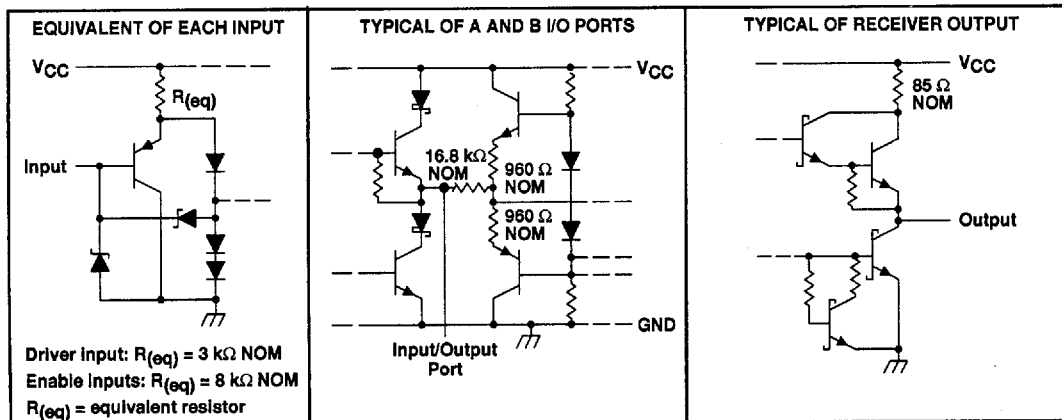


logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the JG package.

schematics of inputs and outputs



8961724 0098794 301

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SN95176B DIFFERENTIAL BUS TRANSCEIVER

SGLS026A – MARCH 1989 – REVISED JUNE 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	7 V
Voltage at any bus terminal	–10 V to 15 V
Enable input voltage, V_I	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 110°C
Storage temperature range, T_{stg}	–65°C to 150°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG or W package	300°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 110^\circ\text{C}$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	336 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	320 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IO}			12		V
			–7		
High-level input voltage, V_{IH}	D, DE, and \overline{RE}	2			V
Low-level input voltage, V_{IL}	D, DE, and \overline{RE}		0.8		V
Differential input voltage, V_{ID} (see Note 2)			±12		V
High-level output current, I_{OH}	Driver		–60		mA
	Receiver		–400		µA
Low-level output current, I_{OL}	Driver		60		mA
	Receiver		8		
Operating free-air temperature, T_A		–40		110	°C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

8961724 0098795 248



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

2–581

SN95176B

DIFFERENTIAL BUS TRANSCEIVER

SGLS026A – MARCH 1989 – REVISED JUNE 1995

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_O Output voltage	$I_O = 0$	0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$	1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$, See Figure 1	2			V
	$R_L = 54 \Omega$, See Figure 1	1.5	2.5	5	V
V_{OD3} Differential output voltage	See Note 3		4		V
$\Delta V_{OD} $ Change in magnitude of differential output voltage§	$R_L = 54 \Omega$, See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage				3	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage§				± 0.2	V
I_O Output current	Output disabled, See Note 4	$V_O = 12 \text{ V}$		1	mA
		$V_O = -7 \text{ V}$		-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$			-400	μA
I_{OS} Short-circuit output current	$V_O = -7 \text{ V}$			-250	mA
	$V_O = 0$			-150	
	$V_O = V_{CC}$			250	
	$V_O = 12 \text{ V}$			250	
I_{CC} Supply current (total package)	No load	Outputs enabled	42	70	mA
		Outputs disabled	26	35	

† The power-off measurement in EIA Standard RS-422-A applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, Test Termination Measurement 2.

4. This applies for both power on and off; refer to EIA Standard RS-485 for exact conditions. The RS-422-A limit does not apply for a combined driver and receiver terminal.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$R_L = 54 \Omega$, See Figure 3		15	22	ns
$t_{t(OD)}$ Differential output transition time			20	30	
t_{PZH} Output enable time to high level	$R_L = 110 \Omega$, See Figure 4		85	120	ns
t_{PZL} Output enable time to low level	$R_L = 110 \Omega$, See Figure 5		40	60	ns
t_{PHZ} Output disable time from high level	$R_L = 110 \Omega$, See Figure 4		150	250	ns
t_{PLZ} Output disable time from low level	$R_L = 110 \Omega$, See Figure 5		20	30	ns

8961724 0098796 184



SYMBOL EQUIVALENTS

DATA SHEET PARAMETER	RS-422-A	RS-485
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_O	V_O
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	V_t (Test Termination Measurement 2)
$\Delta V_{OD} $	$ V_t - \bar{V}_t $	$ V_t - \bar{V}_t $
V_{OC}	$ V_{Os} $	$ V_{Os} $
$\Delta V_{OC} $	$ V_{Os} - \bar{V}_{Os} $	$ V_{Os} - \bar{V}_{Os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7 \text{ V}$, $I_O = -0.4 \text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5 \text{ V}$, $I_O = 8 \text{ mA}$	-0.2‡			V
V_{hys} Input hysteresis voltage ($V_{IT+} - V_{IT-}$)			50		mV
V_{IK} Enable clamp voltage	$I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200 \text{ mV}$, See Figure 2		2.7		V
V_{OL} Low-level output voltage	$V_{ID} = -200 \text{ mV}$, See Figure 2			0.45	V
I_{OZ} High-impedance-state output current	$V_O = 0.4 \text{ V to } 2.4 \text{ V}$			±20	µA
I_I Line input current	Other input = 0 V, See Note 5	$V_I = 12 \text{ V}$		1	mA
		$V_I = -7 \text{ V}$		-0.8	
I_{IH} High-level enable input current	$V_{IH} = 2.7 \text{ V}$			20	µA
I_{IL} Low-level enable input current	$V_{IL} = 0.4 \text{ V}$			-100	µA
r_i Input resistance	$V_I = 12 \text{ V}$		12		kΩ
I_{OS} Short-circuit output current			-15	-85	mA
I_{CC} Supply current (total package)	No load	Outputs enabled	42	70	mA
		Outputs disabled	26	35	

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for both power on and power off. Refer to EIA Standard RS-485 for exact conditions.

SN95176B

DIFFERENTIAL BUS TRANSCEIVER

SGLS026A – MARCH 1989 – REVISED JUNE 1995

switching characteristics, $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low- to high-level output	$V_{ID} = 0\text{ to }3\text{ V}$, See Figure 6		21	35	ns
t_{PHL} Propagation delay time, high- to low-level output			23	35	ns
t_{PZH} Output enable time to high level	See Figure 7		10	20	ns
t_{PZL} Output enable time to low level			12	20	ns
t_{PHZ} Output disable time from high level	See Figure 7		20	35	ns
t_{PLZ} Output disable time from low level			17	25	ns

PARAMETER MEASUREMENT INFORMATION

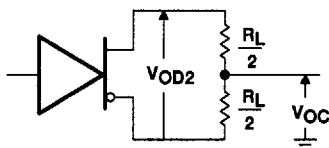


Figure 1. Driver V_{OD} and V_{OC}

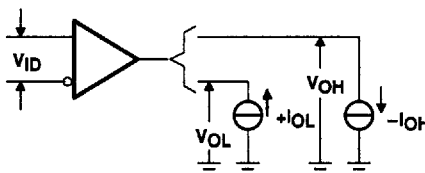
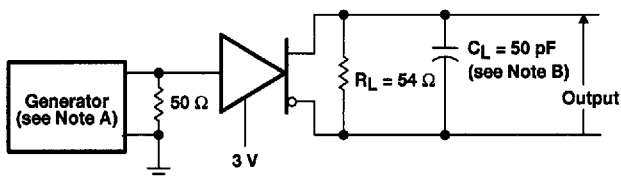


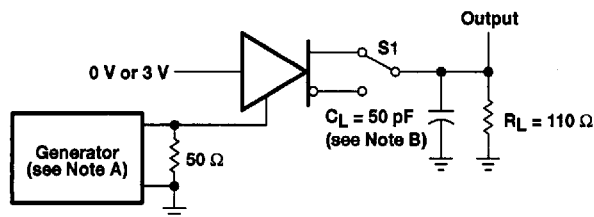
Figure 2. Receiver V_{OH} and V_{OL}



TEST CIRCUIT

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_0 = 50\text{ }\Omega$.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT

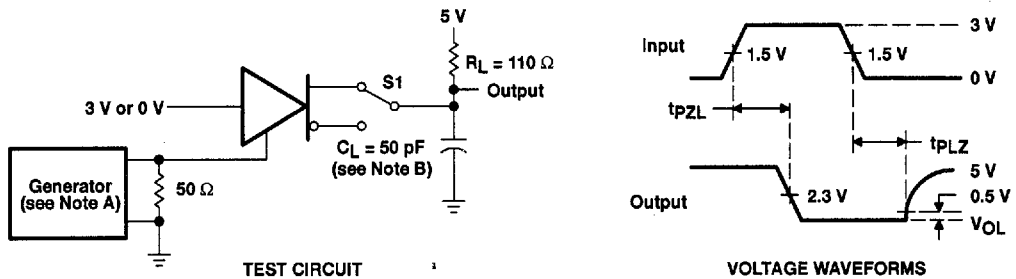
NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1\text{ MHz}$, 50% duty cycle, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$, $Z_0 = 50\text{ }\Omega$.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

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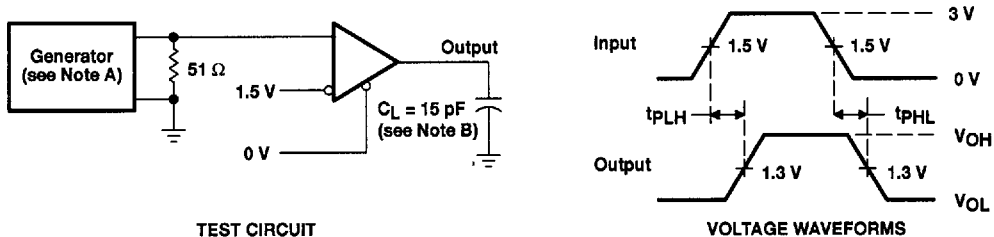
TEXAS
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PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms



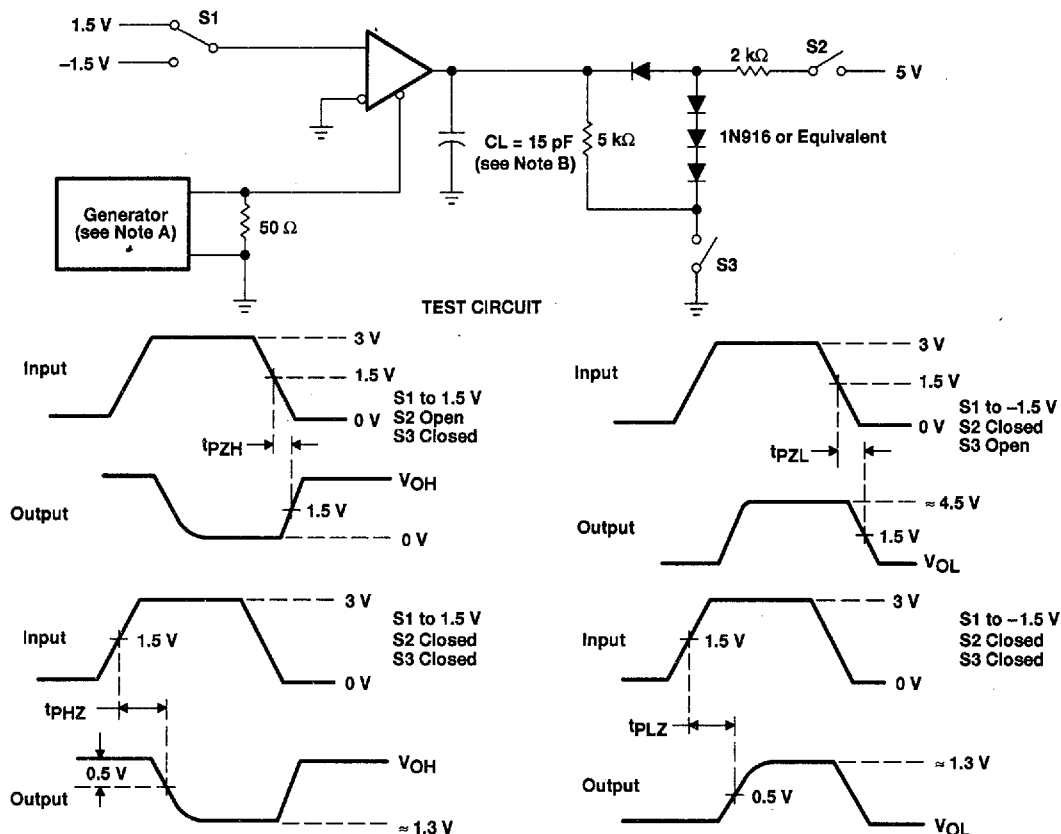
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Test Circuit and Voltage Waveforms

SN95176B DIFFERENTIAL BUS TRANSCEIVER

SGLS026A – MARCH 1989 – REVISED JUNE 1995

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

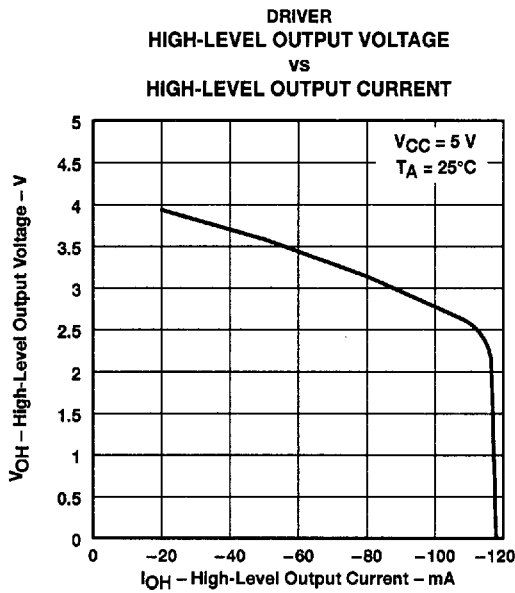


Figure 8

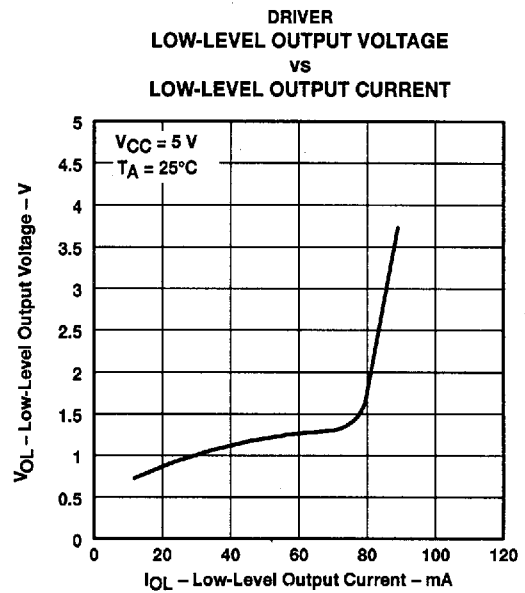


Figure 9

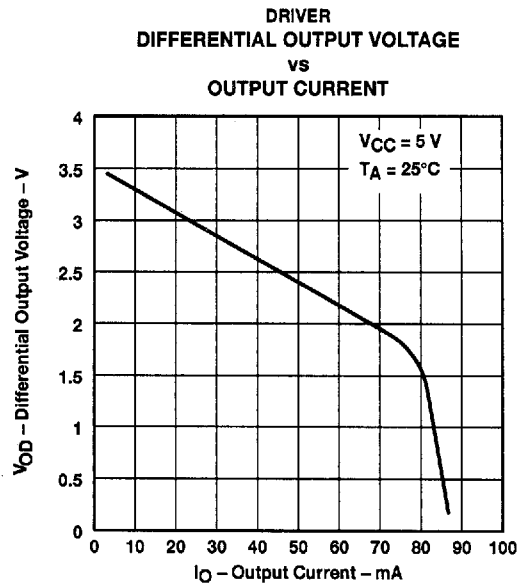


Figure 10

SN95176B DIFFERENTIAL BUS TRANSCEIVER

SGLS026A - MARCH 1989 - REVISED JUNE 1995

TYPICAL CHARACTERISTICS

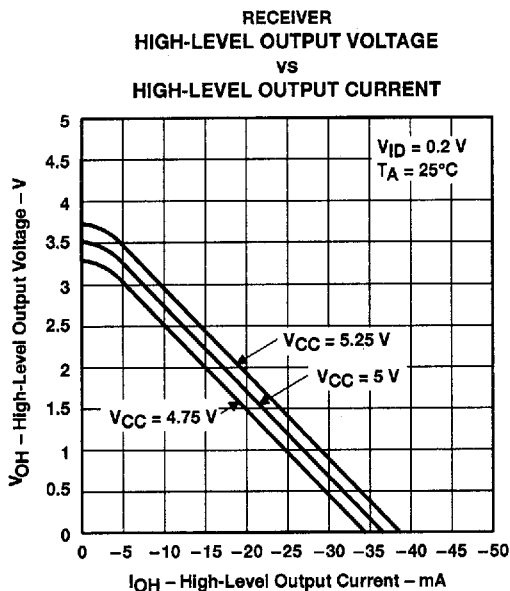


Figure 11

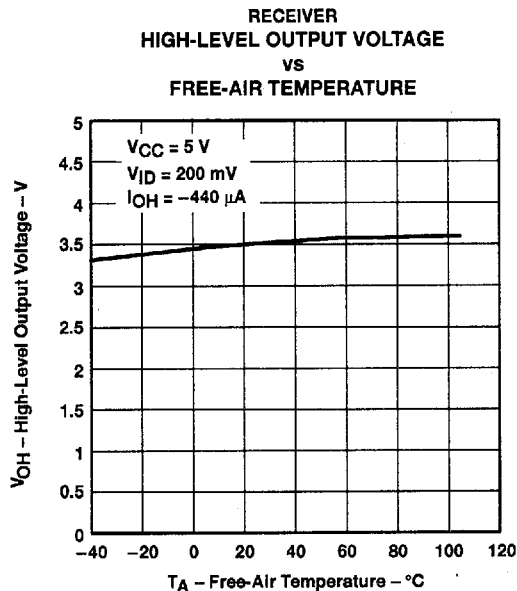


Figure 12

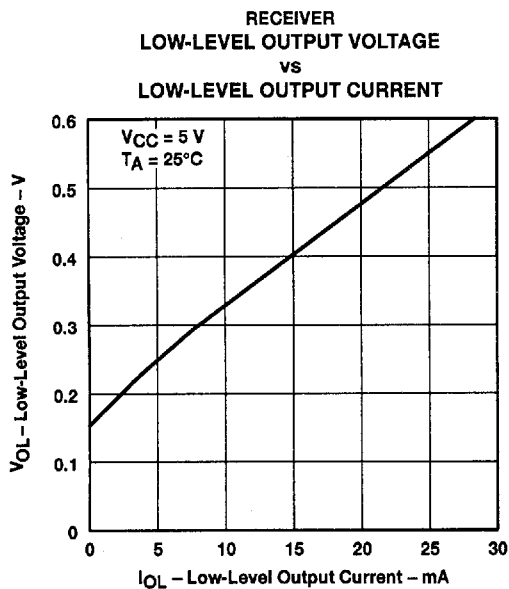


Figure 13

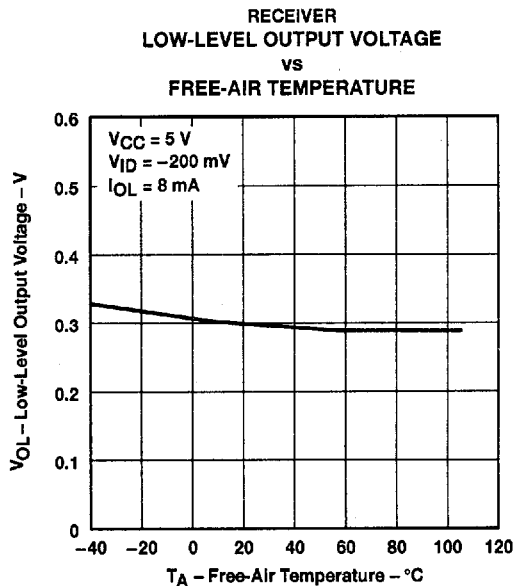


Figure 14

TYPICAL CHARACTERISTICS

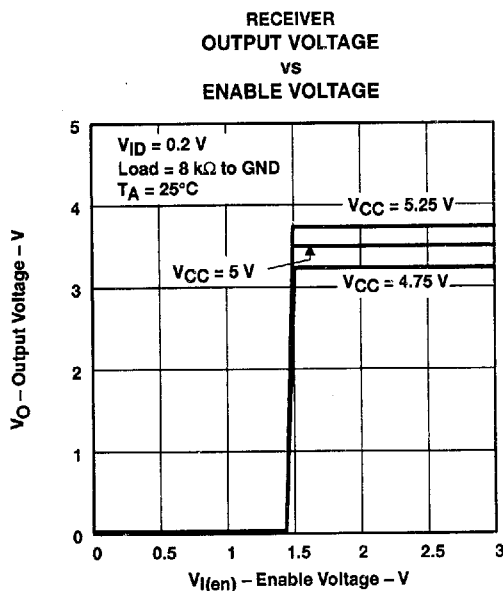


Figure 15

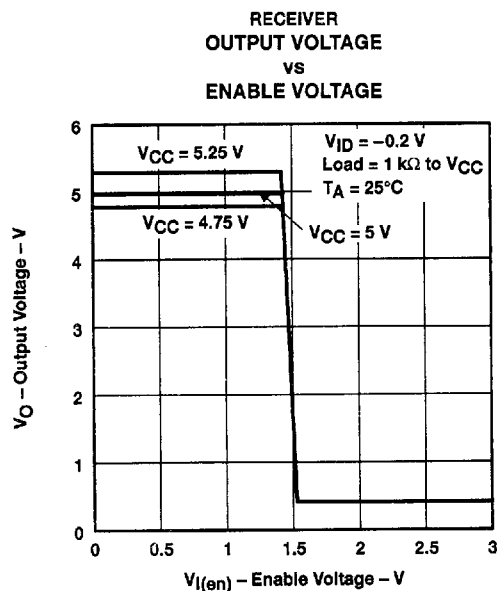


Figure 16

APPLICATION INFORMATION

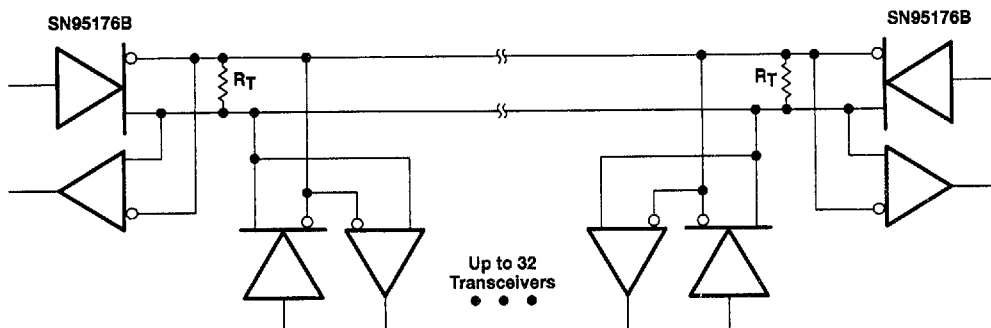


Figure 17. Typical Application Circuit

NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.