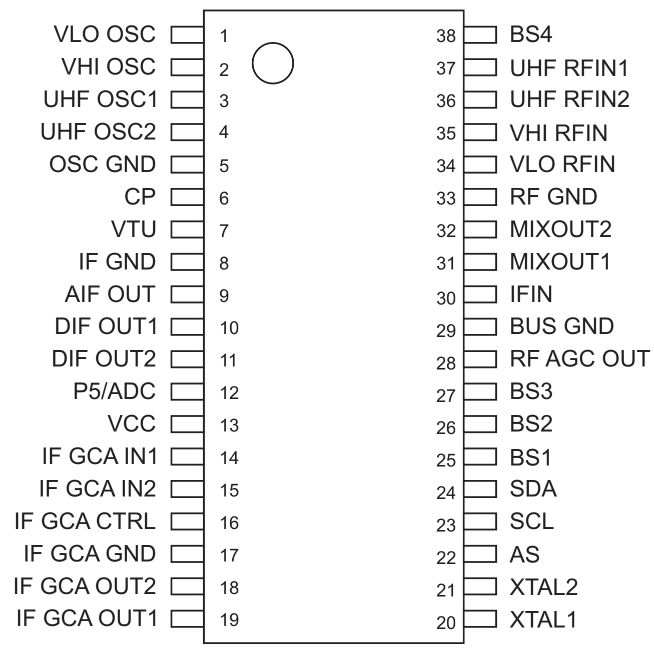
DIGITAL TV TUNER IC

Check for Samples: SN761645

FEATURES

- **Integrated Mixer/Oscillator/PLL and IF GCA**
- **VHF-L, VHF-H, UHF 3-Band Local Oscillator**
- **RF AGC Detector Circuit**
- **I2C Bus Protocol**
- **Seven-Step Charge Pump Current**
- **Four NPN Emitter-Follower Type Band Switch Drivers**
- **One Auxiliary Port/5-Level ADC**
- **Programmable Reference Divider Ratio**
- **Crystal Oscillator 4-MHz/16-MHz Support**
- **Selectable Digital IFOUT and Analog IFOUT**
- **Standby Mode**
- **5-V Power Supply**
- **38-Pin TSSOP Package**

DBT PACKAGE
(TOP VIEW)



APPLICATIONS

- **Digital TV**
- **Digital CATV**
- **Set-Top Box**

DESCRIPTION

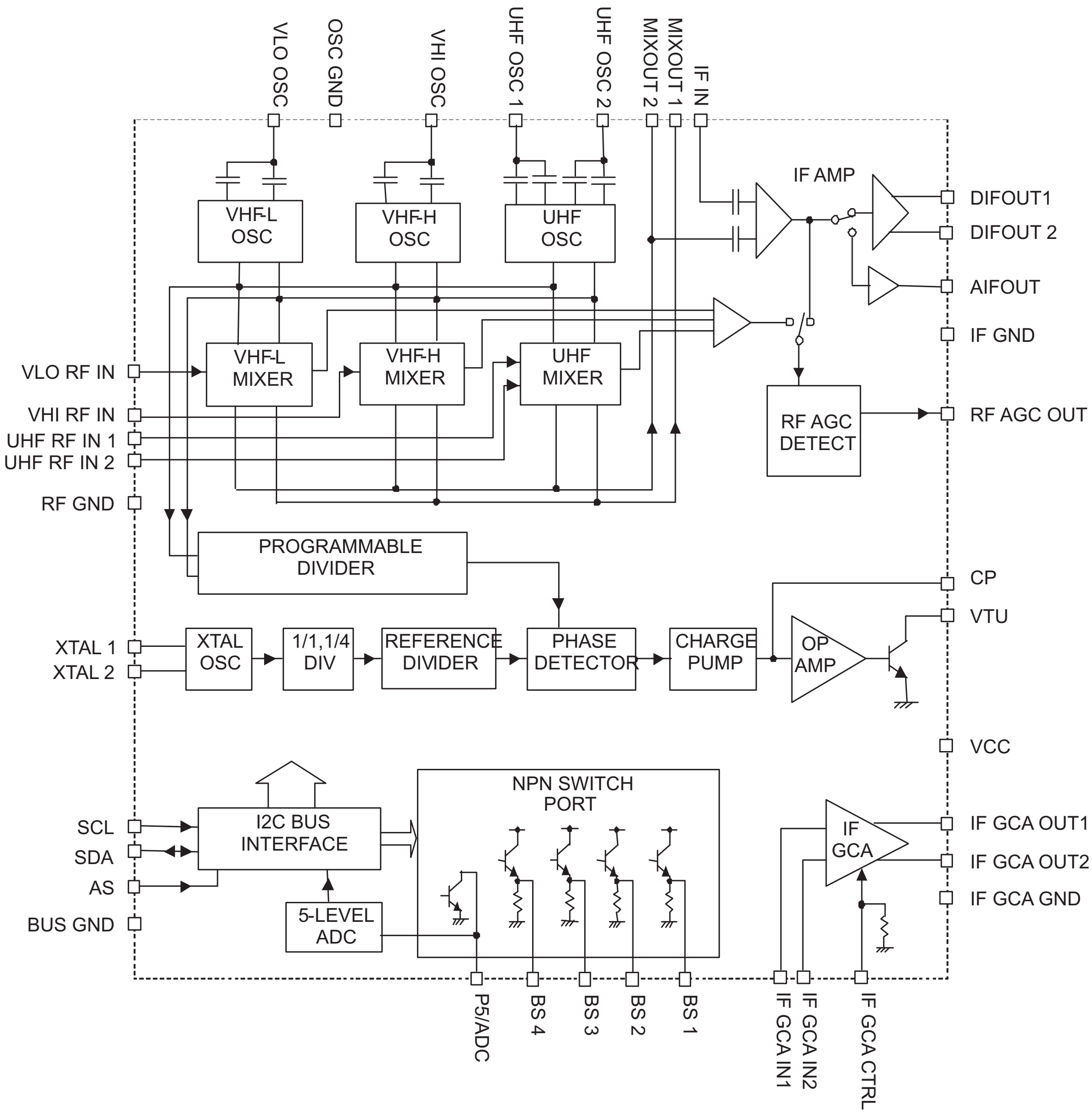
The SN761645 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, RF AGC detector circuit, and IF gain controlled amplifier, and is available in a small outline package.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	SCHEMATIC
NAME	NO.		
AIF OUT	9	IF amplifier output (unbalanced)	Figure 1
AS	22	Address selection input (open or connection to GND)	Figure 2
BS1	25	Band-switch 1 output (emitter follower)	Figure 3
BS2	26	Band-switch 2 output (emitter follower)	Figure 3
BS3	27	Band-switch 3 output (emitter follower)	Figure 3
BS4	38	Band-switch 4 output (emitter follower)	Figure 3
BUS GND	29	BUS ground	
CP	6	Charge pump output	Figure 4
DIF OUT1	10	IF amplifier balance output 1	Figure 5
DIF OUT2	11	IF amplifier balance output 2	Figure 5
IF GCA CTRL	16	IF GCA control voltage input	Figure 6
IF GCA GND	17	IF GCA ground	
IF GCA IN1	14	IF GCA input 1	Figure 7
IF GCA IN2	15	IF GCA input 2	Figure 7
IF GCA OUT1	19	IF GCA output 1	Figure 8
IF GCA OUT2	18	IF GCA output 2	Figure 8
IF GND	8	IF ground	
IF IN	30	IF amplifier input	Figure 9
MIX OUT1	31	Mixer output 1	Figure 10
MIX OUT2	32	Mixer output 2	Figure 10
OSC GND	5	Oscillator ground	
P5/ADC	12	Port-5 output/ADC input	Figure 11
RF AGC OUT	28	RF AGC output	Figure 12
RF GND	33	RF ground	
SCL	23	Serial clock input	Figure 13
SDA	24	Serial data input/output	Figure 14
UHF OSC1	3	UHF oscillator 1	Figure 15
UHF OSC2	4	UHF oscillator 2	Figure 15
UHF RF IN1	37	UHF RF input 1	Figure 16
UHF RF IN2	36	UHF RF input 2	Figure 16
VCC	13	Supply voltage	
VHI OSC	2	VHF HIGH oscillator	Figure 17
VHI RF IN	35	VHF HIGH RF input	Figure 18
VLO OSC	1	VHF LOW oscillator	Figure 19
VLO RF IN	34	VHF LOW RF input	Figure 20
VTU	7	Tuning voltage amplifier output	Figure 21
XTAL1	20	Crystal oscillator	Figure 22
XTAL2	21	Crystal oscillator	Figure 22

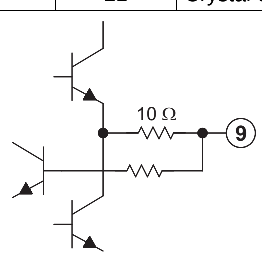


Figure 1. AIF OUT

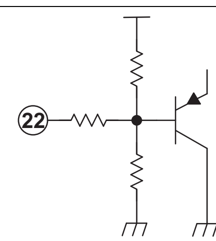


Figure 2. AS

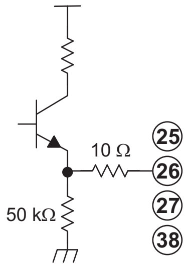


Figure 3. BS1, BS2, BS3, BS4

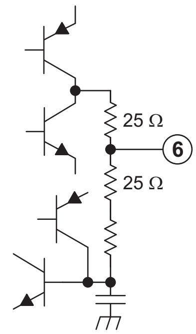


Figure 4. CP

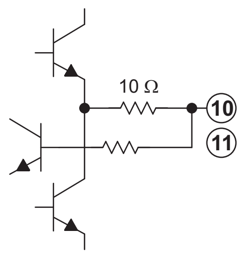


Figure 5. DIF OUT1, DIF OUT2

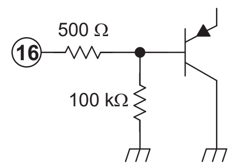


Figure 6. IF GCA CTRL

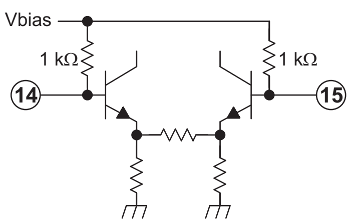


Figure 7. IF GCA IN1, IF GCA IN2

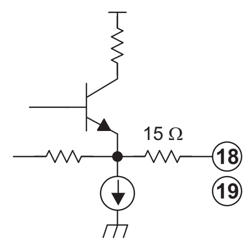


Figure 8. IF GCA OUT1, IF GCA OUT2

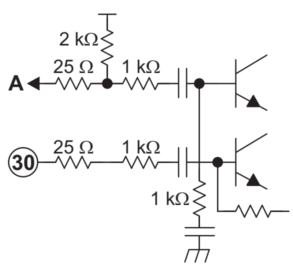


Figure 9. IF IN

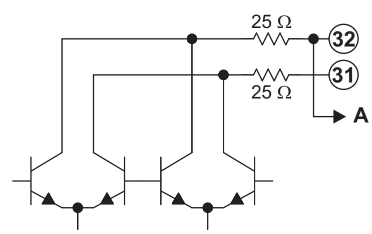


Figure 10. MIXOUT1, MIXOUT2

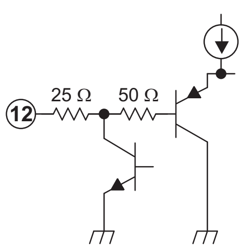


Figure 11. P5/ADC

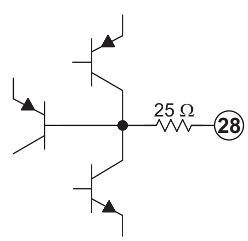


Figure 12. RF AGC OUT

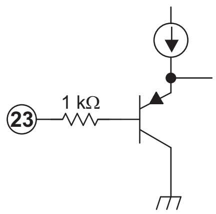


Figure 13. SCL

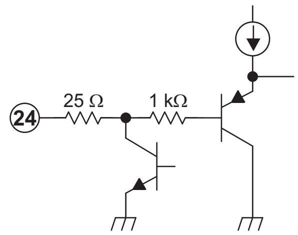


Figure 14. SDA

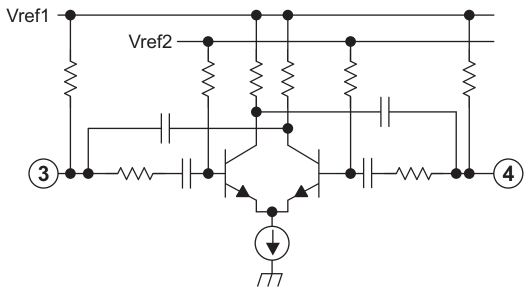


Figure 15. UHF OSC 1, UHF OSC 2

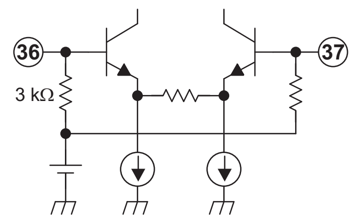


Figure 16. UHF RF IN1, UHF RF IN2

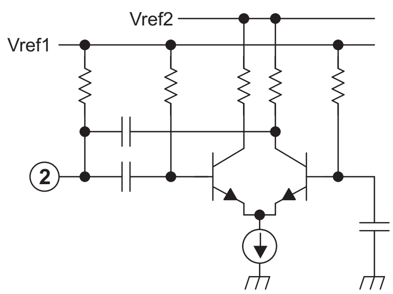


Figure 17. VHI OSC

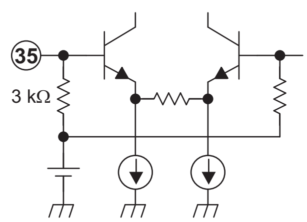


Figure 18. VHI RF IN

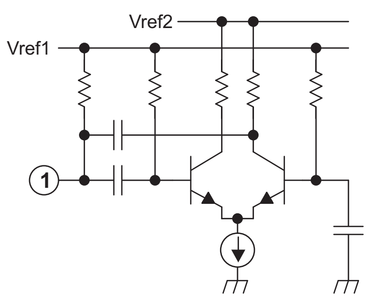


Figure 19. VLO OSC

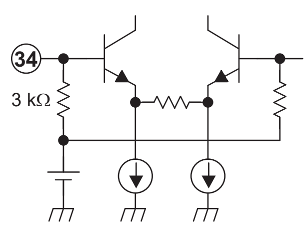


Figure 20. VLO RF IN

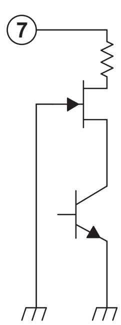


Figure 21. VTU

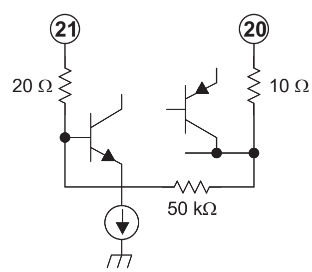


Figure 22. XTAL1, XTAL2

ABSOLUTE MAXIMUM RATINGS(1)

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range (2)	V_{CC}	–0.4	6.5	V
V_{GND}	Input voltage range 1 (2)	RF GND, OSC GND, BUS GND	–0.4	0.4	V
VTU	Input voltage range 2 (2)	VTU	–0.4	35	V
V_{IN}	Input voltage range 3 (2)	Other pins	–0.4	6.5	V
P_D	Continuous total dissipation (3)	$T_A \leq 25°C$		1277	mW
T_A	Operating free-air temperature range		–20	85	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Maximum junction temperature			150	°C
$t_{SC(max)}$	Maximum short-circuit time	Each pin to V_{CC} or to GND		10	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 10.2 mW/°C for T_A > 25°C.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}	4.5	5	5.3	V
VTU	Tuning supply voltage	VTU		30	33	V
I_{BS}	Output current of band switch	BS1 to BS4, one band switch on			10	mA
I_{P5}	Output current of port 5	P5			–5	mA
T_A	Operating free-air temperature		–20		85	°C

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

IF IN1, MIX OUT 1, and MIX OUT 2 (pins 30, 31, and 32, respectively) withstand 1.5 kV, and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

ELECTRICAL CHARACTERISTICS

Total Device and Serial Interface

V_{CC} = 4.5 V to 5.3 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}1$	Supply current 1	BS[1:4] = 0100, IFGCA disabled		90		mA
$I_{CC}2$	Supply current 2	BS[1:4] = 0100, IFGCA enabled		110		mA
$I_{CC-STBY}$	Standby supply current	BS[1:4] = 1100		9		mA
V_{IH}	High-level input voltage (SCL, SDA)		2.3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.05	V
I_{IH}	High-level input current (SCL, SDA)				10	µA
I_{IL}	Low-level input current (SCL, SDA)		–10			µA
V_{POR}	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
I²C Interface						
V_{ADC}	ADC input voltage	See Table 11	0		V_{CC}	V
I_{ADH}	ADC high-level input current	$V_{ADC} = V_{CC}$			10	µA
I_{ADL}	ADC low-level input current	V_{ADC} = 0 V	–10			µA
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High-level output leakage current (SDA)	V_{SDA} = 5.3 V			10	µA
f_{SCL}	Clock frequency (SCL)			100	400	kHz
t_{HD-DAT}	Data hold time	See Figure 23	0		3.45	µs
t_{BUF}	Bus free time		1.3			µs
t_{HD-STA}	Start hold time		0.6			µs
t_{LOW}	SCL-low hold time		1.3			µs
t_{HIGH}	SCL-high hold time		0.6			µs
t_{SU-STA}	Start setup time		0.6			µs
t_{SU-DAT}	Data setup time		0.1			µs
t_r	Rise time (SCL, SDA)				1	µs
t_f	Fall time (SCL, SDA)				0.3	µs
t_{SU-STO}	Stop setup time		0.6			µs

PLL and Band Switch

V_{CC} = 4.5 V to 5.3 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
f_{XTAL}	Crystal oscillator frequency	R_{XTAL} = 25 Ω to 300 Ω		4	16	MHz
Z_{XTAL}	Crystal oscillator input impedance	4-MHz crystal, V_{CC} = 5 V, T_A = 25°C		2		kΩ
V_{VTUL}	Tuning amplifier low-level output voltage	R_L = 20 kΩ, VTU = 33 V	0.2	0.45	0.6	V
I_{VTUOFF}	Tuning amplifier leakage current	Tuning amplifier = off, VTU = 33 V			10	µA
I_{CP000}	Charge-pump current	CP[2:0] = 000		35		µA
I_{CP001}		CP[2:0] = 001		70		
I_{CP010}		CP[2:0] = 010		140		
I_{CP011}		CP[2:0] = 011		210		
I_{CP100}		CP[2:0] = 100		280		
I_{CP101}		CP[2:0] = 101		350		
I_{CP110}		CP[2:0] = 110		420		
V_{CP}	Charge-pump output voltage	PLL locked		1.95		V
I_{CPOFF}	Charge-pump leakage current	V_{CP} = 2 V, T_A = 25°C	–15		15	nA
I_{BS}	Band switch driver output current (BS1–BS4)				10	mA
V_{BS1}	Band switch driver output voltage (BS1–BS4)	I_{BS} = 10 mA	2.9			V
V_{BS2}		I_{BS} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.4	3.6		
I_{BSOFF}	Band switch driver leakage current (BS1–BS4)	V_{BS} = 0 V			8	µA
I_{P5}	Band switch port sink current (P5/ADC)		–5			mA
V_{P5ON}	Band switch port output voltage (P5/ADC)	I_{P5} = –2 mA, V_{CC} = 5 V, T_A = 25°C			0.6	V

RF AGC(1)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 24 reference measurement circuit at 50-Ω system, IF = 36.15 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OAGC0}	RF AGC output source current	ATC = 0			300		nA
I_{OAGC1}		ATC = 1			9		µA
$I_{OAGCSINK}$	RF AGC peak sink current	ATC = 0			100		µA
V_{OAGCH}	RFAGCOUT output high voltage (max level)	ATC = 1		3.7	4.2	4.7	V
V_{OAGCL}	RFAGCOUT output low voltage (min level)	ATC = 1			0.3		V
$V_{AGCSP00}$	Start-point IF output level	AISL = 0	ATP[2:0] = 000		114		dBµV
$V_{AGCSP01}$			ATP[2:0] = 001		112		
$V_{AGCSP02}$			ATP[2:0] = 010		110		
$V_{AGCSP03}$			ATP[2:0] = 011		108		
$V_{AGCSP04}$			ATP[2:0] = 100		106		
$V_{AGCSP05}$			ATP[2:0] = 101		104		
$V_{AGCSP06}$			ATP[2:0] = 110		102		

(1) When AISL = 1, RF AGC function is not available at VHF-L band.

Mixer, Oscillator, IF Amplifier (DIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 24 reference measurement circuit at 50-Ω system, IF = 36.15 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GC_{1D}	Conversion gain (mixer - IF amplifier), VHF-LOW	f_{IN} = 50.85 MHz (1)		35		dB
GC_{3D}		f_{IN} = 149.85 MHz (1)		35		dB
GC_{4D}	Conversion gain (mixer - IF amplifier), VHF-HIGH	f_{IN} = 156.85 MHz (1)		35		dB
GC_{6D}		f_{IN} = 425.85 MHz (1)		35		dB
GC_{7D}	Conversion gain (mixer - IF amplifier), UHF	f_{IN} = 433.85 MHz (1)		35		dB
GC_{9D}		f_{IN} = 857.85 MHz (1)		35		dB
NF_{1D}	Noise figure, VHF-LOW	f_{IN} = 50.85 MHz		9		dB
NF_{3D}		f_{IN} = 149.85 MHz		9		dB
NF_{4D}	Noise figure, VHF-HIGH	f_{IN} = 156.85 MHz		9		dB
NF_{6D}		f_{IN} = 425.85 MHz		10		dB
NF_{7D}	Noise figure, UHF	f_{IN} = 433.85 MHz		10		dB
NF_{9D}		f_{IN} = 857.85 MHz		11		dB
CM_{1D}	Input voltage causing 1% cross modulation distortion, VHF-LOW	f_{IN} = 50.85 MHz (2)		92		dBµV
CM_{3D}		f_{IN} = 149.85 MHz (2)		92		dBµV
CM_{4D}	Input voltage causing 1% cross modulation distortion, VHF-HIGH	f_{IN} = 156.85 MHz (2)		92		dBµV
CM_{6D}		f_{IN} = 425.85 MHz (2)		92		dBµV
CM_{7D}	Input voltage causing 1% cross modulation distortion, UHF	f_{IN} = 433.85 MHz (2)		92		dBµV
CM_{9D}		f_{IN} = 857.85 MHz (2)		92		dBµV
V_{IFO1D}	IF output voltage, VHF-LOW	f_{IN} = 50.85 MHz		117		dBµV
V_{IFO3D}		f_{IN} = 149.85 MHz		117		dBµV
V_{IFO4D}	IF output voltage, VHF-HIGH	f_{IN} = 156.85 MHz		117		dBµV
V_{IFO6D}		f_{IN} = 425.85 MHz		117		dBµV
V_{IFO7D}	IF output voltage, UHF	f_{IN} = 433.85 MHz		117		dBµV
V_{IFO9D}		f_{IN} = 857.85 MHz		117		dBµV
Φ_{PLVL1D}	Phase noise, VHF-LOW	f_{IN} = 50.85 MHz (3)		-92		dBc/Hz
Φ_{PLVL3D}		f_{IN} = 149.85 MHz (4)		-91		dBc/Hz
Φ_{PLVL4D}	Phase noise, VHF-HIGH	f_{IN} = 156.85 MHz (3)		-86		dBc/Hz
Φ_{PLVL6D}		f_{IN} = 425.85 MHz (4)		-83		dBc/Hz
Φ_{PLVL7D}	Phase noise, UHF	f_{IN} = 433.85 MHz (3)		-79		dBc/Hz
Φ_{PLVL9D}		f_{IN} = 857.85 MHz (4)		-77		dBc/Hz

(1) RF input level = 70 dBµV, differential output
(2) f_{undes} = f_{des} ± 7 MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 1 kHz, CP current = 70 µA, reference divider = 24
(4) Offset = 1 kHz, CP current = 420 µA, reference divider = 24

Mixer, Oscillator, IF Amplifier (AIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 24 reference measurement circuit at 50-Ω system, IF = 36.15 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GC_{1A}	Conversion gain (mixer - IF amplifier), VHF-LOW	f_{IN} = 50.85 MHz (1)		29		dB
GC_{3A}		f_{IN} = 149.85 MHz (1)		29		dB
GC_{4A}	Conversion gain (mixer - IF amplifier), VHF-HIGH	f_{IN} = 156.85 MHz (1)		29		dB
GC_{6A}		f_{IN} = 425.85 MHz (1)		29		dB
GC_{7A}	Conversion gain (mixer - IF amplifier), UHF	f_{IN} = 433.85 MHz (1)		29		dB
GC_{9A}		f_{IN} = 857.85 MHz (1)		29		dB
NF_{1A}	Noise figure, VHF-LOW	f_{IN} = 50.85 MHz		9		dB
NF_{3A}		f_{IN} = 149.85 MHz		9		dB
NF_{4A}	Noise figure, VHF-HIGH	f_{IN} = 156.85 MHz		9		dB
NF_{6A}		f_{IN} = 425.85 MHz		10		dB
NF_{7A}	Noise figure, UHF	f_{IN} = 433.85 MHz		10		dB
NF_{9A}		f_{IN} = 857.85 MHz		11		dB
CM_{1A}	Input voltage causing 1% cross modulation distortion, VHF-LOW	f_{IN} = 50.85 MHz (2)		87		dBµV
CM_{3A}		f_{IN} = 149.85 MHz (2)		87		dBµV
CM_{4A}	Input voltage causing 1% cross modulation distortion, VHF-HIGH	f_{IN} = 156.85 MHz (2)		87		dBµV
CM_{6A}		f_{IN} = 425.85 MHz (2)		87		dBµV
CM_{7A}	Input voltage causing 1% cross modulation distortion, UHF	f_{IN} = 433.85 MHz (2)		87		dBµV
CM_{9A}		f_{IN} = 857.85 MHz (2)		87		dBµV
V_{IFO1A}	IF output voltage, VHF-LOW	f_{IN} = 50.85 MHz		117		dBµV
V_{IFO3A}		f_{IN} = 149.85 MHz		117		dBµV
V_{IFO4A}	IF output voltage, VHF-HIGH	f_{IN} = 156.85 MHz		117		dBµV
V_{IFO6A}		f_{IN} = 425.85 MHz		117		dBµV
V_{IFO7A}	IF output voltage, UHF	f_{IN} = 433.85 MHz		117		dBµV
V_{IFO9A}		f_{IN} = 857.85 MHz		117		dBµV
Φ_{PLVL1A}	Phase noise, VHF-LOW	f_{IN} = 50.85 MHz (3)		-92		dBc/Hz
Φ_{PLVL3A}		f_{IN} = 149.85 MHz (3)		-96		dBc/Hz
Φ_{PLVL4A}	Phase noise, VHF-HIGH	f_{IN} = 156.85 MHz (3)		-85		dBc/Hz
Φ_{PLVL6A}		f_{IN} = 425.85 MHz (3)		-88		dBc/Hz
Φ_{PLVL7A}	Phase noise, UHF	f_{IN} = 433.85 MHz (3)		-80		dBc/Hz
Φ_{PLVL9A}		f_{IN} = 857.85 MHz (3)		-85		dBc/Hz

(1) RF input level = 70 dBµV
(2) $f_{undes} = f_{des}$ ± 7 MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 10 kHz, CP current = 35 µA, reference divider = 64

IF Gain Controlled Amplifier

V_{CC} = 5 V, T_A = 25°C, measured in Figure 24 reference measurement circuit at 50-Ω system, IF = IF = 36.15 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IFGCA}	Input current (IF GCA CTRL)	V_{IFGCA} = 3 V		60	90	µA
$V_{IFGCAMAX}$	Maximum gain control voltage	Gain maximum	3		V_{CC}	V
$V_{IFGCAMIN}$	Minimum gain control voltage	Gain minimum	0		0.2	V
$G_{IFGCAMAX}$	Maximum gain	V_{IFGCA} = 3 V		67		dB
$G_{IFGCAMIN}$	Minimum gain	V_{IFGCA} = 0 V		3		dB
GCR_{IFGCA}	Gain control range	V_{IFGCA} = 0 V to 3 V		64		dB
$V_{IFGCAOUT}$	Output voltage	Single-ended output, V_{IFGCA} = 3 V		2.1		Vpp
NF_{IFGCA}	Noise figure	V_{IFGCA} = 3 V		11		dB
$IM3_{IFGCA}$	Third order intermodulation distortion	$f_{IFGCAIN1}$ = 35.65 MHz, $f_{IFGCAIIN2}$ = 36.65 MHz, $V_{IFGCAOUT}$ = –2 dBm, V_{IFGCA} = 3 V		–50		dBc
IIP_{3IFGCA}	Input intercept point	V_{IFGCA} = 0 V		11		dBm
$R_{IFGCAIN}$	Input resistance (IF GCA IN1, IF GCA IN2)			1		kΩ
$R_{IFGCAOUT}$	Output resistance (IF GCA OUT1, IF GCA OUT2)			25		Ω

FUNCTIONAL DESCRIPTION

I²C Bus Mode

I²C Write Mode (R/W = 0)

Table 1. Write Data Format

	MSB							LSB	
Address Byte (ADB)	1	1	0	0	0	0	MA	R/W = 0	A (1)
Divider Byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A (1)
Divider Byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A (1)
Control Byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A (1)
Band Switch Byte (BB)	CP1	CP0	AISL	P5	BS4	BS3	BS2	BS1	A (1)
Control Byte 2 (CB2)	1	1	ATC	MODE	DISGCA	IFDA	CP2	IXD4	A (1)

(1) A = acknowledge

Table 2. Write Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA	Address set bit MA = 0 : AS pin = 0 V (connection to GND) MA = 1 : AS pin = Open	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$	N14 = N13 = N12 = ... = N0 = 0
ATP[2:0]	RF AGC start-point control bits (see Table 3)	ATP[2:0] = 000
RS[2:0]	Reference divider ratio-selection bits (see Table 4)	RS[2:0] = 000
CP[2:0]	Charge-pump current set bits (see Table 5)	CP[2:0] = 000
P5	Port output / ADC input control bit P5 = 0 : ADC input P5 = 1 : Tr = ON	P5 = 0
BS[4:1]	Band-switch driver output control bits BSn = 0: Tr = OFF BSn = 1: Tr = ON	BS[4:1] = 0000
	Band selection and standby function control bits BS2 BS1 0 1 VHF-LO 1 0 VHF-HI 0 0 UHF 1 1 Standby mode / stop MOP function	
ATC	RFAGC output current-set bit ATC = 0: Source current = 300nA ATC = 1: Source current = 9uA	ATC = 0
MODE	Device mode selection bit MODE = 0 : Test mode MODE = 1 : Normal operation	MODE = 0
	Other control bits	
DISGCA	DISGCA IF GCA control bit (see Table 6)	DISGCA = 0
IFDA	IFDA AIF/DIF OUT selection bit (see Table 7)	IFDA = 0
AISL	AISL RFAGC detector input selection bit (see Table 8)	AISL = 0
IXD4	IXD4 Reference divider control bit (see Table 4)	IXD4 = 0

Table 3. RF AGC Start Point

MODE	ATP2	ATP1	ATP0	IFOUT LEVEL	
				(dBμV)	(mVp-p)
1	0	0	0	114	1417
1	0	0	1	112	1126
1	0	1	0	110	894
1	0	1	1	108	710
1	1	0	0	106	564
1	1	0	1	104	448
1	1	1	0	102	356
1	1	1	1	Disabled	

Table 4. Reference Divider Ratio

MODE	IXD4	RS2	RS1	RS0	REFERENCE DIVIDER RATIO
1	0	0	0	0	96
1	0	0	0	1	112
1	0	0	1	0	128
1	0	0	1	1	256
1	0	1	0	0	512
1	0	1	0	1	320
1	1	0	0	0	24
1	1	0	0	1	28
1	1	0	1	0	32
1	1	0	1	1	64
1	1	1	0	0	128
1	1	1	0	1	80
1	X	1	1	1	Forbidden

Table 5. Charge-Pump Current

MODE	CP2	CP1	CP0	CHARGE PUMP CURRENT (μA)
1	0	0	0	35
1	0	0	1	70
1	0	1	0	140
1	0	1	1	210
1	1	0	0	280
1	1	0	1	350
1	1	1	0	420
1	1	1	1	Forbidden

Table 6. IF GCA Control

MODE	DISGCA	IF GCA FUNCTION
1	0	IF GCA enabled
1	1	IF GCA disabled

Table 7. AIF / DIF OUT Selection

MODE	IFDA	IF OUT FUNCTION
1	0	DIF OUT 1,2 selected
1	1	AIF OUT selected

Table 8. RF AGC Detector Input Selection

MODE	AISL	RF AGC DETECTOR INPUT
1	0	IF amplifier selected
1	1 (1)	Mixer selected

(1) When AISL = 1, RF AGC function is not available at VHF-L band (output level is undefined).

I²C Read Mode (R/$\overline{W}$ = 1)

Table 9. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	0	MA	R/$\overline{W}$ = 1	A (1)
Status byte (SB)	POR	FL	1	1	1	A2	A1	A0	–

(1) A = acknowledge

Table 10. Read Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA	Address set bit MA = 0 : VLO OSC/AS pin = 0 V (connection to GND) MA = 1 : VLO OSC/AS pin = Open	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag (1) FL = 0 : PLL unlocked FL = 1 : PLL locked	
A[2:0]	Digital data of ADC (see Table 11) Bit P5 must be set to 0.	

(1) Lock detector works by using phase error pulse at the phase detector. Lock flag (FL) is set or reset according to this pulse-width discriminator. Hence, instability of the PLL may cause the lock detection circuit to malfunction. To stablize the PLL, it is required to evaluate application circuit in various condition of loop-gain (loop filter, CP current) and to verify under operation of the actual application.

Table 11. ADC Level (1)

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	0.6 V_{CC} to V_{CC}
0	1	1	0.45 V_{CC} to 0.6 V_{CC}
0	1	0	0.3 V_{CC} to 0.45 V_{CC}
0	0	1	0.15 V_{CC} to 0.3 V_{CC}
0	0	0	0 V to 0.15 V_{CC}

(1) Accuracy is 0.03 × V_{CC}.

Example I²C Data Write Sequences

Telegram examples:

Start - ADB - DB1 - DB2 - CB1 – BB - CB2 - Stop
Start - ADB - DB1 - DB2 - Stop
Start - ADB - CB1 - BB - CB2 - Stop
Start - ADB - CB1 - BB - Stop
Start - ADB - CB2 - Stop

Abbreviations:

ADB: Address byte
BB: Band switch byte
CB1: Control byte 1
CB2: Control byte 2
DB1: Divider byte 1
DB2: Divider byte 2
Start: Start condition
Stop: Stop condition

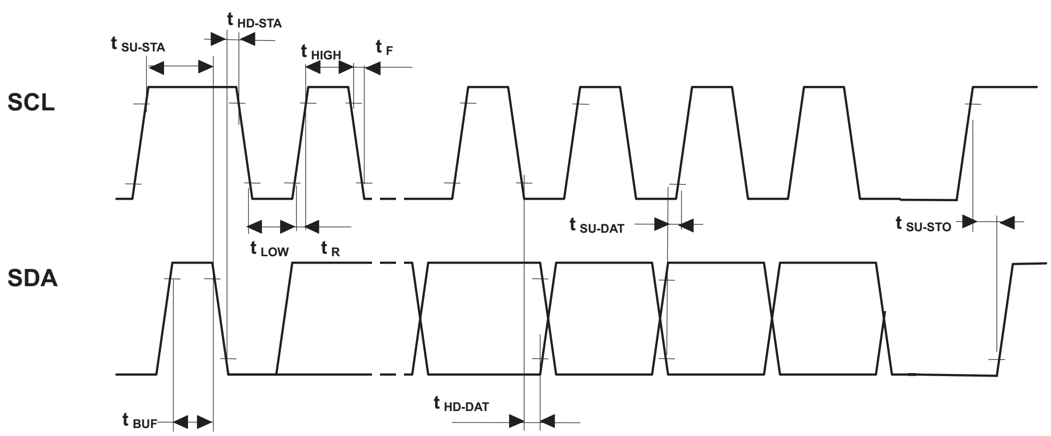
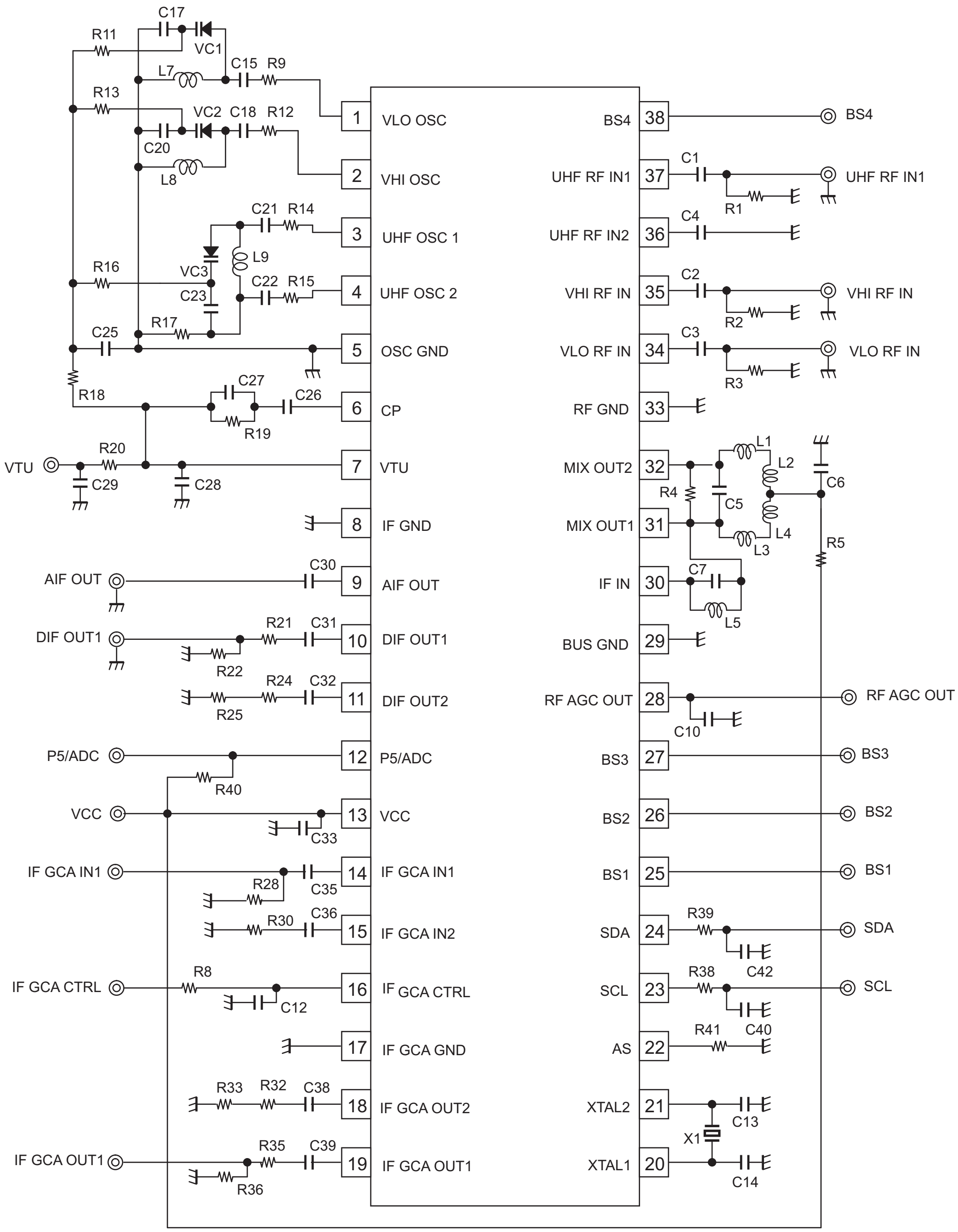


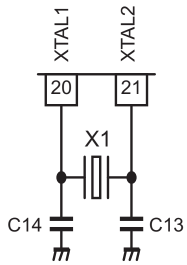
Figure 23. I²C Timing

APPLICATION INFORMATION



NOTE: This application information is advisory and performance-check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Figure 24. Reference Measurement Circuit



Crystal X1		Capacitors	
Frequency	Type	C13	C14
4 MHz	HC49SFNB04000H0 (Kyocera)	27 pF	27 pF
16 MHz	CX3225GB16000D0 (Kyocera)	14 pF	14 pF

Figure 25. Reference Crystal Oscillation Circuit

Table 12. Component Values for Measurement Circuit

PART NAME	VALUE	PART NAME	VALUE
C1 (UHF RFIN1)	2.2nF	R1 (UHF RFIN1)	Open (51Ω)
C2 (VHI RFIN)	2.2nF	R2 (VHI RFIN)	Open (51Ω)
C3 (VLO RFIN)	2.2nF	R3 (VLO RFIN)	Open (51Ω)
C4 (UHF RFIN)	2.2nF	R4 (MIXOUT)	Open
C5 (MIXOUT)	5.5pF	R5 (MIXOUT)	0Ω
C6 (MIXOUT)	2.2nF	R8 (IF GCA CTRL)	0Ω
C7 (IF IN)	0Ω	R9 (VLO OSC)	0Ω
C10 (RF AGC OUT)	0.15µF	R11 (VLO OSC)	3.3kΩ
C12 (IF GCA CTRL)	0.1µF	R12 (VHI OSC)	10Ω
C13 (XTAL2)	27pF	R13 (VHI OSC)	3.3kΩ
C14 (XTAL1)	27pF	R14 (UHF OSC)	4.7Ω
C15 (VLO OSC)	4pF	R15 (UHF OSC)	4.7Ω
C17 (VLO OSC)	68pF	R16 (UHF OSC)	1kΩ
C18 (VHI OSC)	10pF	R17 (UHF OSC)	2.2kΩ
C20 (VHI OSC)	130pF	R18 (VTU)	3.3kΩ
C21 (UHF OSC)	6pF	R19 (CP)	82kΩ
C22 (UHF OSC)	6pF	R20 (VTU)	22kΩ
C23 (UHF OSC)	20pF	R21 (DIF OUT1)	200Ω
C25 (VTU)	2.2nF/50V	R22 (DIF OUT1)	Open
C26 (CP)	3.9nF/50V	R24 (DIF OUT2)	200Ω
C27 (CP)	10pF/50V	R25 (DIF OUT2)	51Ω
C28 (VTU)	150pF/50V	R28 (IF GCA IN1)	(51Ω)
C29 (VTU)	2.2nF/50V	R30 (IF GCA IN2)	(0Ω)
C30 (AIF OUT)	2.2nF	R32 (IF GCA OUT2)	200Ω
C31 (DIF OUT1)	2.2nF	R33 (IF GCA OUT2)	51Ω
C32 (DIF OUT2)	2.2nF	R35 (IF GCA OUT1)	200Ω
C33 (VCC)	0.1µF	R36 (IF GCA OUT1)	Open
C35 (IF GCA IN1)	2.2nF	R38 (SCL)	330Ω
C36 (IF GCA IN2)	2.2nF	R39 (SDA)	330Ω
C38 (IF GCA OUT2)	2.2nF	R40 (P5)	Open
C39 (IF GCA OUT1)	2.2nF	R41 (AS)	Open
C40 (SCL)	Open		
C42 (SDA)	Open	VC1 (VLO OSC)	KDV270E
		VC2 (VHI OSC)	KDV270E
		VC3 (UHF OSC)	KDV216E
		X1	4MHz crystal

Table 12. Component Values for Measurement Circuit (continued)

PART NAME	VALUE		PART NAME	VALUE
L1 (MIXOUT)	470nH (LK1608R47KT Taiyo Yuden)			
L2 (MIXOUT)	560nH (LK1608R56KT Taiyo Yuden)			
L3 (MIXOUT)	470nH (LK1608R47KT Taiyo Yuden)			
L4 (MIXOUT)	560nH (LK1608R56KT Taiyo Yuden)			
L5 (IFIN)	Open			
L7 (VLO OSC)	ϕ3.0mm, 9T, wire0.32mm			
L8 (VHI OSC)	ϕ1.8mm, 4T, wire0.4mm			
L9 (UHF OSC)	ϕ1.8mm, 2T, wire0.4mm			

IF frequency: 36 MHz

Local frequency range: VHF-LOW: 87 to 186 MHz
VHF-HIGH: 193 to 462 MHz
UHF: 470 to 894 MHz

Test Circuits

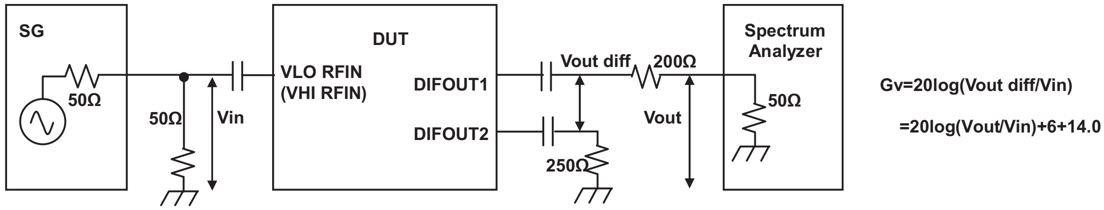


Figure 26. VHF Conversion Gain Measurement Circuit (at DIFOUT)

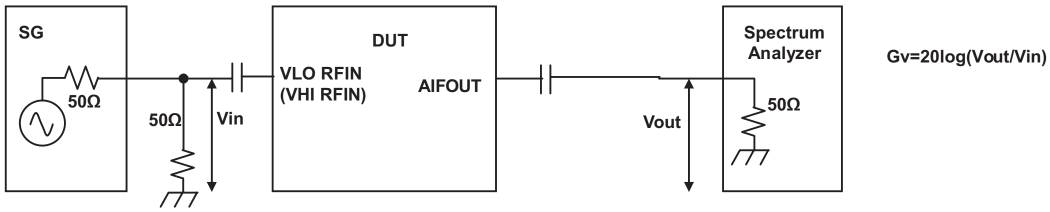


Figure 27. VHF Conversion Gain Measurement Circuit (at AIFOUT)

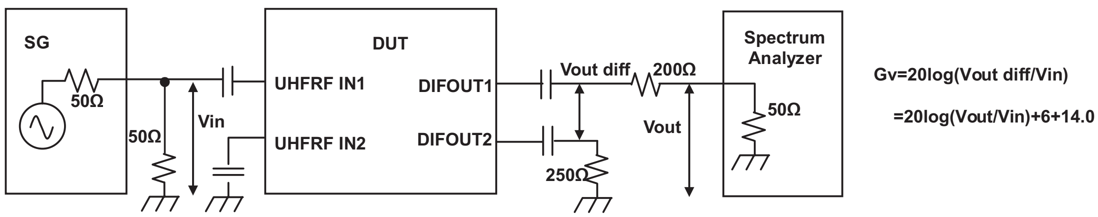


Figure 28. UHF Conversion Gain Measurement Circuit (at DIFOUT)

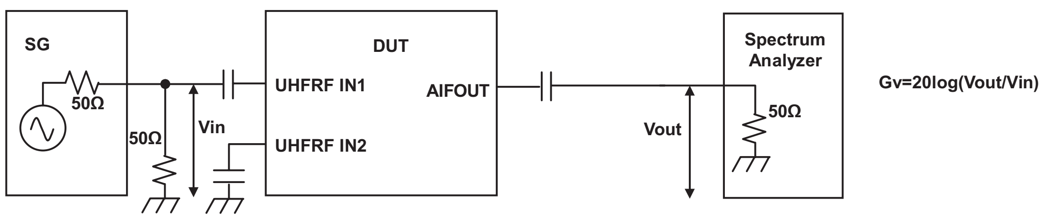


Figure 29. UHF Conversion Gain Measurement Circuit (at AIFOUT)

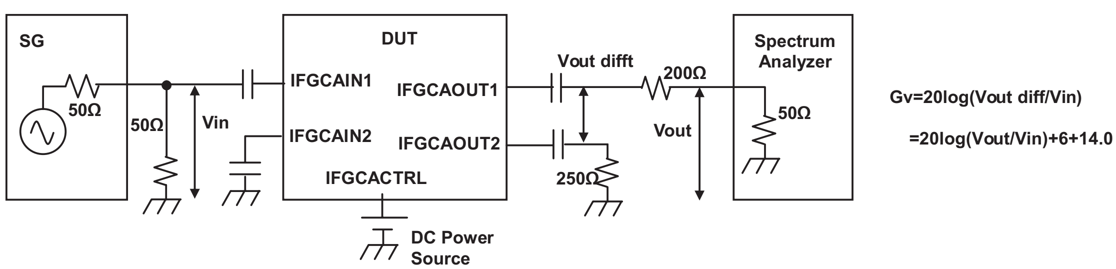


Figure 30. IF GCA Gain Measurement Circuit

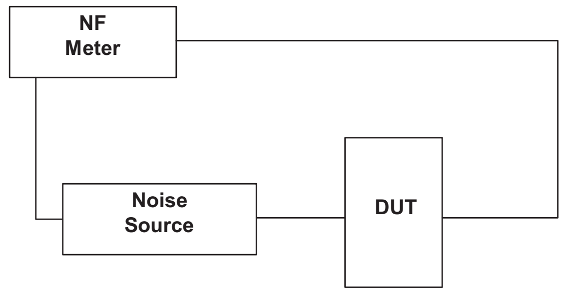


Figure 31. Noise Figure Measurement Circuit

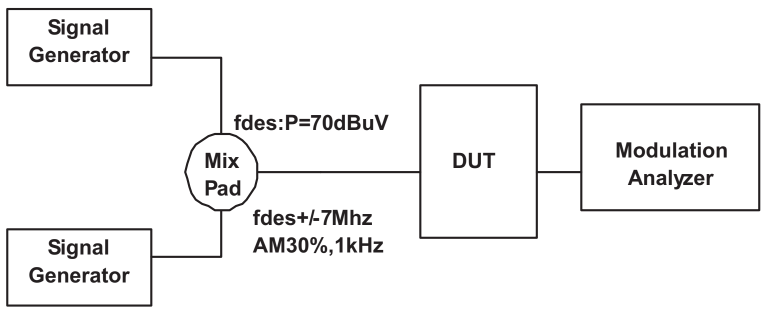


Figure 32. 1% Cross Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band Switch Driver Output Voltage (BS1-BS4)

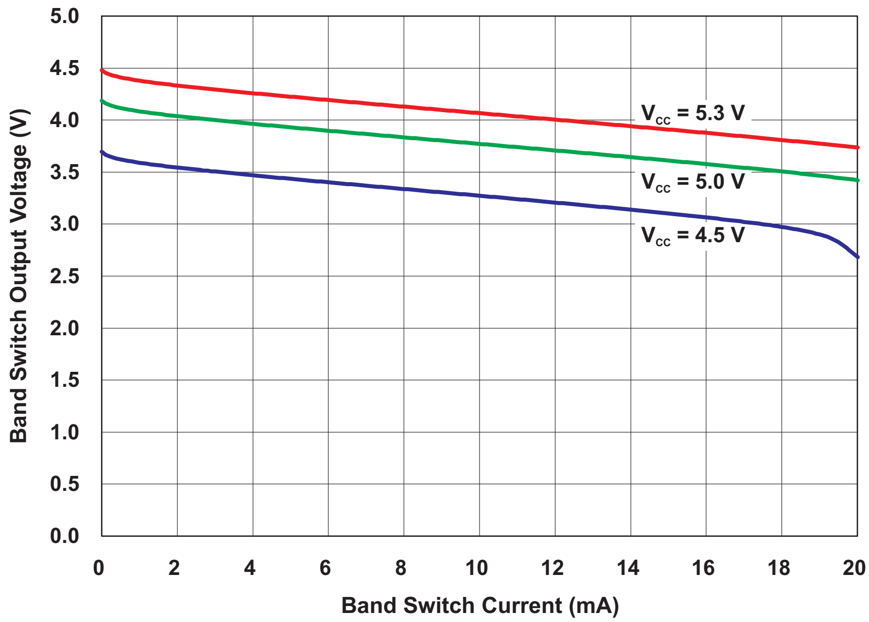


Figure 33. Band Switch Driver Output Voltage

S-Parameter

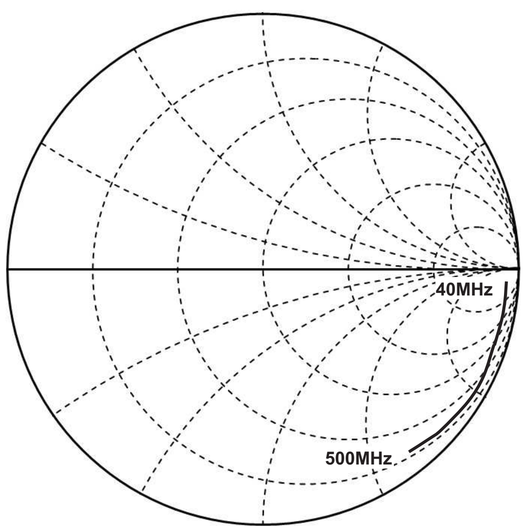


Figure 34. VLO, VHI RFIN

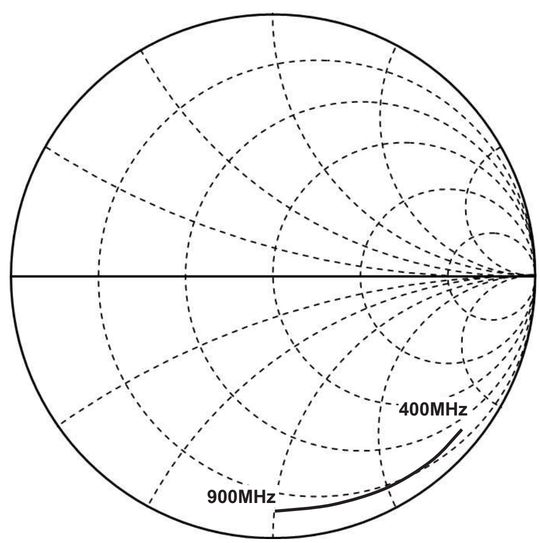


Figure 35. UHF RFIN

TYPICAL CHARACTERISTICS (continued)

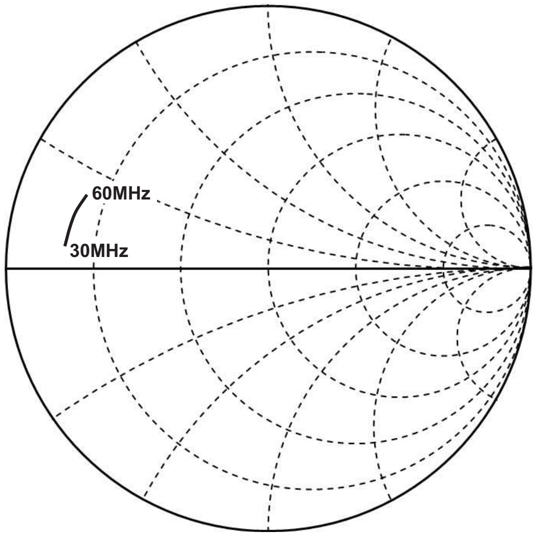


Figure 36. DIFOUT

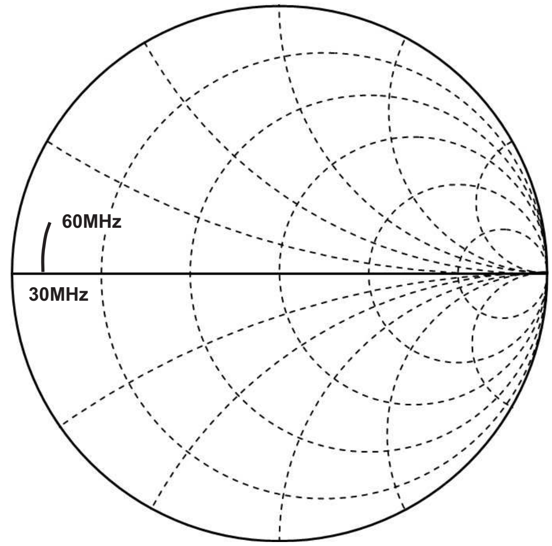


Figure 37. AIFOUT

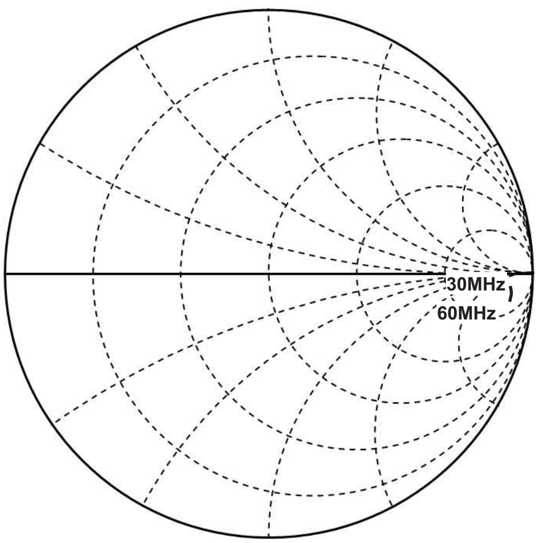


Figure 38. IF GCA IN

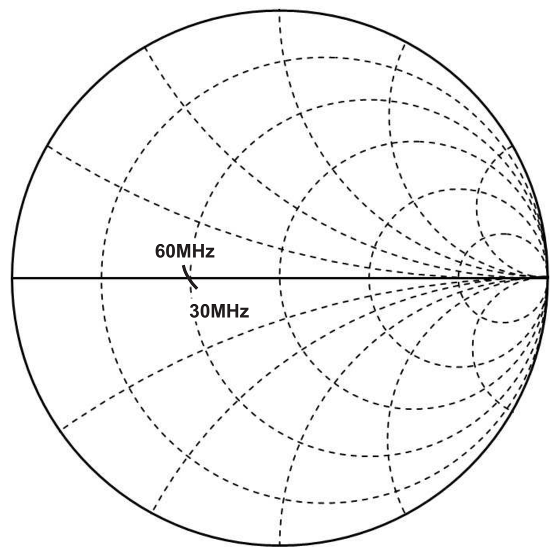


Figure 39. IF GCAOUT

TYPICAL CHARACTERISTICS (continued)

IF GCA Gain vs Control Voltage

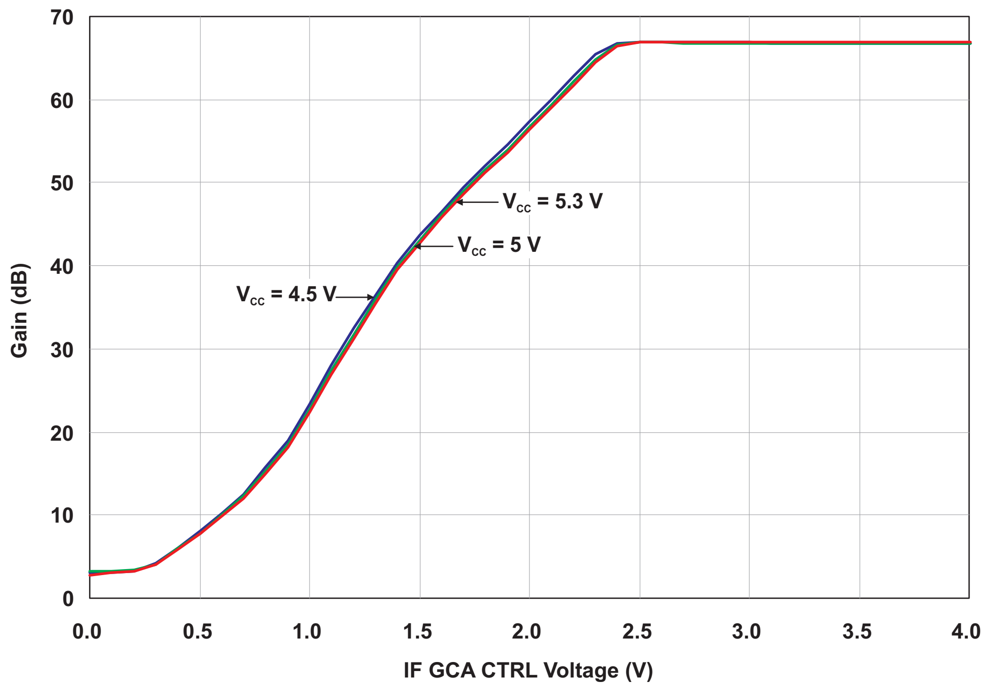


Figure 40. IF GCA Gain vs Control Voltage

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN761645DBTR	NRND	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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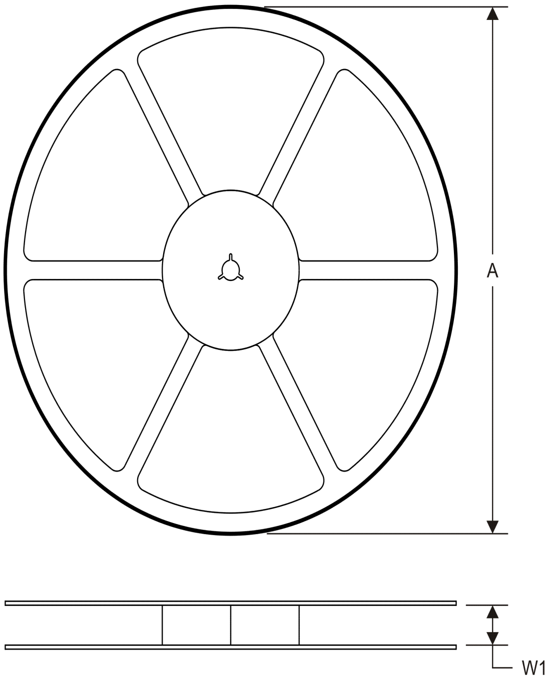
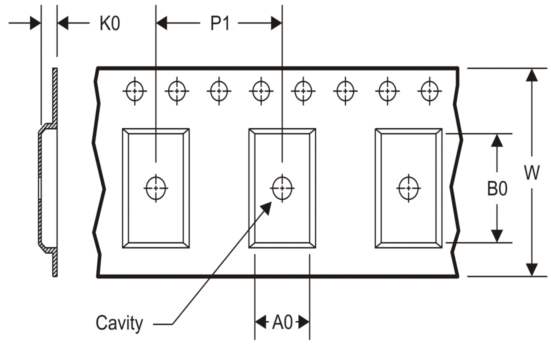
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



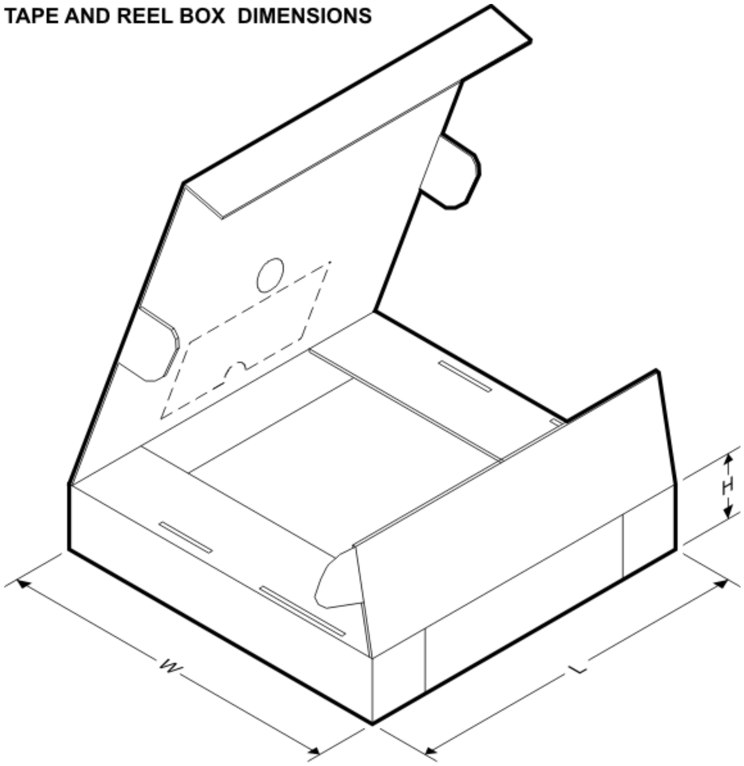
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN761645DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

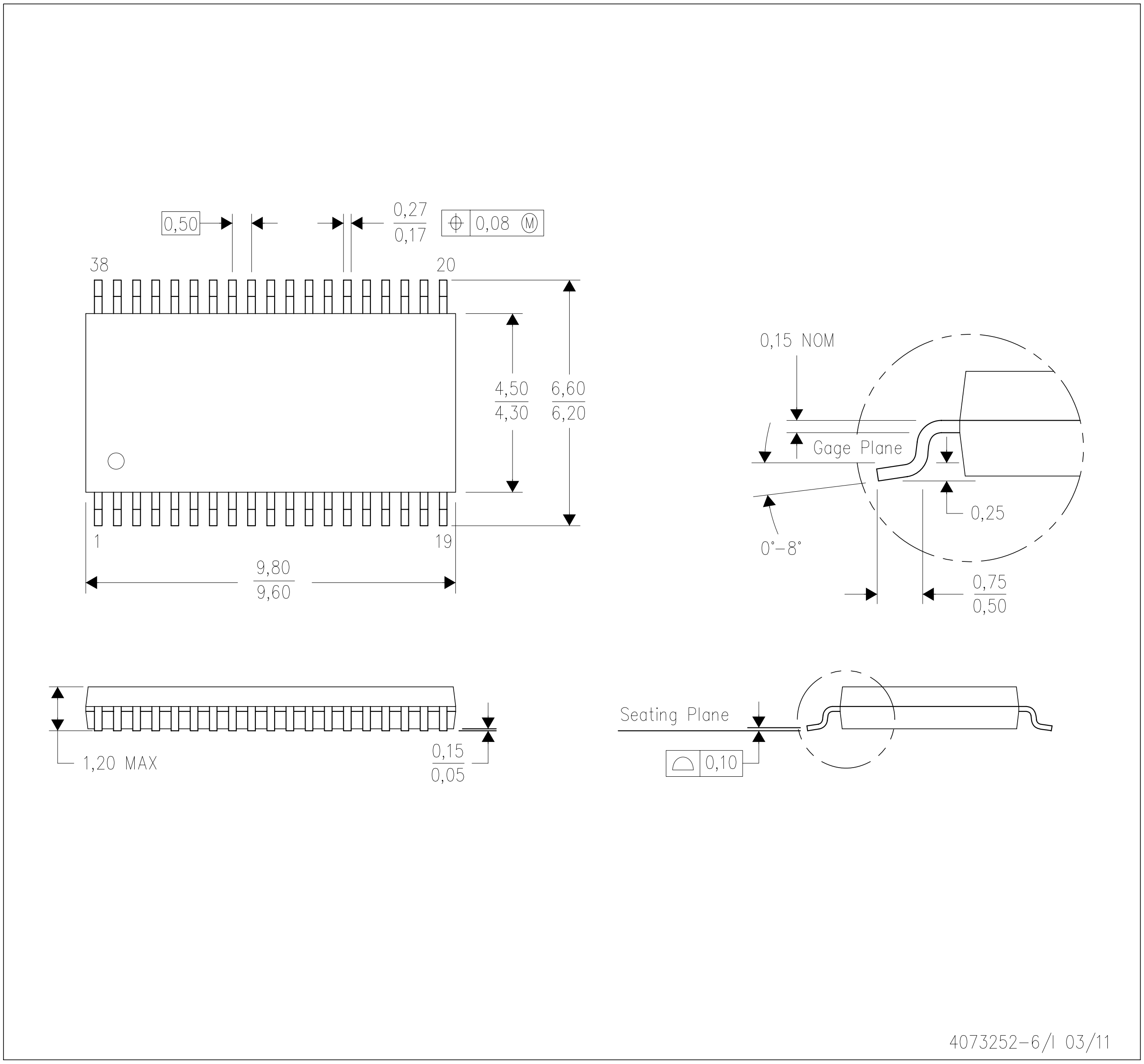
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

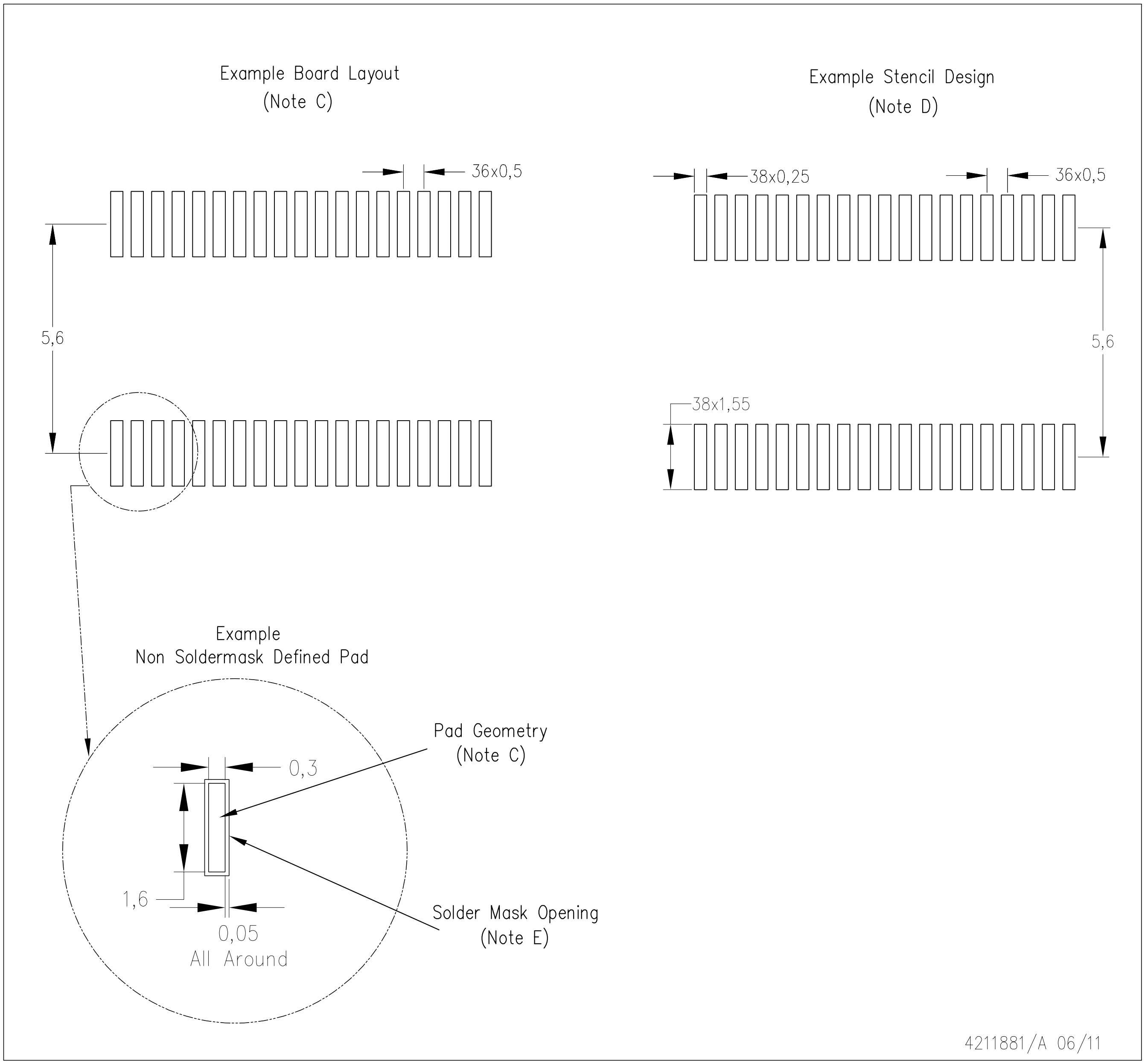
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN761645DBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

DBT (R–PDSO–G38) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

DBT (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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