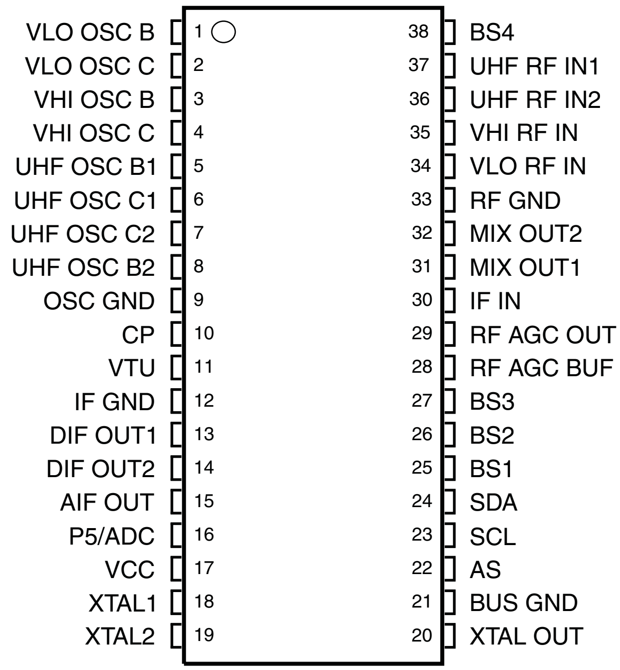
DIGITAL TV TUNER IC

FEATURES

- **Integrated Mixer/Oscillator/PLL**
- **VHF-L, VHF-H, UHF 3-Band Local Oscillator**
- **RF AGC Detector Circuit**
- **I²C Bus Protocol**
  Bidirectional Data Transmission
- **High-Voltage Tuning Voltage Output**
- **Four NPN-Type Band Switch Drivers**
- **One Auxiliary Port/5-Level ADC**
- **Crystal Oscillator Output**
- **Programmable Reference Divider Ratio (24/28/32/64/80/128)**
- **Selectable Digital IFOUT and Analog IFOUT**
- **Standby Mode**
- **5-V Power Supply**
- **38-Pin Thin Shrink Small-Outline Package (TSSOP)**

DBT PACKAGE
(TOP VIEW)



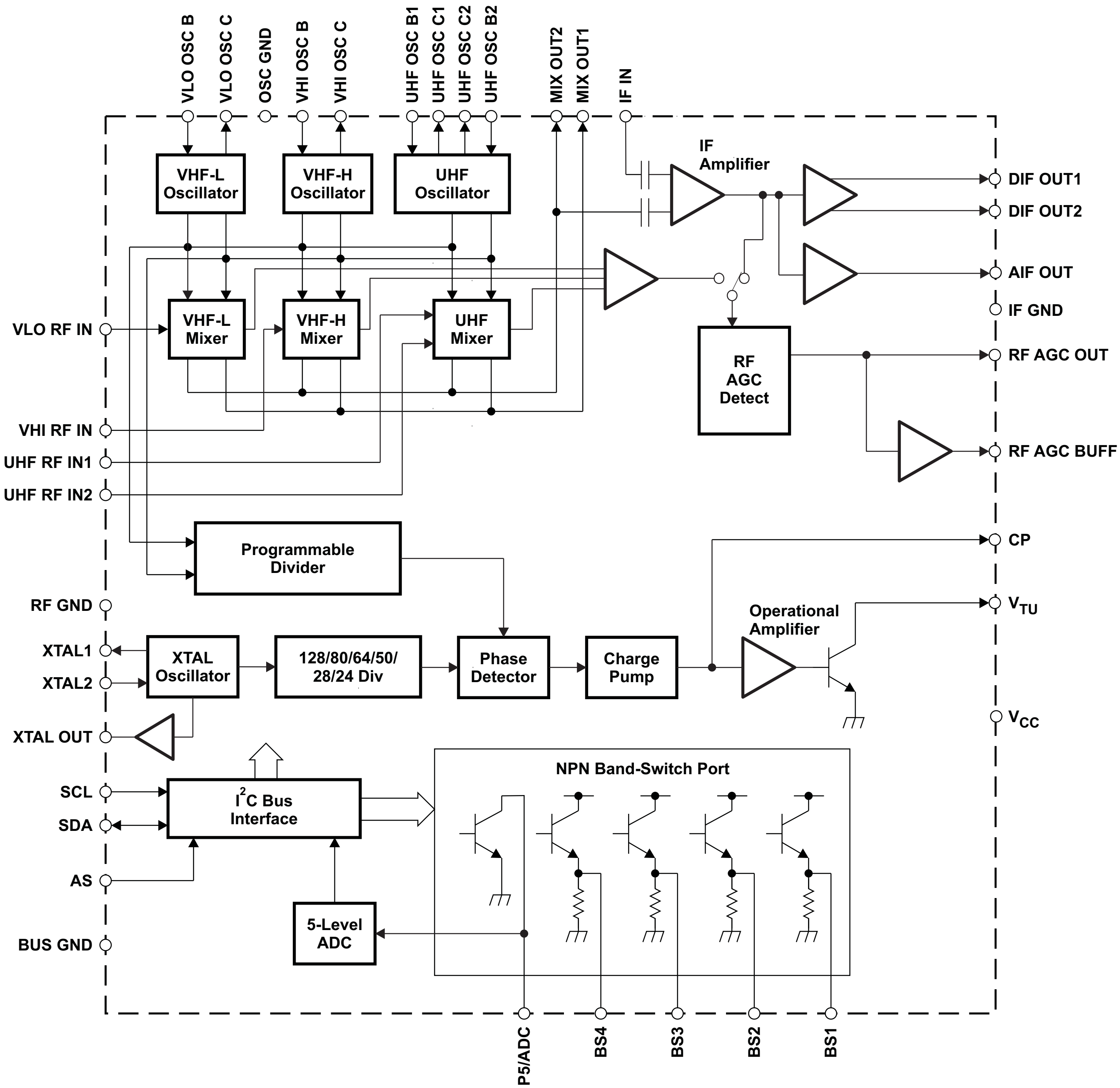
APPLICATIONS

- **Digital TVs**
- **Digital CATVs**
- **Set-Top Boxes**

DESCRIPTION

The SN761642 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, and RF AGC detector circuit. The SN761642 is available in a small-outline package.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION	SCHEMATIC
NAME	NO.		
AIF OUT	15	IF amplifier output (analog)	Figure 1
AS	22	Address selection input	Figure 2
BS1	25	Band switch 1 output	Figure 3
BS2	26	Band switch 2 output	Figure 3
BS3	27	Band switch 3 output	Figure 3
BS4	38	Band switch 4 output	Figure 3
BUS GND	21	BUS ground	
CP	10	Charge-pump output	Figure 4
DIF OUT1	13	IF amplifier output 1	Figure 6
DIF OUT2	14	IF amplifier output 2	Figure 6
IF GND	12	IF ground	
IF IN	30	IF amplifier input	Figure 5
MIXOUT1	31	Mixer output 1	Figure 7
MIXOUT2	32	Mixer output 2	Figure 7
OSC GND	9	Oscillator ground	
P5/ADC	16	Port-5 output/ADC input	Figure 8
RF AGC BUF	28	RF AGC buffer output	Figure 9
RF AGC OUT	29	RF AGC output	Figure 10
RF GND	33	RF ground	
SCL	23	Serial clock input	Figure 11
SDA	24	Serial data input/output	Figure 12
UHF OSC B1	5	UHF oscillator base 1	Figure 13
UHF OSC B2	8	UHF oscillator base 2	Figure 13
UHF OSC C1	6	UHF oscillator collector 1	Figure 13
UHF OSC C2	7	UHF oscillator collector 2	Figure 13
UHF RF IN1	37	UHF RF input 1	Figure 14
UHF RF IN2	36	UHF RF input 2	Figure 14
V_{CC}	17	Supply voltage	
VHI OSC B	3	VHF-H oscillator base	Figure 15
VHI OSC C	4	VHF-H oscillator collector	Figure 15
VHI RF IN	35	VHF-H RF input	Figure 16
VLO OSC B	1	VHF-L oscillator base	Figure 17
VLO OSC C	2	VHF-L oscillator collector	Figure 17
VLO RF IN	34	VHF-L RF input	Figure 18
VTU	11	Tuning voltage amplifier output	Figure 19
XTAL1	18	4-MHz crystal oscillator	Figure 20
XTAL2	19	4-MHz crystal oscillator	Figure 20
XTALOUT	20	4-MHz crystal oscillator buffer output	Figure 21

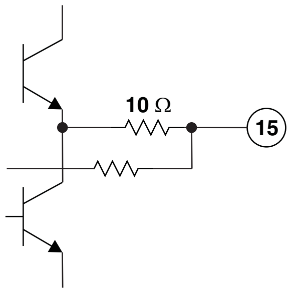


Figure 1. AIF OUT

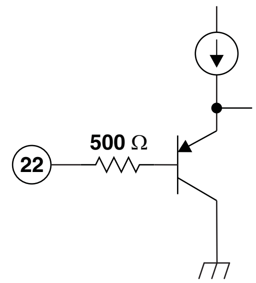


Figure 2. AS

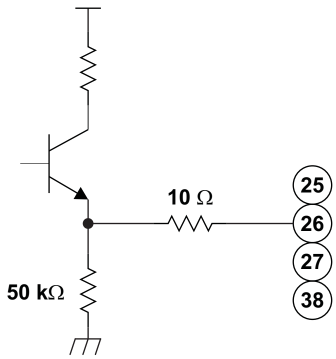


Figure 3. BS1, BS2, BS3, and BS4

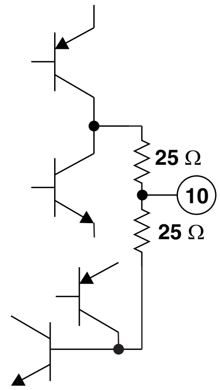


Figure 4. CP

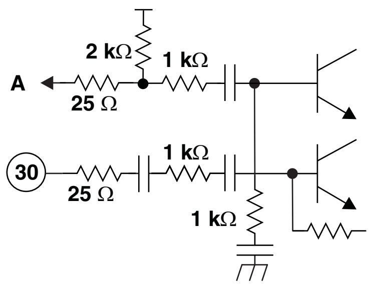


Figure 5. IF IN

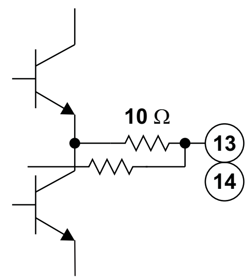


Figure 6. DIF OUT1 and DIF OUT2

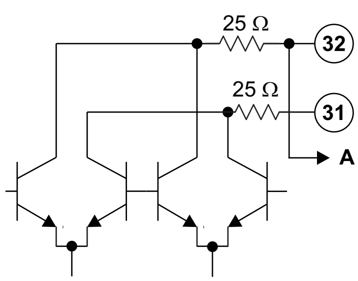


Figure 7. MIXOUT1 and MIXOUT2

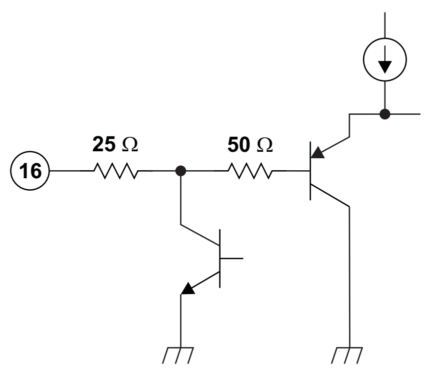


Figure 8. P5/ADC

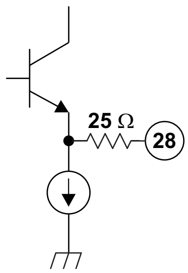


Figure 9. RF AGC BUF

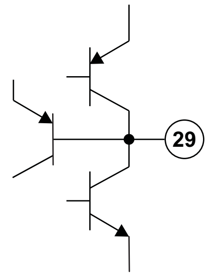


Figure 10. RF AGC OUT

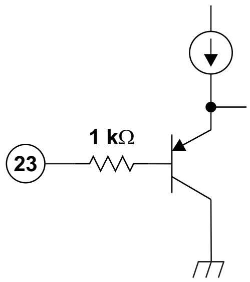


Figure 11. SCL

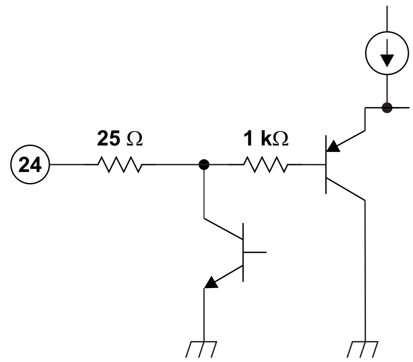


Figure 12. SDA

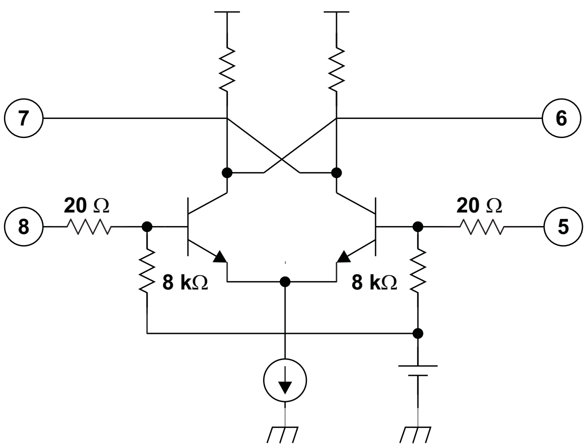


Figure 13. UHF OSC B1, UHF OSC B2, UHF OSC C1, and UHF OSC C2

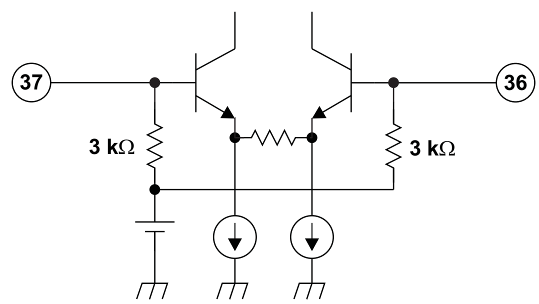


Figure 14. UHF RF IN1 and UHF RF IN2

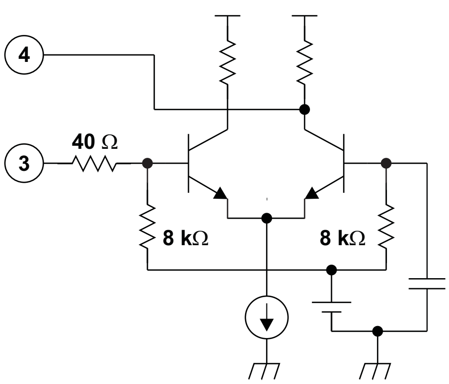


Figure 15. VHI OSC B and VHI OSC C

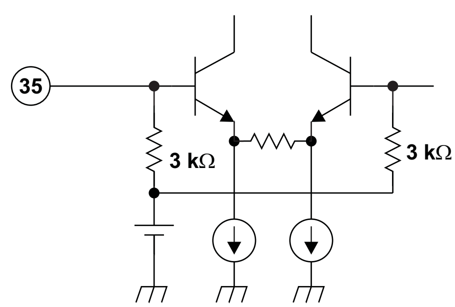


Figure 16. VHI RF IN

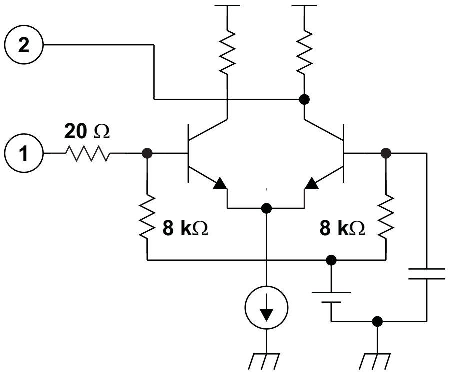


Figure 17. VLO OSC B and VLO OSC C

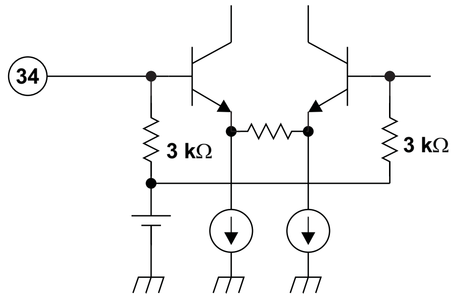


Figure 18. VLO RF IN

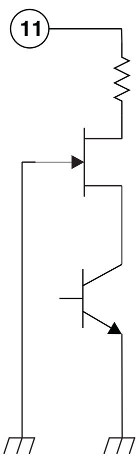


Figure 19. VTU

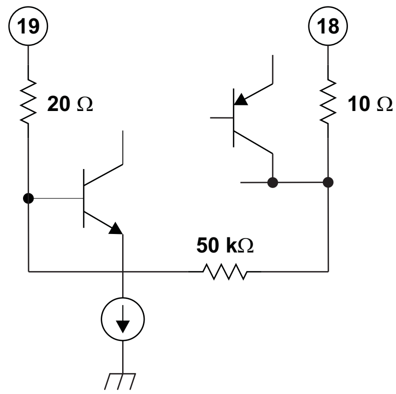


Figure 20. XTAL1 and XTAL2

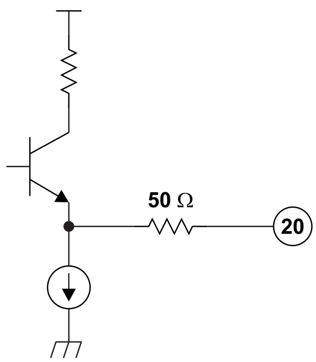


Figure 21. XTALOUT

ABSOLUTE MAXIMUM RATINGS[1]

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range [2]	V_{CC}	–0.4	6.5	V
V_{GND}	Input voltage range 1 [2]	RF GND, OSC GND	–0.4	0.4	V
VTU	Input voltage range 2 [2]	VTU	–0.4	35	V
V_{IN}	Input voltage range 3 [2]	Other pins	–0.4	6.5	V
P_D	Continuous total dissipation [3]	$T_A \leq 25°C$		1276	mW
T_A	Operating free-air temperature range		–20	85	°C
T_{stg}	Storage temperature range		–65	150	°C
T_J	Maximum junction temperature			150	°C
$t_{SC(max)}$	Maximum short-circuit time	Each pin to V_{CC} or to GND		10	s

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 10.2 mW/°C for $T_A \geq 25°C$.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	V_{CC}	4.5	5	5.5	V
VTU	Tuning supply voltage	VTU		30	33	V
I_{BS}	Output current of band switch	BS1 – BS4, one bandswitch on			10	mA
I_{P5}	Output current of port 5	P5/ADC			–5	mA
T_A	Operating free-air temperature		–20		85	°C

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

IF IN, MIXOUT1, and MIXOUT2 (pins 30–32) withstand 1.5 kV, and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

ELECTRICAL CHARACTERISTICS

Total Device and Serial Interface

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}1$	Supply current 1	BS[1:4] = 0100, DIFOUT enabled		90	120	mA
$I_{CC}2$	Supply current 2	BS[1:4] = 0100, DIFOUT enabled, I_{BS} = 10 mA		100	130	mA
$I_{CC-STBY}$	Standby supply current	BS[1:4] = 1100		9	14	mA
V_{IH}	High-level input voltage (SCL, SDA)		2.3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.05	V
I_{IH}	High-level input current (SCL, SDA)				10	μA
I_{IL}	Low-level input current (SCL, SDA)		–10			μA
V_{POR}	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
I²C Interface						
V_{ASH}	Address-select high-input voltage (AS)	V_{CC} = 5 V	4.5		5	V
V_{ASM1}	Address-select mid-input 1 voltage (AS)	V_{CC} = 5 V	2		3	V
V_{ASM2}	Address-select mid-input 2 voltage (AS)	V_{CC} = 5 V	1		1.5	V
V_{ASL}	Address-select low-input voltage (AS)	V_{CC} = 5 V			0.5	V
I_{ASH}	Address-select high-input current (AS)				50	μA
I_{ASL}	Address-select low-input current (AS)		–10			μA
V_{ADC}	ADC input voltage	See Table 10	0		V_{CC}	V
I_{ADH}	ADC high-level input current	V_{ADC} = V_{CC}			10	μA
I_{ADL}	ADC low-level input current	V_{ADC} = 0 V	–10			μA
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High-level output leakage current (SDA)	V_{SDA} = 5.5 V			10	μA
f_{SCL}	Clock frequency (SCL)			100	400	kHz
t_{HD-DAT}	Data hold time	See Figure 22	0		0.9	μs
t_{BUF}	Bus free time		1.3			μs
t_{HD-STA}	Start hold time		0.6			μs
t_{LOW}	SCL-low hold time		1.3			μs
t_{HIGH}	SCL-high hold time		0.6			μs
t_{SU-STA}	Start setup time		0.6			μs
t_{SU-DAT}	Data setup time		0.1			μs
t_r	Rise time (SCL, SDA)				0.3	μs
t_f	Fall time (SCL, SDA)				0.3	μs
t_{SU-STO}	Stop setup time		0.6			μs

PLL and Band Switch

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
f_{XTAL}	Crystal oscillator frequency	R_{XTAL} = 25 Ω to 300 Ω		4		MHz
Z_{XTAL}	Crystal oscillator input impedance		1.6	2.4		kΩ
V_{XLO}	XTALOUT output voltage	Load = 10 pF/5.1 kΩ, V_{CC} = 5 V, T_A = 25°C		0.48		Vp-p
V_{VTUL}	Tuning amplifier low-level output voltage	R_L = 22 kΩ, VTU = 30 V	0.2	0.3	0.46	V
I_{VTUOFF}	Tuning amplifier leakage current	Tuning amplifier = off, VTU = 30 V			10	µA
I_{CP11}	Charge-pump current	CP[2:0] = 011	450	600	750	µA
I_{CP10}		CP[2:0] = 010	250	350	450	
I_{CP01}		CP[2:0] = 001	100	140	200	
I_{CP00}		CP[2:0] = 000	35	70	95	
I_{CP100}		CP[2:0] = 100, Mode = 1	650	900	1200	
V_{CP}	Charge-pump output voltage	PLL locked		1.95		V
I_{CPOFF}	Charge-pump leakage current	V_{CP} = 2 V, T_A = 25°C	–15		15	nA
I_{BS}	Band switch driver output current (BS1–BS4)				10	mA
V_{BS1}	Band switch driver output voltage (BS1–BS4)	I_{BS} = 10 mA	3			V
V_{BS2}		I_{BS} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.5	3.7		
I_{BSOFF}	Band switch driver leakage current (BS1–BS4)	V_{BS} = 0 V			8	µA
I_{P5}	Band switch port sink current (P5/ADC)				–5	mA
V_{P5ON}	Band switch port output voltage (P5/ADC)	I_{P5} = –2 mA, V_{CC} = 5 V, T_A = 25°C			0.6	V

RF AGC(1)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 23 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OAGC0}	RF AGC output source current	ATC = 0		300		nA
I_{OAGC1}		ATC = 1		9		µA
$I_{OAGCSINK}$	RF AGC peak sink current	ATC = 0		100		µA
V_{OAGCH}	RFAGCOUT output high voltage (max level)	ATC = 1	3.5	4	4.5	V
V_{OAGCL}	RFAGCOUT output low voltage (min level)	ATC = 1		0.3		V
I_{AGCBUF}	RFAGCBUF output current	ATC = 0		1.5		mA
$V_{OAGCBFH}$	RFAGCBUF output high voltage (max level)	ATC = 1	3.5	4	4.5	V
$V_{OAGCBFL}$	RFAGCBUF output low voltage (min level)	ATC = 1		0.3		V
$V_{AGCSP00}$	Start-point IF output level	ATP[2:0] = 000, ATC=0, AISL=0		114		dBµV
$V_{AGCSP01}$		ATP[2:0] = 001, ATC=0, AISL=0		112		
$V_{AGCSP02}$		ATP[2:0] = 010, ATC=0, AISL=0		110		
$V_{AGCSP03}$		ATP[2:0] = 011, ATC=0, AISL=0		108		
$V_{AGCSP04}$		ATP[2:0] = 100, ATC=0, AISL=0		106		
$V_{AGCSP05}$		ATP[2:0] = 101, ATC=0, AISL=0		104		
$V_{AGCSP06}$		ATP[2:0] = 110, ATC=0, AISL=0		102		

(1) When AISL=1, RF AGC function is not available at VHF-L band (output level is undefined).

Mixer, Oscillator, IF Amplifier (DIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 23 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{C1D}	Conversion gain (mixer-IF amplifier), VHF-LOW	f_{in} = 57 MHz (1)	35	dB
G_{C3D}		f_{in} = 171 MHz (1)	35	
G_{C4D}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 177 MHz (1)	35	dB
G_{C6D}		f_{in} = 467 MHz (1)	35	
G_{C7D}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 473 MHz (1)	35	dB
G_{C9D}		f_{in} = 864 MHz (1)	35	
NF_{1D}	Noise figure, VHF-LOW	f_{in} = 57 MHz	9	dB
NF_{3D}		f_{in} = 171 MHz	9	
NF_{4D}	Noise figure, VHF-HIGH	f_{in} = 177 MHz	9	dB
NF_{6D}		f_{in} = 467 MHz	10	
NF_{7D}	Noise figure, UHF	f_{in} = 473 MHz	10	dB
NF_{9D}		f_{in} = 864 MHz	12	
CM_{1D}	Input voltage causing 1% cross-modulation distortion, VHF-LOW	f_{in} = 57 MHz (2)	79	dBμV
CM_{3D}		f_{in} = 171 MHz (2)	79	
CM_{4D}	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	f_{in} = 177 MHz (2)	79	dBμV
CM_{6D}		f_{in} = 467 MHz (2)	79	
CM_{7D}	Input voltage causing 1% cross-modulation distortion, UHF	f_{in} = 473 MHz (2)	77	dBμV
CM_{9D}		f_{in} = 864 MHz (2)	77	
V_{IFO1D}	IF output voltage, VHF-LOW	f_{in} = 57 MHz	117	dBμV
V_{IFO3D}		f_{in} = 171 MHz	117	
V_{IFO4D}	IF output voltage, VHF-HIGH	f_{in} = 177 MHz	117	dBμV
V_{IFO6D}		f_{in} = 467 MHz	117	
V_{IFO7D}	IF output voltage, UHF	f_{in} = 473 MHz	117	dBμV
V_{IFO9D}		f_{in} = 864 MHz	117	
Φ_{PLVL1D}	Phase noise, VHF-LOW	f_{in} = 57 MHz (3)	–90	dBc/Hz
Φ_{PLVL3D}		f_{in} = 171 MHz (4)	–85	
Φ_{PLVL4D}	Phase noise, VHF-HIGH	f_{in} = 177 MHz (3)	–85	dBc/Hz
Φ_{PLVL6D}		f_{in} = 467 MHz (4)	–77	
Φ_{PLVL7D}	Phase noise, UHF	f_{in} = 473 MHz (3)	–80	dBc/Hz
Φ_{PLVL9D}		f_{in} = 864 MHz (4)	–77	

(1) IF = 44 MHz, RF input level = 70 dBμV, differential output
(2) f_{undes} = f_{des} ±6 MHz, Pin = 70 dBμV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 1 kHz, CP current = 350 μA, reference divider = 64
(4) Offset = 1 kHz, CP current = 900 μA, reference divider = 64

Mixer, Oscillator, IF Amplifier (AIF OUT)

V_{CC} = 5 V, T_A = 25°C, measured in Figure 23 reference measurement circuit at 50-Ω system, IF = 45.75 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{C1A}	Conversion gain (mixer-IF amplifier), VHF-LOW	f_{in} = 55.25 MHz(1)	29	dB
G_{C3A}		f_{in} = 169.25 MHz(1)	29	
G_{C4A}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 175.25 MHz(1)	29	dB
G_{C6A}		f_{in} = 465.25 MHz(1)	29	
G_{C7A}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 471.25 MHz(1)	29	dB
G_{C9A}		f_{in} = 862.25 MHz(1)	29	
NF_{1A}	Noise figure, VHF-LOW	f_{in} = 55.25 MHz	9	dB
NF_{3A}		f_{in} = 169.25 MHz	9	
NF_{4A}	Noise figure, VHF-HIGH	f_{in} = 175.25 MHz	9	dB
NF_{6A}		f_{in} = 465.25 MHz	10	
NF_{7A}	Noise figure, UHF	f_{in} = 471.25 MHz	10	dB
NF_{9A}		f_{in} = 862.25 MHz	12	
CM_{1A}	Input voltage causing 1% cross-modulation distortion, VHF-LOW	f_{in} = 55.25 MHz(2)	79	dBµV
CM_{3A}		f_{in} = 169.25 MHz(2)	79	
CM_{4A}	Input voltage causing 1% cross-modulation distortion, VHF-HIGH	f_{in} = 175.25 MHz(2)	79	dBµV
CM_{6A}		f_{in} = 465.25 MHz(2)	79	
CM_{7A}	Input voltage causing 1% cross-modulation distortion, UHF	f_{in} = 471.25 MHz(2)	79	dBµV
CM_{9A}		f_{in} = 862.25 MHz(2)	77	
V_{IFO1A}	IF output voltage, VHF-LOW	f_{in} = 55.25 MHz	117	dBµV
V_{IFO3A}		f_{in} = 169.25 MHz	117	
V_{IFO4A}	IF output voltage, VHF-HIGH	f_{in} = 175.25 MHz	117	dBµV
V_{IFO6A}		f_{in} = 465.25 MHz	117	
V_{IFO7A}	IF output voltage, UHF	f_{in} = 471.25 MHz	117	dBµV
V_{IFO9A}		f_{in} = 862.25 MHz	117	
Φ_{PLVL1A}	Phase noise, VHF-LOW	f_{in} = 55.25 MHz(3)	–95	dBc/Hz
Φ_{PLVL3A}		f_{in} = 169.25 MHz(3)	–95	
Φ_{PLVL4A}	Phase noise, VHF-HIGH	f_{in} = 175.25 MHz(3)	–90	dBc/Hz
Φ_{PLVL6A}		f_{in} = 465.25 MHz(3)	–90	
Φ_{PLVL7A}	Phase noise, UHF	f_{in} = 471.25 MHz(3)	–85	dBc/Hz
Φ_{PLVL9A}		f_{in} = 862.25 MHz(3)	–90	

(1) IF = 44 MHz, RF input level = 70 dBµV
(2) f_{undes} = f_{des} ±6 MHz, Pin = 70 dBµV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) Offset = 10 kHz, CP current = 70 µA, reference divider = 128

FUNCTIONAL DESCRIPTION

I^2C Bus Mode

I^2C Write Mode ($R/\overline{W}$ = 0)

Table 1. Write Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	$R/\overline{W}$ = 0	A(1)
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A(1)
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A(1)
Control byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A(1)
Band switch byte (BB)	CP1	CP0	AISL	P5	BS4	BS3	BS2	BS1	A(1)
Control byte 2 (CB2)	1	1	ATC	MODE	T3	T2/IFDA	T1/CP2	T0/XLO	A(1)

(1) A : acknowledge

Table 2. Write Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address-set bits (see Table 3)	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$	N14 = N13 = N12 = ... = N0 = 0
ATP[2:0]	RF AGC start-point control bits (see Table 4)	ATP[2:0] = 000
RS[2:0]	Reference divider ratio-selection bits (see Table 5)	RS[2:0] = 000
CP[1:0]	Charge-pump current-set bit (see Table 6)	CP[1:0] = 00
AISL(1)	RF AGC detector input selection bit AISL = 0: IF amplifier AISL = 1: Mixer output	AISL = 0
P5	Port output/ADC input control bit P5 = 0: ADC INPUT P5 = 1: Tr = ON	P5 = 0
BS[4:1]	Band switch control bits BSn = 0: Tr = OFF BSn = 1: Tr = ON	BSn = 0
	Band selection by BS[1:2] **BS1** **BS2** 1 0 VHF-LO 0 1 VHF-HI 0 0 UHF 1 1 Standby mode/stop MOP function (XTALOUT is available in standby mode)	
ATC	RF AGC current-set bit ATC = 0: Current = 300 nA ATC = 1: Current = 9 µA	ATC = 0
Mode T3 T2/IFDA T1/CP2 T0/XLO	Mode = 0: DIFOUT1, 2 selected T3, T2/IFDA, T1/CP2, T0/XLO are test bits and XTALOUT control bit (see Table 7)	MODE = 0 T[3:0] = 0000
	Mode = 1: T2/IFDA = 0 : DIFOUT1, 2 selected T2/IFDA = 1 : AIFOUT selected T1/CP2 : Icp control bit, See Table 6 T0/XLO = 0 : XTALOUT enabled T0/XLO = 1 : XTALOUT disabled	

(1) When AISL=1, RF AGC function is not available at VHF-L band (Output level is undefined.)

Table 3. Address Selection

MA1	MA0	VOLTAGE APPLIED ON AS INPUT
0	0	0 V to 0.1 V_{CC} (Low)
0	1	OPEN, or 0.2 V_{CC} to 0.3 V_{CC} (Mid2)
1	0	0.4 V_{CC} to 0.6 V_{CC} (Mid1)
1	1	0.9 V_{CC} to V_{CC} (High)

Table 4. RF AGC Start Point

ATP2	ATP1	ATP0	IFOUT LEVEL (dBμV)
0	0	0	114
0	0	1	112
0	1	0	110
0	1	1	108
1	0	0	106
1	0	1	104
1	1	0	102
1	1	1	Disabled

Table 5. Reference Divider Ratio

RS2	RS1	RS0	REFERENCE DIVIDER RATIO
0	0	0	24
0	0	1	28
0	1	0	32
0	1	1	64
1	0	0	128
1	X	1	80

Table 6. Charge-Pump Current

MODE	CP2	CP1	CP0	CHARGE PUMP CURRENT (μA)
X	0	0	0	70
X	0	0	1	140
X	0	1	0	350
X	0	1	1	600
1	1	0	0	900

Table 7. Test Bits/XTALOUT Control [(1)]

MODE	T3	T2/IFDA	T1/CP2	T0/XLO	DEVICE OPERATION	XTALOUT 4-MHz OUTPUT
0	0	0	0	0	Normal operation	Enabled
0	0	0	0	1	Normal operation	Disabled
1	X	X	X	0	Normal operation	Enabled
1	X	X	X	1	Normal operation	Disabled
0	X	1	X	X	Test mode	Not available
0	1	X	X	X	Test mode	Not available

(1) RFAGC and XTALOUT are not available in test mode.

I^{2}C Read Mode (R/$\overline{W}$ = 1)

Table 8. Read Data Format

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1	A [(1)]
Status byte (SB)	POR	FL	1	1	X	A2	A1	A0	–

(1) A : acknowledge

Table 9. Read Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address set bits (see Table 3)	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag PLL locked (FL = 1), unlocked (FL = 0)	
A[2:0]	Digital data of ADC (see Table 10) Bit P5 must be set to 0.	

Table 10. ADC Level [(1)]

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	0.6 V_{CC} to V_{CC}
0	1	1	0.45 V_{CC} to 0.6 V_{CC}
0	1	0	0.3 V_{CC} to 0.45 V_{CC}
0	0	1	0.15 V_{CC} to 0.3 V_{CC}
0	0	0	0 V to 0.15 V_{CC}

(1) Accuracy is 0.03 × V_{CC}.

Example I²C Data Write Sequences

Telegram examples:

Start-ADB-DB1-DB2-CB1-BB-CB2-Stop
Start-ADB-DB1-DB2-Stop
Start-ADB-CB1-BB-CB2-Stop
Start-ADB-CB1-BB-Stop
Start-ADB-CB2-Stop

Abbreviations:

ADB: Address byte
BB: Band switch byte
CB1: Control byte 1
CB2: Control byte 2
DB1: Divider byte 1
DB2: Divider byte 2
Start: Start condition
Stop: Stop condition

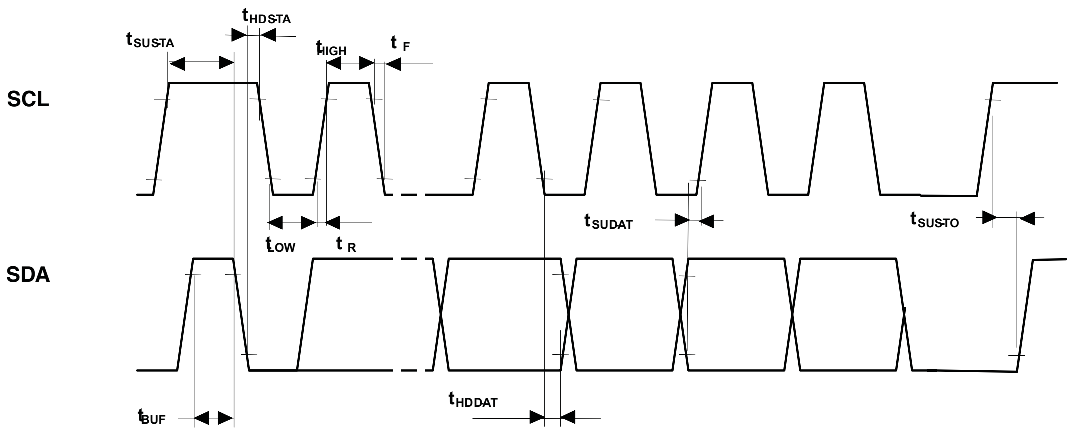
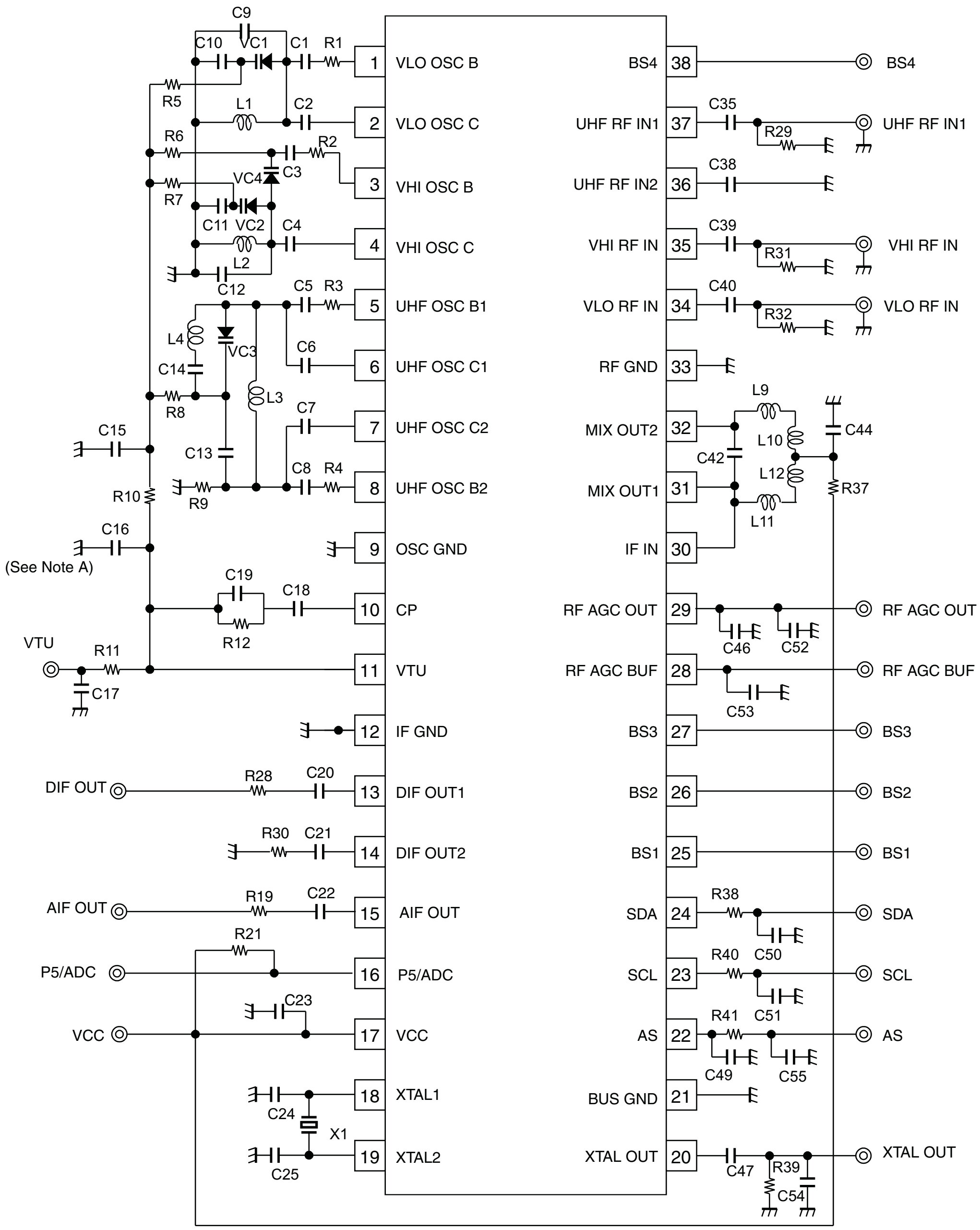


Figure 22. I²C Timing Chart

APPLICATION INFORMATION



A. To prevent abnormal oscillation, connect C16, which does not affect a PLL.

B. This application information is advisory and performance-check is required at actual application circuits. TI assumes no responsibility for the consequences of use of this circuit, such as an infringement of intellectual property rights or other rights, including patents, of third parties.

Figure 23. Reference Measurement Circuit

Component Values for Measurement Circuit(1)

PARTS NAME	VALUE	PARTS NAME	VALUE
C1 (VLO OSC B)	1 pF	L1 (VLO OSC)	Φ3.0 mm, 7T, wire 0.32 mm
C2 (VLO OSC C)	2 pF	L2 (VHI OSC)	Φ2.0 mm, 3T, wire 0.4 mm
C3 (VHI OSC B)	7 pF	L3 (UHF OSC)	Φ1.8 mm, 3T, wire 0.4 mm
C4 (VHI OSC C)	5 pF	L4 (UHF OSC)	Φ1.8 mm, 3T, wire 0.4 mm
C5 (UHF OSCB1)	1.5 pF	L9 (MIX OUT2)	680 nH (LK1608R68K-T)
C6 (UHF OSCC1)	1 pF	L10 (MIX OUT2)	0 Ω
C7 (UHF OSCC2)	1 pF	L11 (MIX OUT1)	680 nH (LK1608R68K-T)
C8 (UHF OSCB2)	1.5 pF	L12 (MIX OUT1)	0 Ω
C9 (VLO OSC)	Open	R1(VLO OSC B)	0
C10(VLO OSC)	39 pF	R2 (VHI OSC B)	12 Ω
C11 (VHI OSC)	51 pF	R3 (UHF OSC B1)	4.7 Ω
C12 (VHI OSC)	0.5 pF	R4 (UHF OSC B2)	0
C13 (UHF OSC)	10 pF	R5 (VLO OSC)	3.3 kΩ
C14 (UHF OSC)	100 pF	R6 (VHI OSC)	3.3 kΩ
C15 (VTU)	2.2 nF/50 V	R7 (VHI OSC)	3.3 kΩ
C16 (CP)	150 pF/50 V	R8 (UHF OSC)	1 kΩ
C17 (VTU)	2.2 nF/50 V	R9 (UHF OSC)	2.2 kΩ
C18(CP)	0.01 u/50 V	R10 (VTU)	3 kΩ
C19(CP)	22 pF/50 V	R11 (VTU)	22 kΩ
C20 (DIF OUT1)	2.2 nF	R12 (CP)	47 kΩ
C21 (DIF OUT2)	2.2 nF	R19 (AIF OUT)	0
C22 (AIF OUT)	2.2 nF	R21 (P5/ADC)	Open
C23 (VCC)	0.1 µF	R28 (DIF OUT1)	200 Ω
C24 (XTAL)	27 pF	R29 (UHF RF IN1)	(50 Ω)
C25 (XTAL)	27 pF	R30 (DIF OUT2)	250 Ω
C35 (UHF RF IN1)	2.2 nF	R31 (VHI RF IN)	(50 Ω)
C38 (UHF RFIN2)	2.2 nF	R32 (VLO RF IN)	(50 Ω)
C39 (VHI RF IN)	2.2 nF	R37 (MIXOUT)	0
C40 (VLO RF IN)	2.2 nF	R38 (SDA)	330 Ω
C42 (MIX OUT)	6.5 pF	R39 (XTAL OUT)	5.1 kΩ
C44 (MIX OUT)	2.2 nF	R40 (SCL)	330 Ω
C46 (RF AGC OUT)	0.1 µF	R41 (AS)	Open
C47 (XTAL OUT)	0.01 µF	VC1 (VLO OSC)	MA2S374
C49 (AS)	22 pF	VC2 (VHI OSC)	MA2S374
C50 (SDA)	Open	VC3 (UHF OSC)	MA2S372
C51 (SCL)	Open	VC4 (VHI OSC)	MA2S372
C52 (RF AGC OUT)	0.047 µF	X1	4-MHz crystal
C53 (RF AGC BUF)	Open		
C54 (XTAL OUT)	10 pF		
C55 (AS)	Open		

(1) If frequency = 44MHz,local frequency range:
VHF-LOW: 101–215 MHz
VHF-HIGH: 221–511 MHz
UHF: 517–908 MHz

APPLICATION INFORMATION (CONTINUED)

Test Circuits

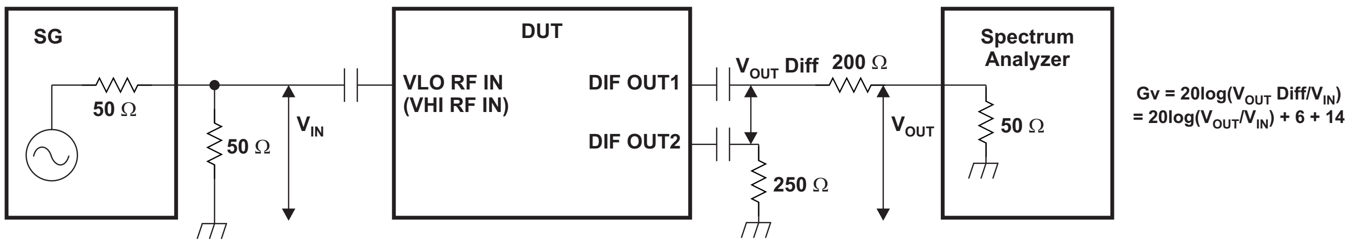


Figure 24. VHF-Conversion Gain-Measurement Circuit (at DIFOUT)

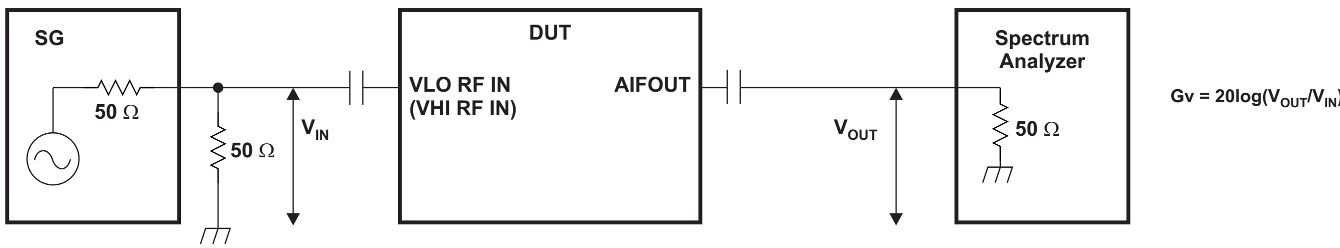


Figure 25. VHF-Conversion Gain Measurement Circuit (at AIFOUT)

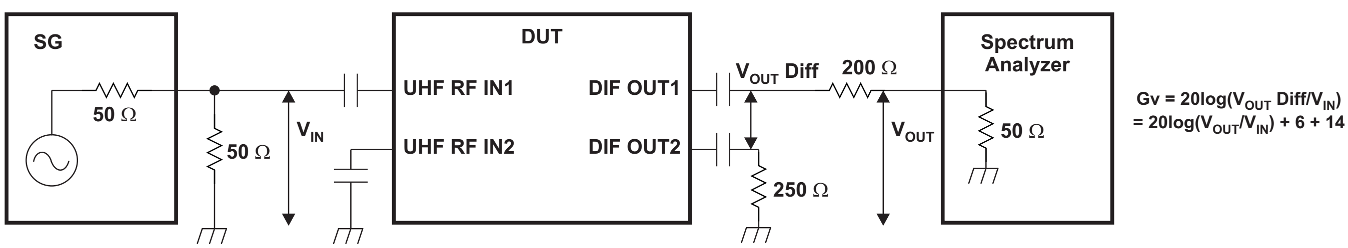


Figure 26. UHF-Conversion Gain-Measurement Circuit (at DIFOUT)

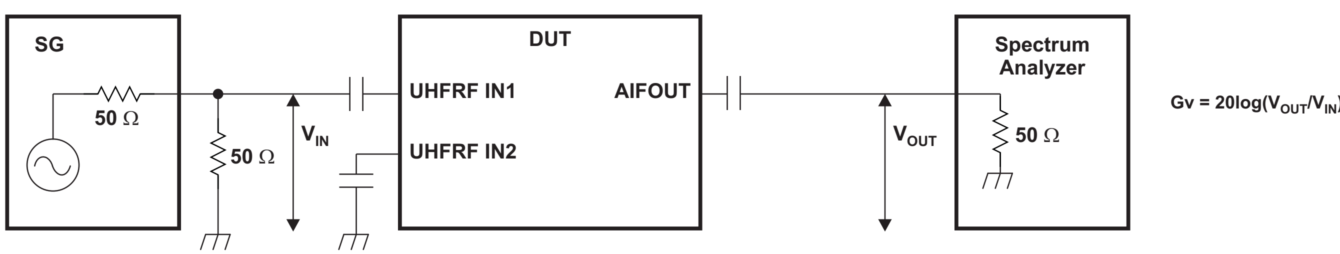


Figure 27. UHF-Conversion Gain Measurement Circuit (at AIFOUT)

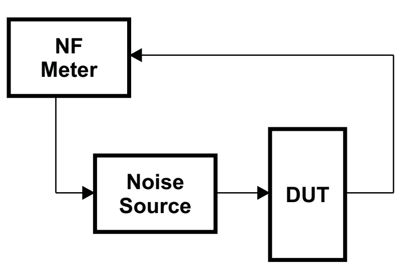


Figure 28. Noise-Figure Measurement Circuit

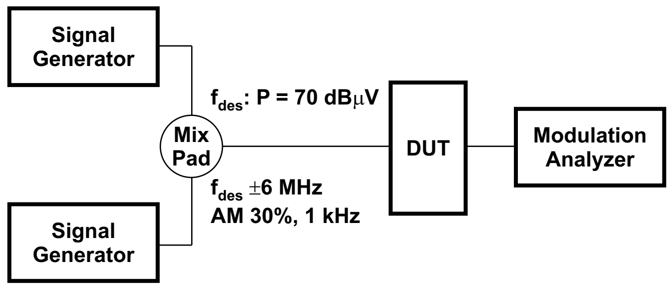


Figure 29. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band Switch Driver Output Voltage (BS1–BS4)

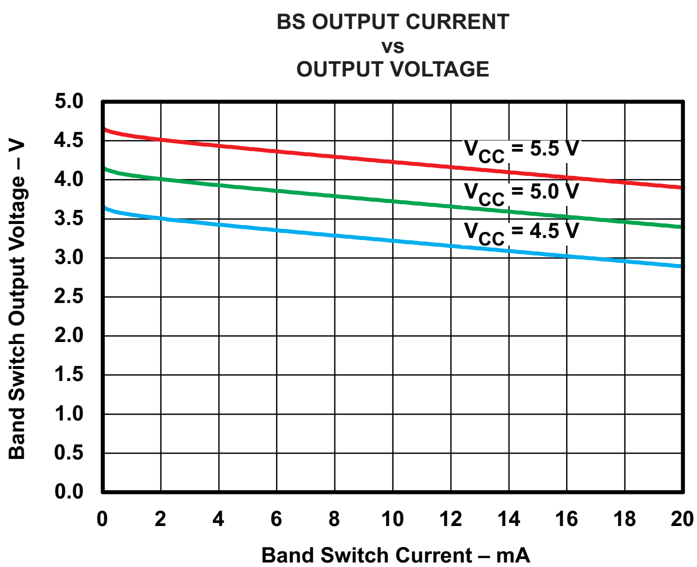


Figure 30. Band Switch Driver Output Voltage

TYPICAL CHARACTERISTICS (continued)

S-Parameter

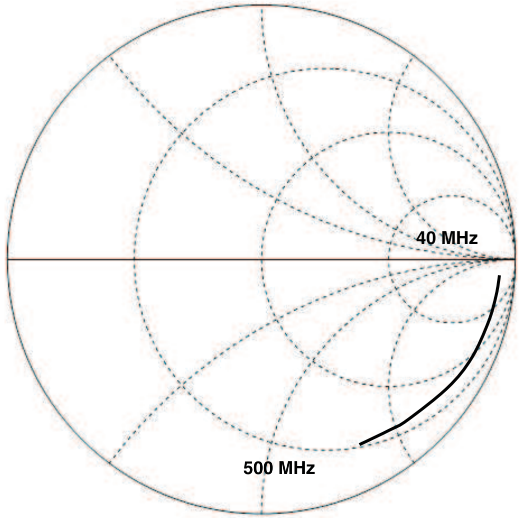


Figure 31. VLO RFIN, VHI RFIN

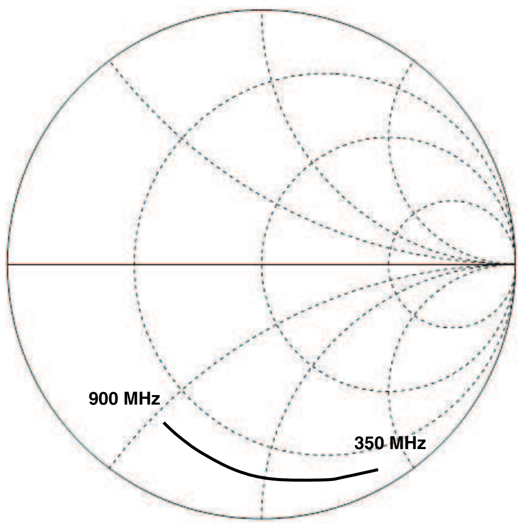


Figure 32. UHF RFIN

TYPICAL CHARACTERISTICS (continued)

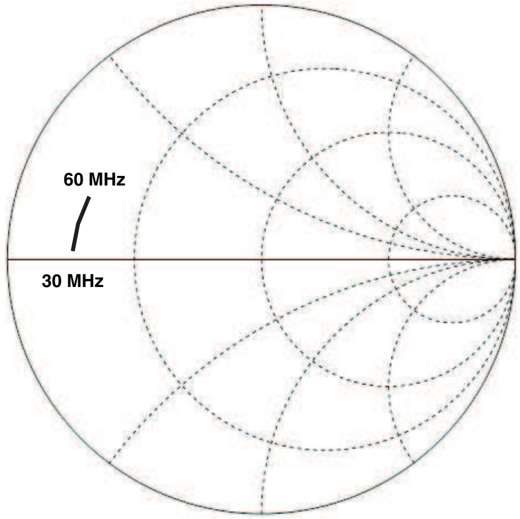


Figure 33. DIFOUT

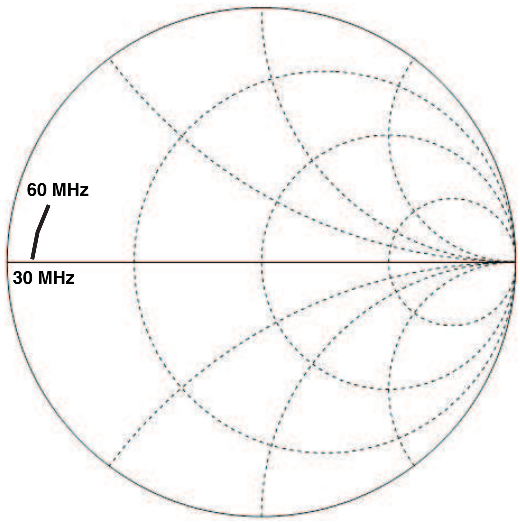
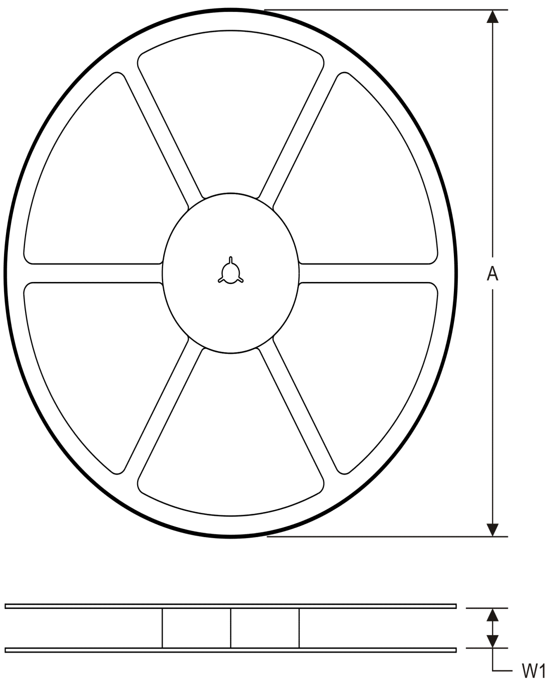


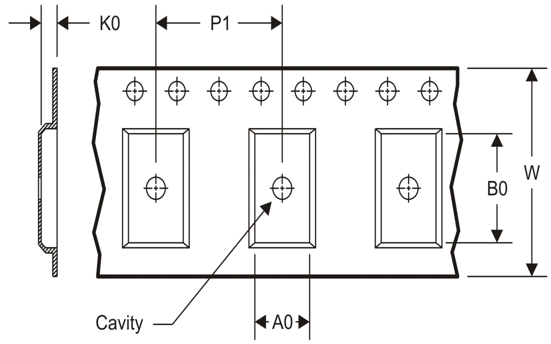
Figure 34. AIFOUT

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



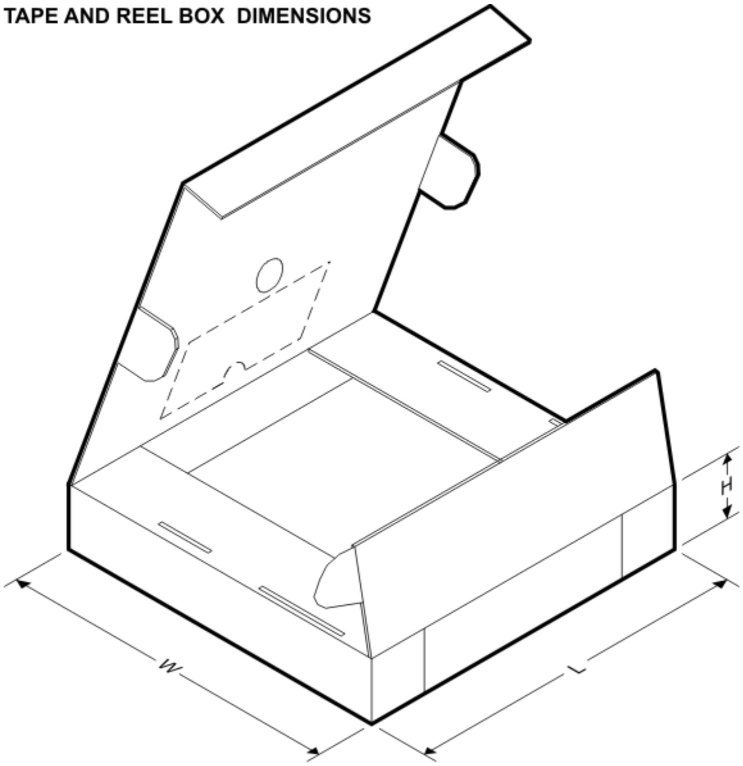
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN761642DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

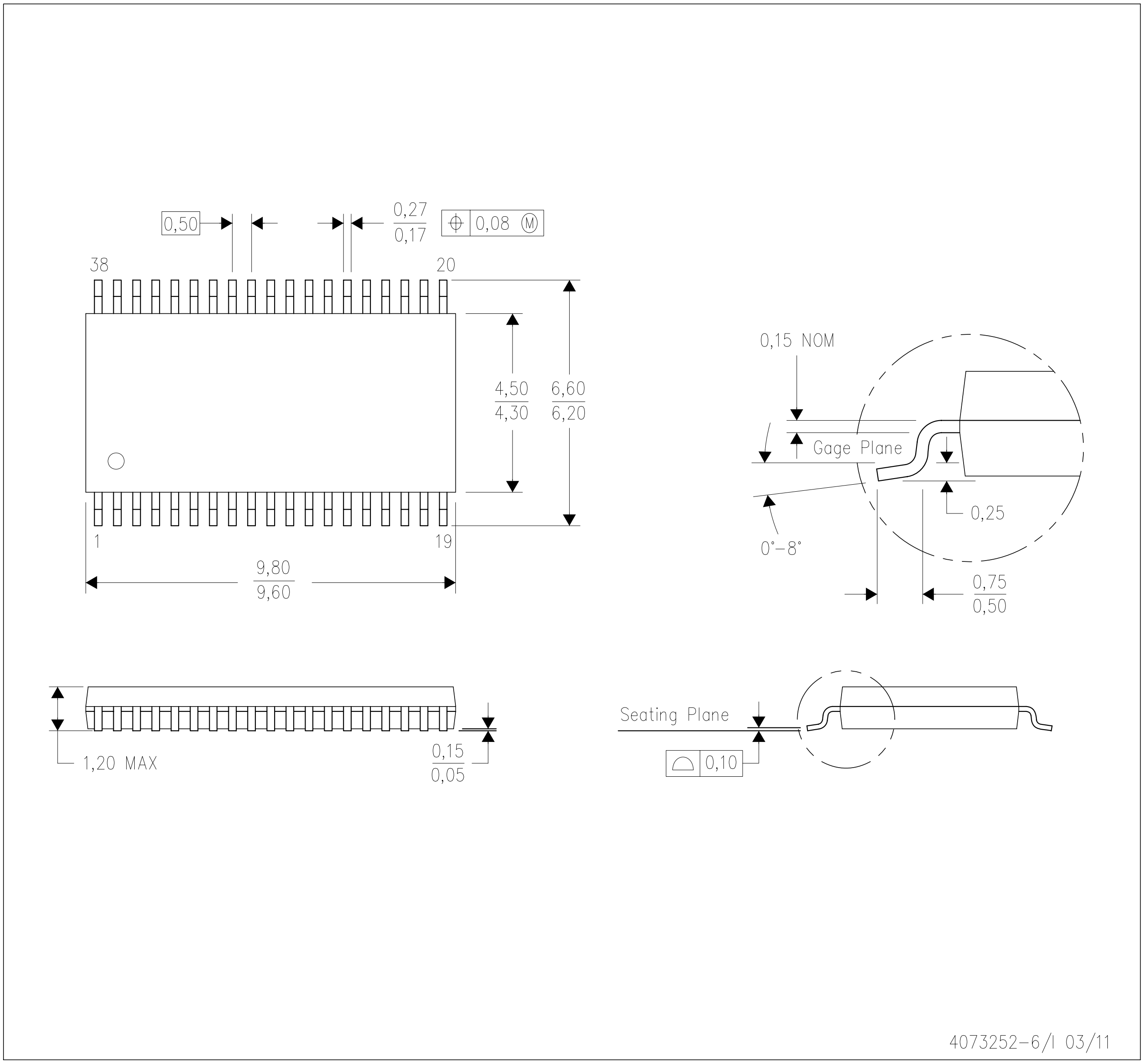
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN761642DBTR	TSSOP	DBT	38	2000	367.0	367.0	38.0

DBT (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.