10-Bit Counter
SN54/74LS491A

74LS491A

Features/Benefits

- **CRT vertical and horizontal timing generation**
- **Bus-structured pinout**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **Low-current PNP inputs reduce loading**

Ordering Information

PART NUMBER	TEMP	PACKAGE	DESCRIPTION
SN54LS491A	Mil	JS,W,L(28)	10.5 MHz Counter
SN74LS491A	Com	NS,JS,NL(28)	25 MHz Counter

Description

The 'LS491/A is a 10-bit up/down counter with set, load and hold capabilities for two LSB, two MSB and six middle bits that are HIGH or LOW as a group. Five control inputs (SET, $\overline{LD}$, $\overline{CNT}$, $\overline{CIN}$ and $\overline{UP}$) provide one of five operations which occur synchronously on the rising edge of the clock (CK).

The SET operation sets the output register (Q9-Q0) to all HIGHs. The LOAD operation loads the inputs (D9-D0) into the register. When COUNT or CARRY IN are not asserted ($\overline{CNT}$ = HIGH or $\overline{CIN}$ = HIGH), the HOLD operation holds the previous value regardless of clock transitions. The COUNT UP operation adds one to the output of the register when the count up input is asserted ($\overline{UP}$ = LOW). The COUNT DOWN operation subtracts one from the output register when the count up input is not asserted ($\overline{UP}$ = HIGH). SET overrides both LOAD and COUNT, LOAD overrides COUNT, and COUNT is conditional on CARRY IN.

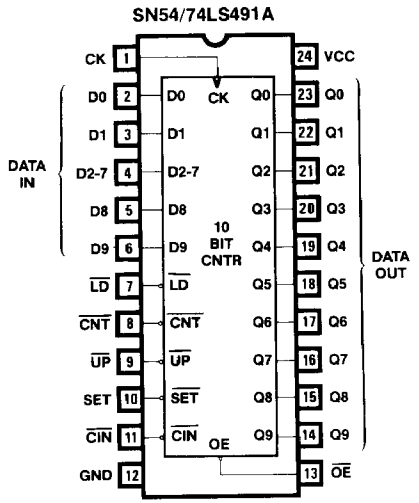
The data output pins are enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The 24-mA I_{OL} outputs are suitable for driving RAM/PROM address lines in video graphics systems.

Function Table

$\overline{OE}$	CK	SET	$\overline{LD}$	$\overline{CNT}$	$\overline{CIN}$	$\overline{UP}$	D9-D0	Q9-Q0	OPERATION
H	*	*	*	*	*	*	*	Z	HI-Z*
L	↑	H	X	X	X	X	X	H	SET all HIGH
L	↑	L	L	X	X	X	D	D	LOAD D
L	↑	L	H	H	X	X	X	Q	HOLD
L	↑	L	H	L	H	X	X	Q	HOLD
L	↑	L	H	L	L	L	X	Q plus 1	COUNT UP
L	↑	L	H	L	L	H	X	Q minus 1	COUNT DN

* When $\overline{OE}$ is HIGH, the three-state outputs are disabled to the high-inpedance states; however, sequential operation of the counter is not affected.

Logic Symbol



SKINNYDIP® and PAL® are registered trademarks of Monolithic Memories.

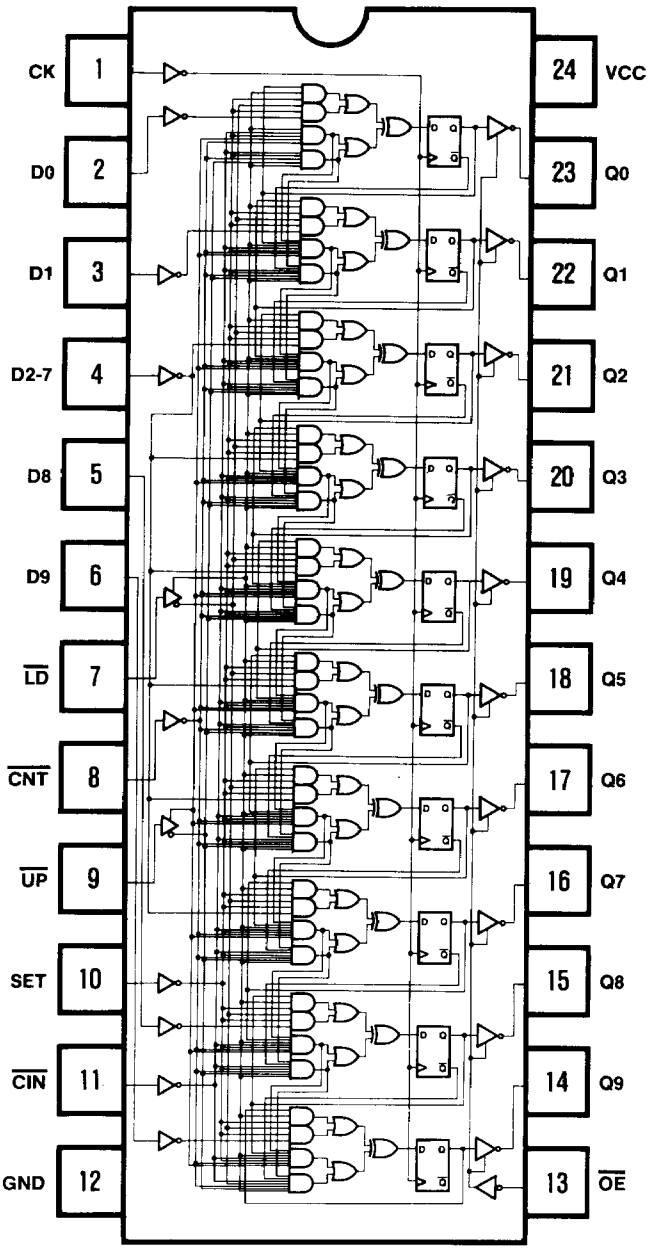
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374

TWX: 910-338-2376

Monolithic Memories MMI

Logic Diagram

10-Bit Up/Down Counter



Absolute Maximum Ratings

Supply voltage V_{CC} ..... 7 V
Input voltage ..... 5.5 V
Off-state output voltage ..... 5.5 V
Storage temperature ..... −65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER		COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_w	Width of clock	High	15	7		ns
		Low	25	15		
t_{su}	Setup time		30	20		ns
t_h	Hold time		0	−15		ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA			−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V			0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			25	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OL} = 24 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, V_{IH} = 2 V	I_{OH} = −3.2 mA	2.4			V
I_{OZL}	Off-state output current	V_{CC} = MAX, V_{IL} = 0.8 V, V_{IH} = 2 V	V_O = 0.4 V			−100	μA
I_{OZH}			V_O = 2.4 V			100	μA
I_{OS}**	Output short-circuit current	V_{CC} = 5 V	V_O = 0 V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX			120	180	mA

* V_{IL} ad V_{IH} parameters are, in effect, input conditions of D.C. and Functional output tests and are not directly tested. V_{IL} is specified at 0.8 V, and V_{IH} is specified at 2.0 V.

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

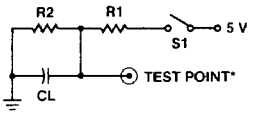
† All typical values are set at V_{CC} = 5 V, T_A = 25°C.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load)	MILITARY MIN	MILITARY TYP†	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP†	COMMERCIAL MAX	UNIT
f_{MAX}	Maximum counting frequency**	Commercial $R_1 = 200\ \Omega$ $R_2 = 390\ \Omega$ Mil $R_1 = 390\ \Omega$ $R_2 = 750\ \Omega$	15.3			25			MHz
t_{CLK}	Clock to Q			10	25		10	15	ns
t_{PZX}	Output enable delay			11	25		11	20	ns
t_{PXZ}	Output disable delay			10	25		10	20	ns

** f_{MAX} is derived from: $1/f_{MAX} [(t_{su} + t_h), t_w (High) + t_w (Low), t_{CLK}]$.

Test Load

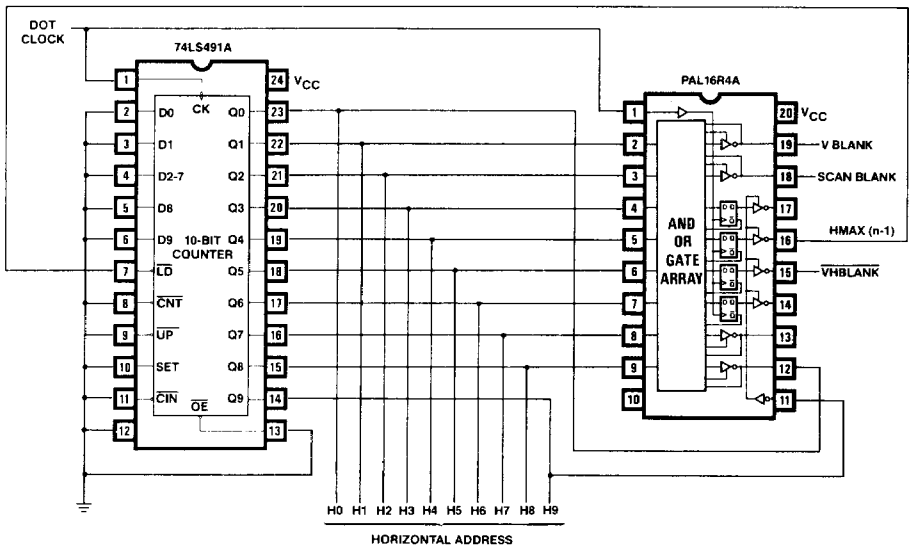


* The "Test Point" is driven by the outputs under test, and observed by instrumentation

Notes: 1. t_{PD} is tested with switch S_1 closed, C_L = 50 pF and measured at 1.5 V output level.
2. t_{PZX} is measured at the 1.5 V output level with C_L = 50 pF. S_1 is open for high impedance to "1" test, and closed for high impedance to "0" test.
3. t_{PXZ} is tested with C_L = 5 pF. S_1 is open for "1" to high impedance test, measured at V_{OH} −0.5 V output level. S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5 V output level.

Application

Video Horizontal Timing and Blanking



Timing Analysis:

Path 1 — Outputs of 74LS491A setting up at PAL16R4A inputs

$$t_{PD_{CK\text{-}Q/74LS491A}} + t_{SU_{PAL16R4A}} = 15\text{ ns} + 25\text{ ns} = 40\text{ ns}$$

Path 2 — Outputs of PAL16R4A setting up at 74LS491A inputs

$$t_{PD_{CK\text{-}Q/PAL16A}} + t_{SU_{74LS491A}} = 25\text{ ns} + 30\text{ ns} = 55\text{ ns}$$

Accordingly, the worst-case timing of the two paths is 55-ns, which results in a maximum video dot clock frequency of 18.18 MHz. Strict interpretation of the 60 Hz field rate NTSC Standard suggests that up to 52.1 μsec of time is available for active-raster-line duration. In practice however, most CRT monitors overscan the screen to correct horizontal sweep nonlinearities. As a consequence, the horizontal blanking time is increased, and the active video time decreased, typically to about 40 μsec. For the application circuit shown above, over 512 dots (pixels) for one line can be displayed:

$$\frac{40\ \mu\text{sec per line}}{55\text{ ns per pixel per line}} = 727\text{ pixels}$$

Normally, at least a 10-bit counter is required to provide a video timing chain for such resolutions. The 74LS491A combined with a high-speed PAL® (PAL16R4A) is capable of generating a complete set of video timing signals. Note that in the application circuit, the maximum horizontal count [H MAX (n-1)] is decoded one clock early, due to the 1-level pipelining used to obtain circuit speed.