

## SN65LVPE801 8.0 Gbps SATA Express Equalizer and Redriver

### 1 Features

- SATA Express Support
- Selectable Equalization and De-Emphasis
- Hot Plug Capable
- Receiver Detect and OOB Support
- Multirate Operation
  - SATA: 1.5 Gbps, 3.0 Gbps, 6.0 Gbps
  - PCIe: 2.5 Gbps, 5.0 Gbps, 8.0 Gbps
- Suitable to Receive 8.0 Gbps Data Over Up to 40 Inches (1.0 Meter) of FR4 PC Board
- Compensates Up to 14-dB Loss on the Receive Side and 1.2dB Loss on the Transmit Side at 3 GHz
- Integrated Output Squelch
- Auto Low Power Feature Lowers Power by > 90%
  - < 100 mW (Active Mode, typical)
  - < 11 mW (Auto Low Power Mode, typical)
- Single 3.3-V Supply
- High Protection Against ESD Transient
  - HBM: 6 kV
  - CDM: 1.5 kV
- Ultra Small Footprint, 2.00 mm x 2.00 mm QFN Package

### 2 Applications

- Notebooks
- Desktops
- Docking Stations
- Servers
- Workstations

### 3 Description

The SN65LVPE801 is a versatile single channel, SATA Express signal conditioner supporting data rates up to 8.0 Gbps. The device supports SATA Gen 1, 2, and 3 specifications as well as PCIe 1.0, 2.0, 3.0. The SN65LVPE801 operates from a single 3.3 V supply and has 100  $\Omega$  line termination with self-biasing feature, making the device suitable for AC coupling. The inputs incorporate an out-of-band (OOB) detector, which automatically squelches the output when the input differential voltage falls below threshold while maintaining a stable common-mode voltage. The device is also designed to handle spread spectrum clocking (SSC) transmission per SATA standard.

The SN65LVPE801 handles interconnect losses at its input with selectable equalization settings that can be programmed to match the loss in the channel. For data rates of 3 Gbps and lower the SN65LVPE801 equalizes signals for a span of up to 50 inches of FR4 board material. For data rates of 8 Gbps the device compensates up to 40 in of FR4 material. The equalization level is controlled by the setting of the signal control pin EQ.

Two de-emphasis levels can be selected on the transmit side to provide 0 or 1.2dB of additional high-frequency loss compensation at the output.

The device is hot-plug capable<sup>(1)</sup> preventing device damage under device *hot*-insertion such as async signal plug/removal, unpowered plug/removal, powered plug/removal, or surprise plug/removal.

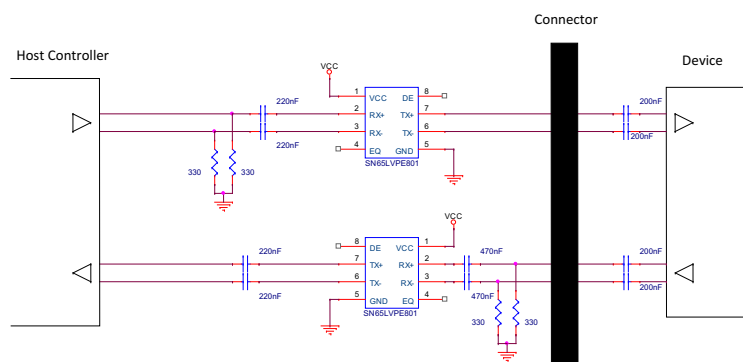
(1) Requires use of AC coupling capacitors at differential inputs and outputs.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVPE801	WSO8 (8)	2.00mm x 2.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 SATA Express Reference Schematic



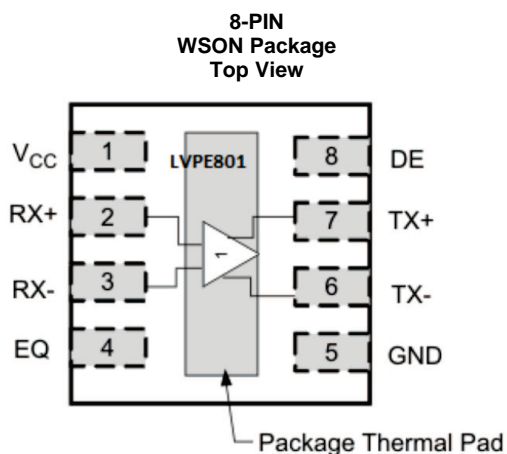
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## 5 Revision History

DATE	REVISION	NOTES
January 2015	*	Initial release.

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O TYPE	DESCRIPTION
NO.	NAME		
HIGH SPEED DIFFERENTIAL I/O			
2	RX+	I, CML	Non-inverting and inverting CML differential inputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
3	RX−	I, CML	
7	TX+	O, VML	Non-inverting and inverting VML differential outputs. These pins are tied to an internal voltage bias by dual termination resistor circuit.
6	TX−	O, VML	
CONTROL PINS			
4	EQ	I, LVCMOS	Selects equalization settings per <a href="#">Table 1</a> . Internally tied to GND.
8	DE	I, LVCMOS	Selects de-emphasis settings per <a href="#">Table 1</a> . Internally tied to GND.
POWER			
1	V <sub>CC</sub>	Power	Positive supply should be 3.3 V ±10%
5	GND	Power	Supply ground

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range <sup>(2)</sup>	V <sub>CC</sub>	–0.5	4	V
Voltage range	Differential I/O	–0.5	4	V
	Control I/O	–0.5	V <sub>CC</sub> + 0.5	V

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground pin.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±6000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

typical values for all parameters are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C; all temperature limits are specified by design

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3	3.3	3.6	V
	Coupling capacitor	See <a href="#">Applications and Implementation</a>			nF
T <sub>A</sub>	Operating free-air temperature	0		85	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65LVPE801	UNIT
		DRF (8 PINS)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	97.8	°C/W
R <sub>θJCTop</sub>	Junction-to-case (top) thermal resistance	81.9	
R <sub>θJB</sub>	Junction-to-board thermal resistance	65.6	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.3	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	65.6	
R <sub>θJCbott</sub>	Junction-to-case (bottom) thermal resistance	19.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS						
ICC <sub>Max-s</sub>	Active mode supply current	EQ/DE = NC, K28.5 pattern at 8 Gbps, V <sub>ID</sub> = 700 mV <sub>pp</sub>	29	40		mA
I <sub>CCPS</sub>	Auto power save mode I <sub>CC</sub>	When auto low power conditions are met	3.3	5.9		mA
	Maximum data rate			8.0		Gbps
OOB						
V <sub>OOB</sub>	Input OOB threshold	F = 750 MHz	50	70	90	mV <sub>pp</sub>
D <sub>VdiffOOB</sub>	OOB differential delta			25		mV
D <sub>VCMOOB</sub>	OOB common-mode delta			50		mV
CONTROL LOGIC						
V <sub>IH</sub>	High-level input voltage	For all control pins	1.4			V
V <sub>IL</sub>	Low-level input voltage			0.5		V
VIN <sub>HYS</sub>	Input hysteresis		115			mV
I <sub>IH</sub>	High-level input current	V <sub>IH</sub> = V <sub>CC</sub> (DE/EQ)		20		μA
I <sub>IL</sub>	Low-level input current	V <sub>IL</sub> = 0V (DE/EQ)	10			μA
RECEIVER AC/DC						
Z <sub>DIFFRX</sub>	Differential input impedance		85	100	115	Ω
Z <sub>SERX</sub>	Single-ended input impedance		40			Ω
V <sub>CMRX</sub>	Common-mode voltage			1.7		V
RL <sub>DiffRX</sub>	Differential mode return loss (RL)	f = 150 MHz – 300 MHz	20	26		dB
		f = 300 MHz – 600 MHz	18	22		
		f = 600 MHz – 1.2 GHz	14	17		
		f = 1.2 GHz – 2.4 GHz	10	12		
		f = 2.4 GHz – 3.0 GHz	8	12		
		f = 3.0 GHz – 5.0 GHz	6	11		
RX <sub>DiffRLSlope</sub>	Differential mode RL slope	f = 300 MHz – 6.0 GHz (see <a href="#">Figure 1</a> )		–13		dB/dec
RL <sub>CMRX</sub>	Common-mode return loss	f = 150 MHz – 300 MHz	8	9		dB
		f = 300 MHz – 600 MHz	14	17		
		f = 600 MHz – 1.2 GHz	12	18		
		f = 1.2 GHz – 2.4 GHz	8	10		
		f = 2.4 GHz – 3.0 GHz	6	8		
		f = 3.0 GHz – 5.0 GHz	6	8.5		
V <sub>diffRX</sub>	Differential input voltage PP	f = 1.5 GHz and 3.0 GHz	120		1600	mV/ppd
IB <sub>RX</sub>	Impedance balance	f = 150 MHz – 300 MHz	30	41		dB
		f = 300 MHz – 600 MHz	34	41		
		f = 600 MHz – 1.2 GHz	24	33		
		f = 1.2 GHz – 2.4 GHz	14	24		
		f = 2.4 GHz – 3.0 GHz	12	26		
		f = 3.0 GHz – 5.0 GHz	6	18		
		f = 5.0 GHz – 6.5 GHz	5	18		
TRANSMITTER AC/DC						
Z <sub>diffTX</sub>	Pair differential impedance		85	100	122	Ω
Z <sub>SETX</sub>	Single-ended input impedance		40			Ω
V <sub>TXtrans</sub>	Sequencing transient voltage	Transient voltages on the serial data bus during power sequencing (lab load)	–1.2	0.3	1.2	V

## Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RL <sub>DiffTX</sub> Differential mode return loss	f = 150 MHz – 300 MHz	14	22		dB
	f = 300 MHz – 600 MHz	12	21		
	f = 600 MHz – 1.2 GHz	11	18		
	f = 1.2 GHz – 2.4 GHz	10	14		
	f = 2.4 GHz – 3.0 GHz	10	14		
	f = 3.0 GHz – 5.0 GHz	8	14		
TX <sub>DiffRLSlope</sub> Differential mode RL slope	f = 300 MHz – 3.0 GHz (see Figure 1)		–13		dB/dec
RL <sub>CMTX</sub> Common-mode return loss	f = 150 MHz – 300 MHz	10	20		dB
	f = 300 MHz – 600 MHz	9	16		
	f = 600 MHz – 1.2 GHz	8	13.5		
	f = 1.2 GHz – 2.4 GHz	6	8.5		
	f = 2.4 GHz – 3.0 GHz	5	8		
	f = 3.0 GHz – 5.0 GHz	4	7		
IB <sub>TX</sub> Impedance balance	f = 150 MHz – 300 MHz	34	38		dB
	f = 300 MHz – 600 MHz	32	38		
	f = 600 MHz – 1.2 GHz	24	33		
	f = 1.2 GHz – 2.4 GHz	18	25		
	f = 2.4 GHz – 3.0 GHz	18	25		
	f = 3.0 GHz – 5.0 GHz	12	21		
	f = 5.0 GHz – 6.5 GHz	8	21		
Diff <sub>VppTX</sub> Differential output voltage swing	f = 3.0 GHz (under no interconnect loss)	400	650	900	mV/ppd
VCM <sub>AC_TX</sub> TX AC CM voltage	At 1.5 GHz		15	50	mVppd
	At 3.0 GHz		10	26	dBmv (rms)
	At 6.0 GHz		12	30	
VCM <sub>TX</sub> Common-mode voltage			1.70		V

## 7.6 Timing Requirements

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DEVICE PARAMETERS</b>					
t <sub>PDelay</sub> Propagation delay	Measured using K28.5 pattern, See Figure 3		275	350	ps
AutoLP <sub>ENTRY</sub> Auto low power entry time	Electrical idle at input, See Figure 8		11		μs
AutoLP <sub>EXIT</sub> Auto low power exit time	After first signal activity, See Figure 8		33	50	ns
<b>OOB</b>					
t <sub>OOB1</sub> OOB mode enter	See Figure 7		1	5	ns
t <sub>OOB2</sub> OOB mode exit	See Figure 7		1	5	ns
<b>RECEIVER AC/DC</b>					
t <sub>20-80RX</sub> Rise/fall time	Rise times and fall times measured between 20% and 80% of the signal. 8 Gbps speed measured 1" from device pin	62		75	ps
t <sub>skewRX</sub> Differential skew	Difference between the single-ended mid-point of the RX+ signal rising/falling edge, and the single-ended mid-point of the RX– signal falling/rising edge			30	ps
<b>TRANSMITTER AC/DC</b>					
t <sub>20-80TX</sub> Rise/Fall time	Rise times and fall times measured between 20% and 80% of the signal. At 8 Gbps under no load conditions measured at the pin	44	58	85	ps

## Timing Requirements (continued)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{skewTX}}$	Differential skew	Difference between the single-ended mid-point of the TX+ signal rising/falling edge, and the single-ended mid-point of the TX– signal falling/rising edge, D1, D0 = $V_{CC}$		2	15	ps
$t_{\text{xR/Fimb}}$	TX rise/fall imbalance	At 3 Gbps		6%	20%	
$t_{\text{xAmplmb}}$	TX amplitude imbalance			1%	10%	

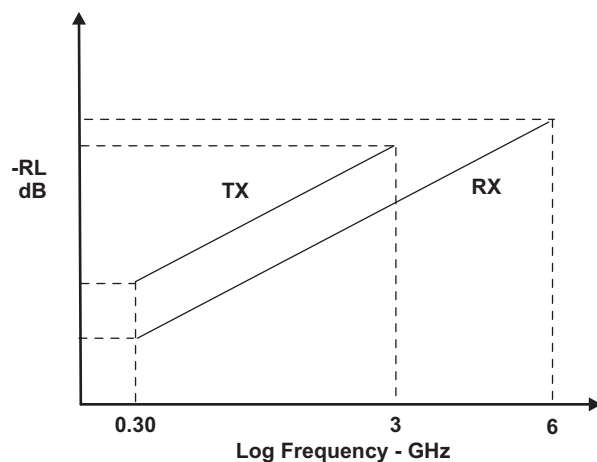


Figure 1. TX, RX Differential Return Loss Limits

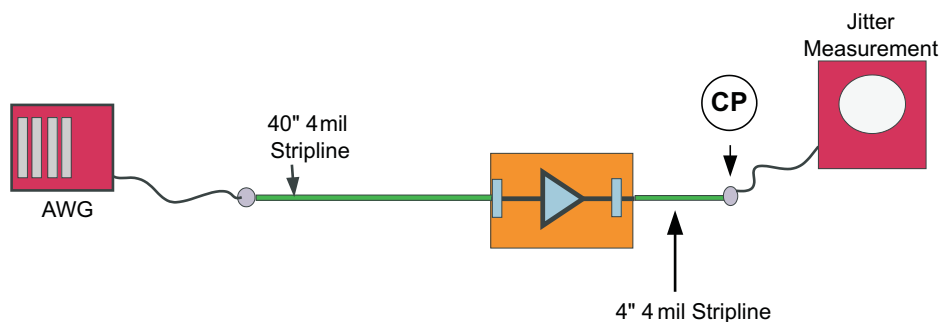


Figure 2. Jitter Measurement Test Condition

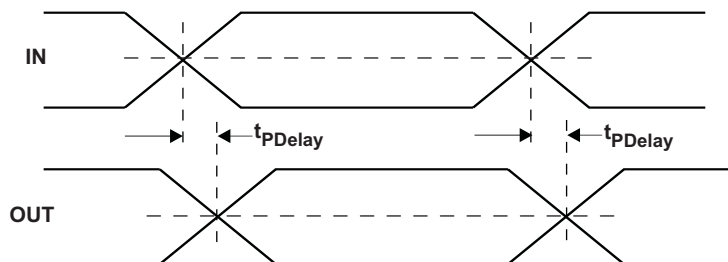
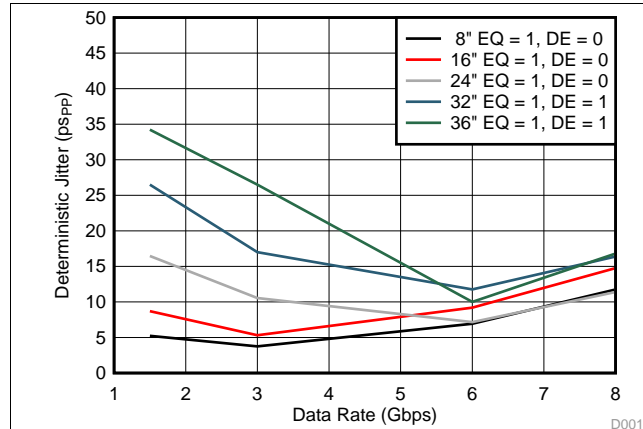


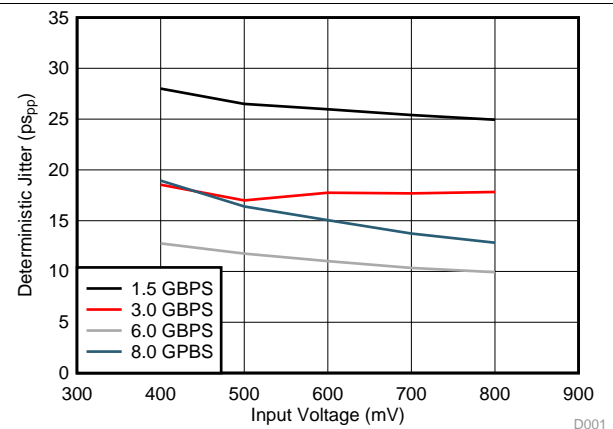
Figure 3. Propagation Delay Timing Diagram

## 7.7 Typical Characteristics



A function of input trace length of 4 mil FR-4

**Figure 4. Deterministic Jitter vs Data Rate**



Function of data rate after equalizing for 32\"

**Figure 5. Deterministic Jitter vs Launch Amplitude**

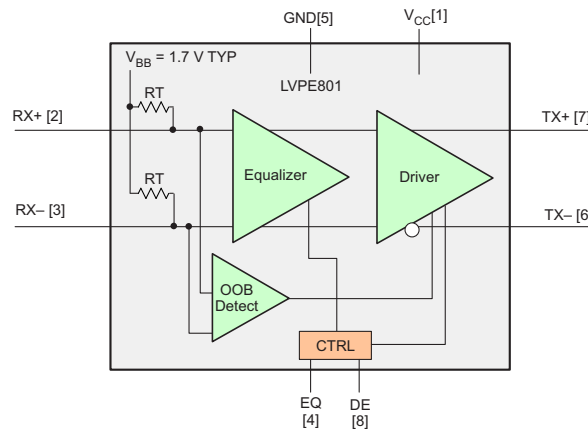


## 8 Detailed Description

### 8.1 Overview

The SN65LVPE801 is a single channel equalizer and redriver. The device operates over a wide range of signaling rates, supporting operation from DC to 8 Gbps. The wide operating range supports SATA Gen 1,2,3 (1.5 Gbps, 3.0 Gbps, and 6.0 Gbps respectively) as well as PCI Express 1.0, 2.0, 3.0 (2.5 Gbps, 5.0 Gbps, and 8.0 Gbps). The device also supports SATA Express (SATA 3.2) which is a form factor specification that allows for SATA and PCI Express signaling over a single connector.

### 8.2 Functional Block Diagram



**Figure 6. Data Flow Block Diagram**

### 8.3 Feature Description

#### 8.3.1 SATA Express

SATA Express (sometimes SATAe) is an electro-mechanical standard that supports both SATA and PCI Express storage devices. SATAe is standardized in the SATA 3.2 standard. The standard is concerned with providing a smooth transition from SATA to PCIe storage devices. The standard provides for standardized cables and connectors, and muxes the PCIe and SATA lanes at the host side so that either SATA compliant or PCIe compliant devices may operate with a host.

SATAe provides support for SATA1, SATA2 and SATA3 devices (operating from 1.5 Gbps to 6.0 Gbps), as well as PCIe1, PCIe2 and PCIe3 devices (operating from 2.5 Gbps to 8.0 Gbps).

The SN65LVPE801 provides for equalization and re-drive of a single channel input signal complying with any of the SATA or PCIe standards available with SATAe.

The SATAe standard provides for a mechanism for a host to recognize and detect whether a SATA or PCIe device is plugged into the host. See the [Typical SATA Applications](#) section for the details of the SATA Express Interface Detect operation.

#### 8.3.2 Receiver Termination

The receiver has integrated terminations to an internal bias voltage. The receiver differential input impedance is nominally 100  $\Omega$ , with a  $\pm 15\%$  variation.

#### 8.3.3 Receiver Internal Bias

The SN65LVPE801 receiver is internally biased to 1.7 V, providing support for AC coupled inputs.

## Feature Description (continued)

### 8.3.4 Receiver Equalization

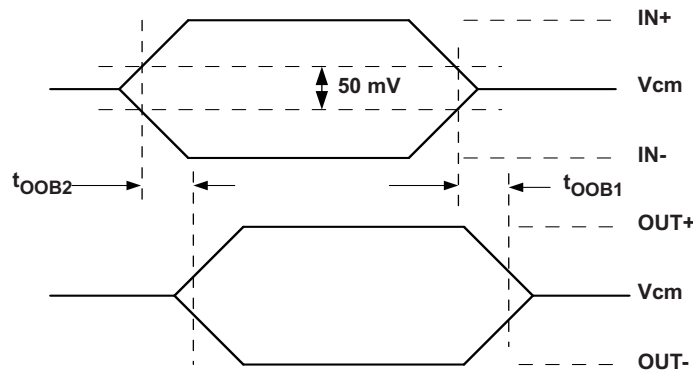
The SN65LVPE801 incorporates programmable equalization. The EQ input controls the level of equalization that is used to open the eye of the received input signal. If the EQ input is left open, or pulled LO, 7 dB (at 3 GHz) of equalization is applied. When the EQ input is HIGH, the equalization is set to 14 dB (again at 3 GHz). [Table 1](#) shows the equalization values discussed.

**Table 1. EQ and DE Settings**

EQ	EQUALIZATION dB (at 6 Gbps)	DE	DE-EMPHASIS db (at 6 Gbps)
0 (default)	7	0 (default)	0
1	14	1	-1.2

### 8.3.5 OOB/Squelch

The SN65LVPE801 receiver incorporates an Out-Of-Band (OOB) detection circuit in addition to the main signal chain receiver. The OOB detector continuously monitors the differential input signal to the device. The OOB detector has a 50-mVpp entry threshold. If the differential signal at the receiver input is less than the OOB entry threshold, the device transmitter transitions to squelch. The SN65LVPE801 will enter squelch within 5 ns of the input signal falling below the OOB entry threshold. The SN65LVPE801 continues to monitor the input signal while in squelch. While in squelch, if the OOB detector determines that the input signal now exceeds the 90 mVpp exit threshold, the SN65LVPE801 will exit squelch within 5 ns. See [Figure 7](#).

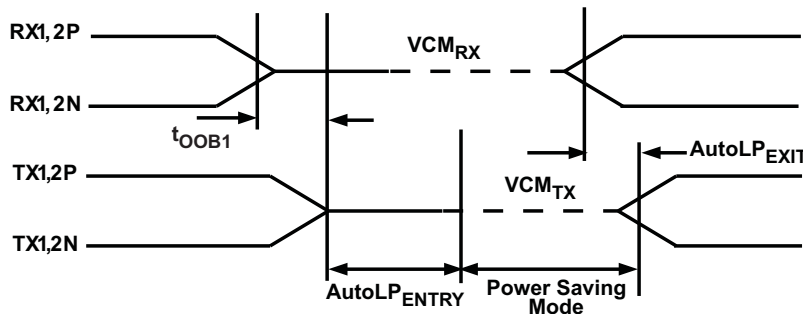


**Figure 7. OOB Enter and Exit Timing  
Receiver Input Termination is Disabled**

When the SN65LVPE801 enters squelch state the transmitter output is squelched. The transmitter non-inverting (TX+) output and the transmitter inverting output (TX-) are both driven to the transmitter nominal common mode voltage which is 1.7 V.

### 8.3.6 Auto Low Power

The SN65LVPE801 also includes an Auto Low Power Mode (ALP). ALP is entered when the differential input signal has been less than 50 mV for > 10  $\mu$ s. The device enters and exits Low Power Mode by actively monitoring the input signal level. In this state the device selectively shuts off internal circuitry to lower power by > 90% of its normal operating power. While in ALP mode the device continues to actively monitor input signal levels. When the input signal exceeds the OOB exit threshold level, the device reverts to the active state. Exit time from Auto Low Power Mode is < 50 ns (max). See [Figure 8](#).



**Figure 8. Auto Low Power Mode Entry and Exit Timing**

### 8.3.7 Transmitter Output Signal

The SN65LVPE801 differential output signal is 650 mVpp when de-emphasis is disabled (DE input is open or pulled low).

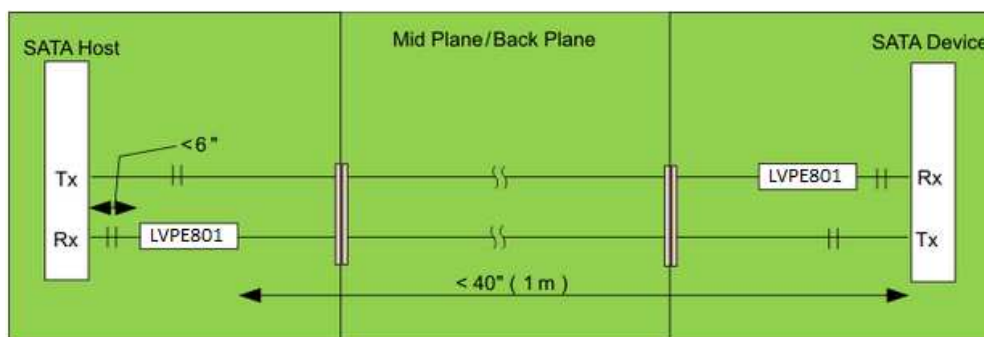
### 8.3.8 Transmitter Common Mode

The SN65LVPE801 transmitter common mode output is set to 1.7 V.

### 8.3.9 De-Emphasis

The SN65LVPE801 transmitter incorporates programmable de-emphasis to provide signal conditioning to offset the anticipated channel losses based on expected use cases for the device. Figure 10 shows an example of a SATA host communicating with a SATA device through a backplane. In such a use case, an SN65LVPE801 would be located at the end of the interconnect channels (i.e. at the device end for the host TX channel, and at the host end for the host RX channel). These locations are selected based on the signal conditioning that is incorporated into the SN65LVPE801. The SN65LVPE801 provides up to 14 dB of equalization, while supporting up to 1.2 dB of de-emphasis. The optimum location would therefore be at the end of the interconnect, allowing the receiver equalization to address the majority of the channel loss, while the de-emphasis would be employed to overcome the much shorter interconnect length.

The DE input controls the amount of de-emphasis that is applied at the transmitter output. The de-emphasis selections are shown in Table 1. When DE is left open, or pulled low, de-emphasis shall be off. When DE is pulled HIGH, 1.2 dB of de-emphasis is used at the transmitter output.



**Note:**

Trace lengths are suggested values based on TI HSPICE simulations (done over programmable limits of input EQ) to meet SATA loss and jitter spec.

Actual trace length supported by the LVPE801 may be more or less than suggested values and will depend on board layout, trace widths and number of connectors used in the high speed signal path.

**Figure 9. Trace Length Example**

### 8.3.10 Transmitter Termination

The SN65LVPE801 transmitter includes integrated terminations. The receiver differential output impedance is nominally 100  $\Omega$ , with a  $\leq 22\%$  variation.

## 8.4 Device Functional Modes

### 8.4.1 Active

Active mode is the normal operating mode. When power is applied to the device, and the differential input signal to the receiver is greater than 90 mV<sub>pp</sub>, the device is in active mode and meets all the specifications in the data sheet.

### 8.4.2 Squelch

When the device is powered, and the differential input signal to the receiver is less than 50 mV<sub>pp</sub>, the device is in squelch mode. In squelch mode the transmitter outputs are both set to VCM<sub>TX</sub> or 1.7 V.

### 8.4.3 Auto Low Power

When the device is powered and the differential input signal to the receiver has been less than 50 mV<sub>pp</sub> for greater than 10 ns, the device transitions to Auto Low Power (ALP) mode. In ALP, the transmitter outputs are both set to VCM<sub>TX</sub>. In addition, while in ALP, the device shuts off internal circuitry to lower power to less than 10% of the power in the Active mode.

## 9 Applications and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

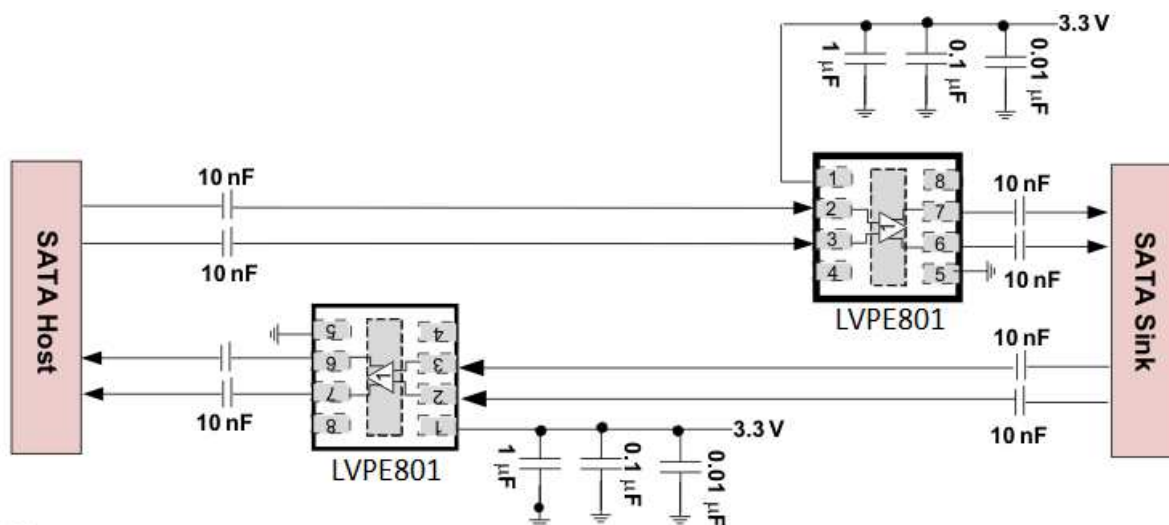
### 9.1 Application Information

The SN65LVPE801 can be used for SATA applications as well as SATA Express applications. The device supports SATA Gen1, Gen2, and Gen3 applications with data rates from 1.5 to 6 Gbps. The built-in equalization circuits provide up to 14 dB of equalization at 3 GHz. This equalization can support SATA GEN2 (3 Gbps) applications over up to 50 inches of FR-4 material. The same 14 dB equalizer is suited to SATA Gen3 (6 Gbps) applications up to 40 inches of FR4.

In addition to SATA applications, the SN65LVPE801 can support SATA Express applications. SATA Express provides a standardized interface to support both SATA (Gen1, Gen2, and Gen3) and PCI Express (PCIe 1.0, 2.0 and 3.0).

All applications of the SN65LVPE801 share some common applications issues. For example, power supply filtering, board layout, and equalization performance with varying interconnect losses. Other applications issues are specific, such as implementing receiver detection for SATA Express applications. The Typical Application examples demonstrate common implementations of the SN65LVPE801 supporting SATA, as well as SATA Express applications.

### 9.2 Typical SATA Applications



#### Note:

- 1) Place supply caps close to device pin
- 2) EQ and DE selection at 7 dB and 0dB respectively
- 3) Actual EQ /DE settings will depend on device placement relative to host and SATA connector

**Figure 10. Typical Device Implementation**

## Typical SATA Applications (continued)

### 9.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
SATA Signaling Rate	1.5 - 6.0 Gbps
AC Coupling Capacitance	10 nF
Interconnect Characteristic Impedance	100 Ohms
Interconnect Length	Up to 50" FR4 for SATA Gen2 Up to 40" FR4 for SATA Gen3
Termination Resistance	100 Ohms differential integrated into TX and RX

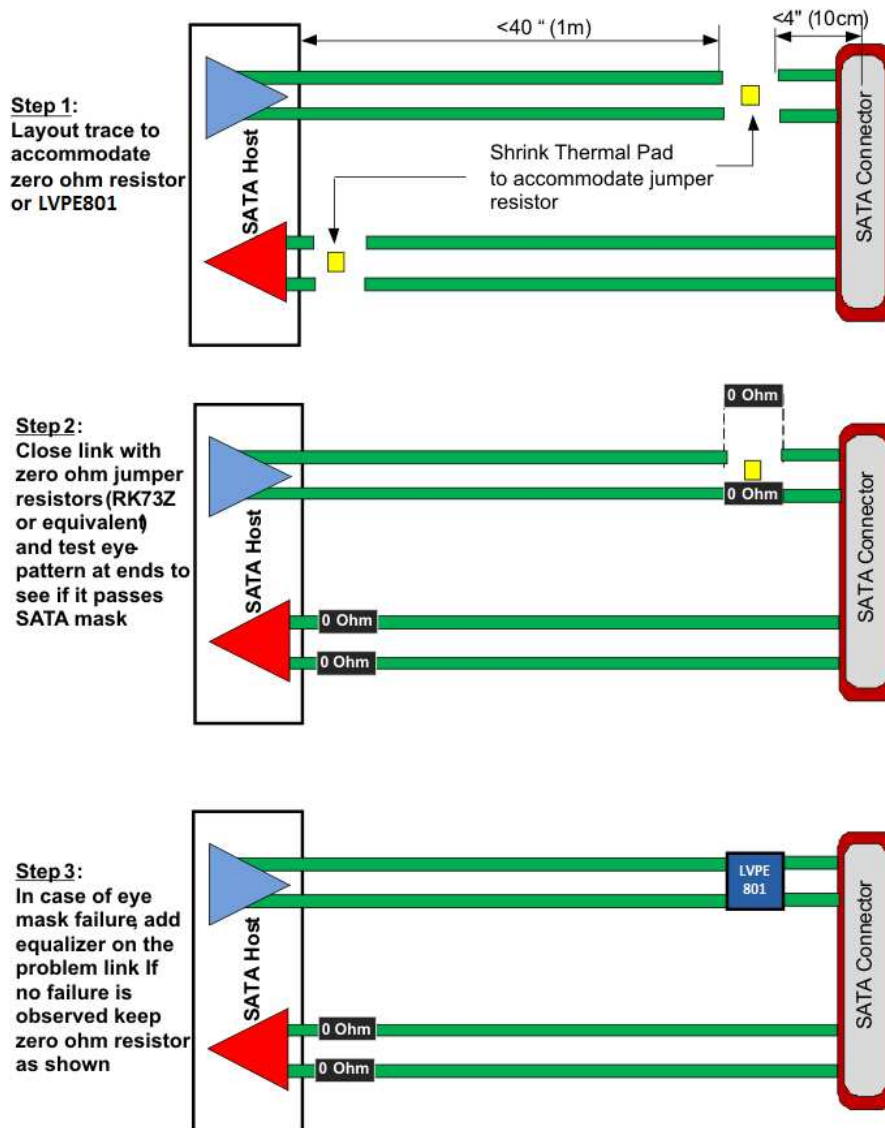
### 9.2.2 Detailed Design Procedure

**Figure 10** shows a typical SATA Application. The SATA host, which may be a notebook or desktop, communicates with a SATA sink, which could be a SSD mass storage device. The SATA host and sink communicate over a backplane differential pair, or a SATA cable. When using the SN65LVPE801 as an equalizer/redriver, the designer would optimally place the SN65LVPE801 close to the end of the interconnect. The SN65LVPE801 provides up to 14 dB of equalization, and up to 1.2 dB of de-emphasis. Placing the SN65LVPE801 close to the end of the interconnect allows the device equalizer to address the majority of the high frequency losses introduced in the channel.

The designer will want to ensure that the channel loss for the interconnect material and length is matched reasonably well to the selectable equalization and de-emphasis settings available on the SN65LVPE801. The table above provides an estimate of the amount of FR4 material that could be used as a function of the signal rate. In any case, channel modeling would be prudent to ensure that the SATA host, interconnect, SATA equalizer/re-driver, and SATA Sink can establish and maintain a low BER link.

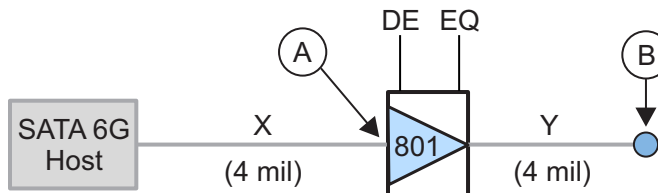
The AC coupling capacitors of 10 nF are chosen to comply with the SATA standard (< 12 nF)

Often a designer may not be sure whether a signal conditioning device like the SN65LVPE801 will be needed in their specific application. The SN65LVPE801 allows the user to take the guess work of using a signal conditioning device in a SATA link. With the SN65LVPE801 the designer has the option to use or remove the device based on signal conditioning needs. **Figure 11** shows guidelines that could be used to allow in situ testing when a board is available. The designer would start with 0  $\Omega$  resistors in place to determine if the eye quality at the end of the link is satisfactory. If the eye opening is not sufficient, the 0  $\Omega$  resistors could be replaced with the SN65LVPE801.



**Figure 11. Implementation Guideline**

To demonstrate the effectiveness of the SN65LVPE801 signal conditioning for varied configurations that may be encountered, [Figure 12](#) will be used as a reference. A Gen3, 6 Gbps SATA host communicates with a sink located at point B. The host and sink are separated by “X+Y” inches, where X represents the distance between the host and the SN65LVPE801, while Y represents the distance between the SN65LVPE801 and the sink. The [Application Curves](#) are for a 6-Gbps K28.5 pattern, with  $V_{CC} = 3.3\text{ V}$  and at an ambient temperature of 25°C.



**Figure 12. Test Points**



## 9.2.3 Application Curves

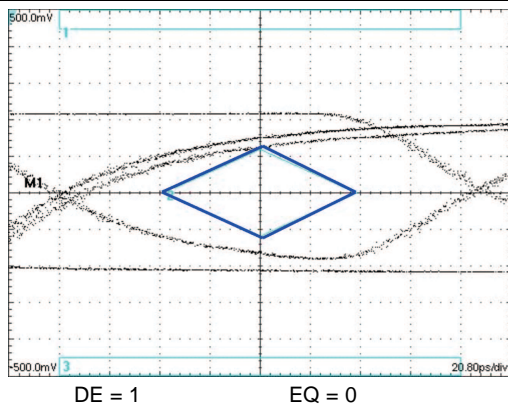


Figure 13. Eye Pattern at A → X = 8"; Y = 2"

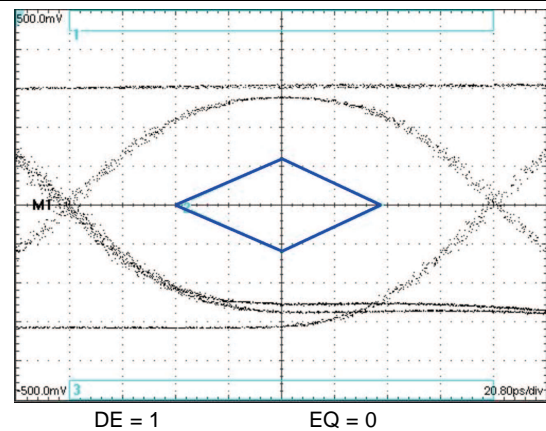


Figure 14. Eye Pattern at B → X = 8"; Y = 2"

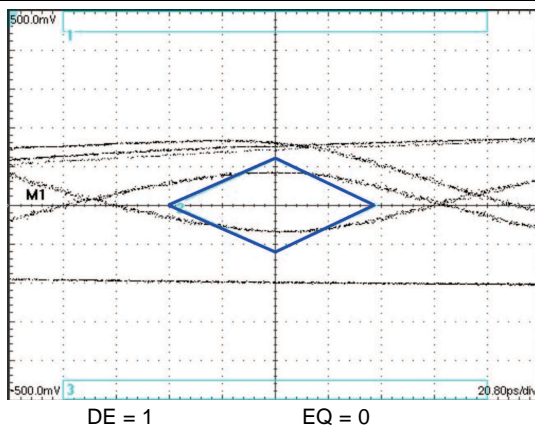


Figure 15. Eye Pattern at A → X = 16"; Y = 2"

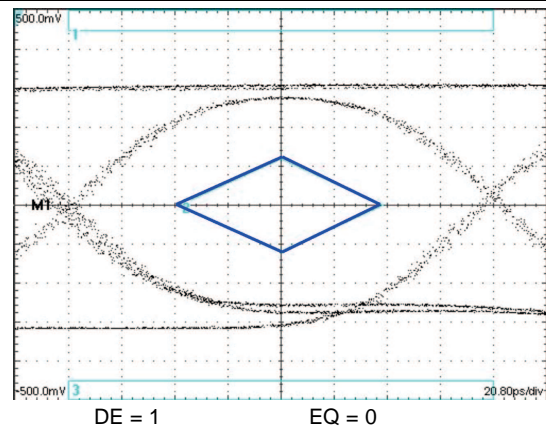


Figure 16. Eye Pattern at B → X = 16"; Y = 2"

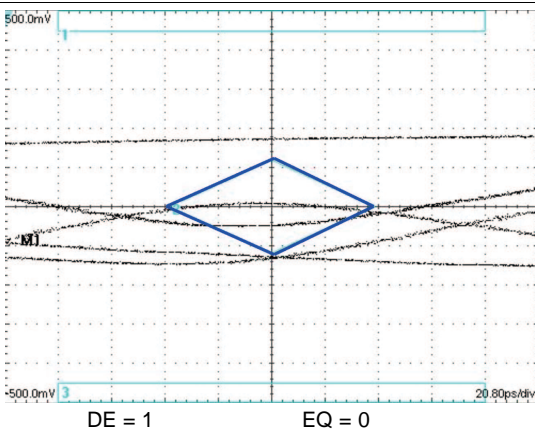


Figure 17. Eye Pattern at A → X = 24"; Y = 2"

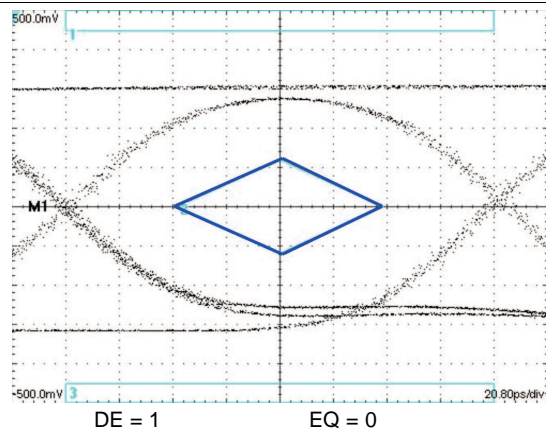
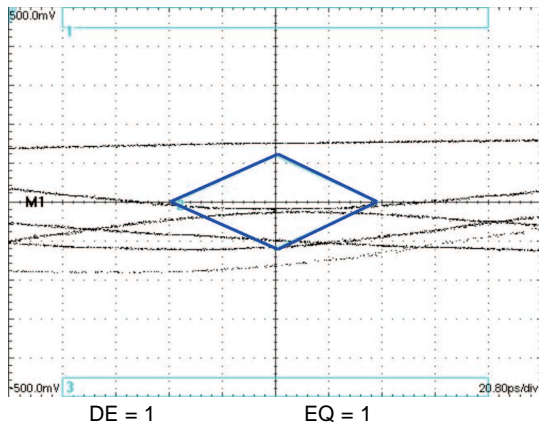
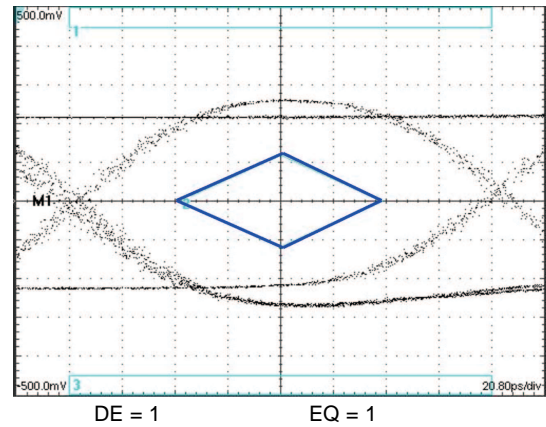


Figure 18. Eye Pattern at B → X = 24"; Y = 2"

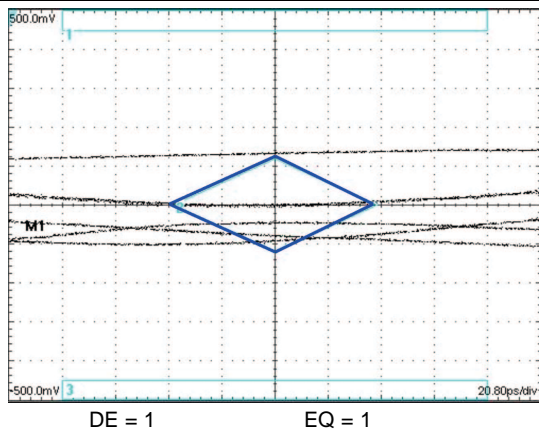




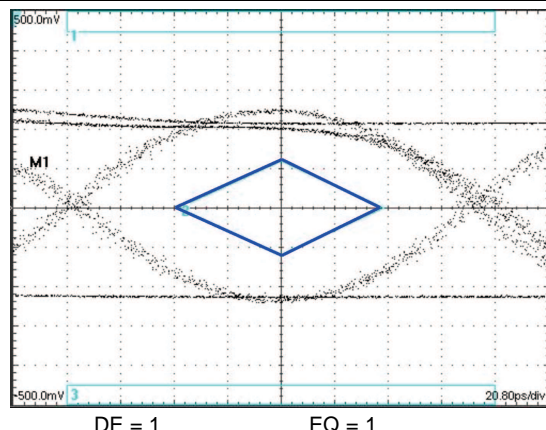
**Figure 19. Eye Pattern at A → X = 32"; Y = 2"**



**Figure 20. Eye Pattern at B → X = 32"; Y = 2"**

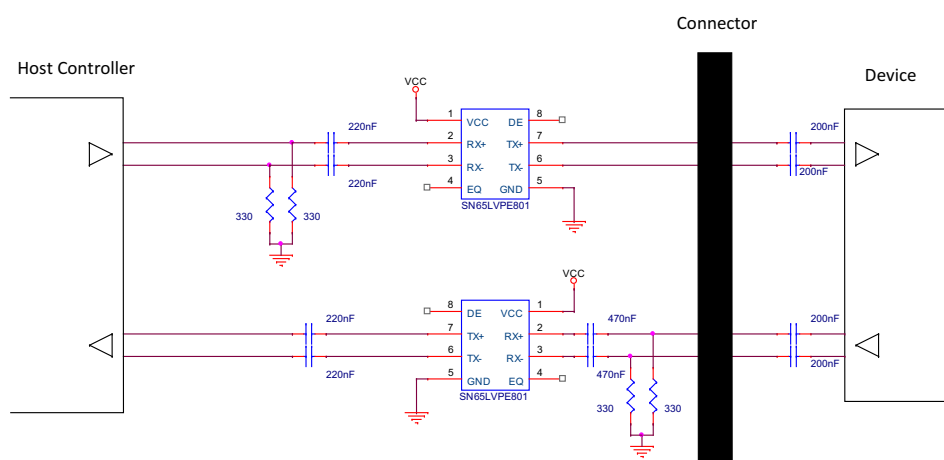


**Figure 21. Eye Pattern at A → X = 40"; Y = 2"**



**Figure 22. Eye Pattern at B → X = 40"; Y = 2"**

## 9.2.4 SATA Express Applications



**Figure 23. SN65LVPE801 SATA Express Reference Schematic**  
**EQ: 7 dB when Floated, DE: 0 dB when Floated**

### 9.2.4.1 Design Requirements

DESIGN PARAMETERS	VALUE
SATA Express Signaling Rate	1.5 - 8.0 Gbps
AC Coupling Capacitance	200 - 220 nF
Interconnect Characteristic Impedance	100 Ohms
Interconnect Length	Up to 50" FR4 for SATA Gen2 Up to 40" FR4 for SATA Gen3
Termination Resistance	100 Ohms differential integrated into TX and RX

### 9.2.4.2 Detailed Design Procedure

Figure 23 is a reference schematic of a SATAe implementation using the SN65LVPE801. With a SATAe design, both SATA and PCI Express must be supported. SATAe supports both cabled and direct connections. Using a cabled application as an example, the SATAe power connector includes an Interface Detect (IFDet, power connector pin P4) signal that indicates whether a SATA client or a PCIe client is connected.

When the SATAe host determines that a PCIe client is connected, the SATAe host performs receiver detection. Receiver detection determines the presence of a client by detecting the load impedance. The transmitter performs a common mode voltage shift, and measures the rate at which the voltage at the transmitter output changes. The rate of change indicates if a client is present (fast charging when a low impedance load is present, or slow charging when the load is open or high impedance). With the implementation in Figure 23, 330-Ω pulldowns have been inserted between the host and the SN65LVPE801. The pulldown resistors indicate to the host that a client is present. While an actual client would be expected to have an active load of 50 Ω single ended, the 330 Ω is chosen here to meet two requirements. The 330 Ω is low enough to force the SATAe host to decide that a receiver is present, while also high enough to only marginally affect the load when the SN65LVPE801 is active, and presenting a 50-Ω load. With the 50 Ω and 330 Ω are both present, the parallel combination of 43 Ω is satisfactory for most applications.

Assuming that the SATAe host has detected (via IFDet) that a SATA client is present, the SATAe host communicates with the client via the SN65LVPE801. The SATA standard does not have a receiver detection mode as is present in PCIe. A SATA host does use OOB signaling to communicate identification information. The SN65LVPE801 incorporates an OOB detector in order to support OOB signaling through the device. The OOB detector drives a squelch circuit on the SN65LVPE801 output transmitter. (See [OOB/Squelch](#) for more details on the OOB/Squelch circuitry.)

Returning again to Figure 23, we see 200-nF AC coupling capacitors on the device or client side of the interface. These capacitors allow interfacing to both SATA and PCIe clients. In the case of a PCIe client, the 200 nF is within the acceptable range for all PCIe devices. When a SATA client is present, the 200 nF capacitor has little effect on the overall link, as it appears in series with the 12-nF (max) AC coupling capacitor incorporated into the SATA client. The 200 nF in series with the 12 nF presents an effective capacitance of 11.3 nF, as expected less than the 12-nF maximum permitted.

The physical placement of the resistors on the high-speed transmission lines can be made as not to create a stub on the transmission line by using resistors with the 0201 package size, an example is provided in Figure 24.

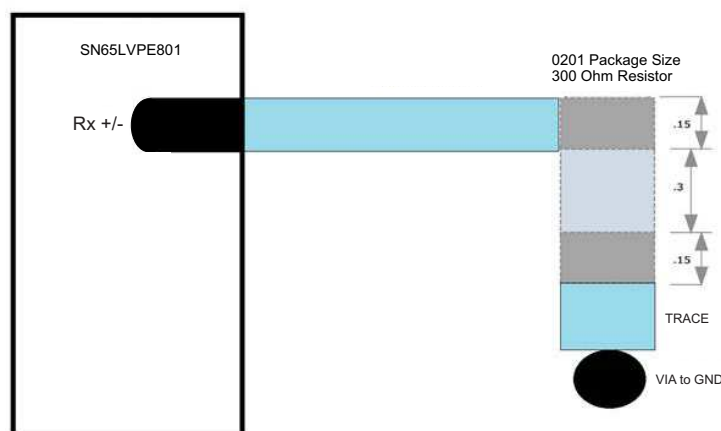
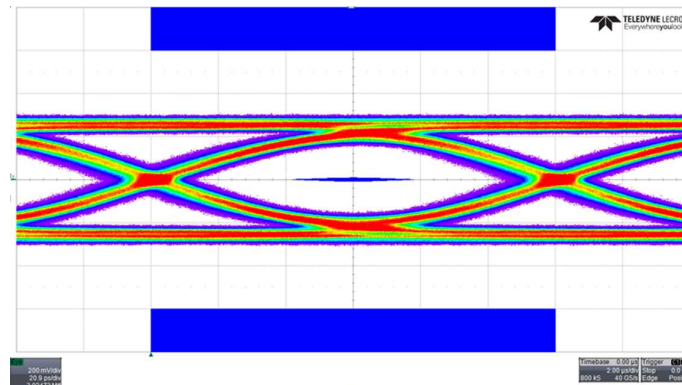


Figure 24. Resistor Placement to Avoid Stub (All Dimensions in mm)

### 9.2.4.3 Application Curve

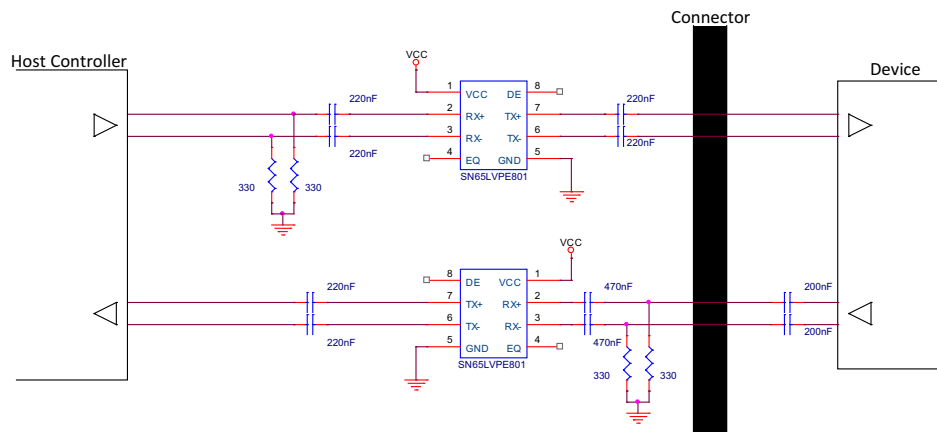
Eye-diagrams were taken on the SN65LVPE801 configured as in Figure 23 above. Testing was performed at a PCIe 3.0 speed of 8Gbps.



**Figure 25. SN65LVPE801 8-Gbps Eye-Diagram**

### 9.2.5 PCIe Applications

PCIe-only applications are implemented in a manner very similar to SATA Express applications as covered in 9.2.2. Looking at Figure 27, and comparing it to the SATA Express application in Figure 24, a single change is noted. For PCIe applications the 220 nF AC-coupling capacitors on the Host-to-Device link are relocated from the Device side of the connector to the Host side. No other changes are required. PCIe device detection operates as outlined in Section 9.2.2.2.



**Figure 26. SN65LVPE801 PCI-Express Reference Schematic**  
EQ: 7 dB when Floated, DE: 0 dB when Floated

## 10 Power Supply Recommendations

### 10.1 Device Power

The SN65LVPE801DRF is designed to operate from a single 3.3-V supply. Always practice proper power supply sequencing procedure. Apply  $V_{CC}$  first before any input signals are applied to the device. The power down sequence is in reverse order.

## 11 Layout

### 11.1 Layout Guidelines

#### 11.1.1 Return Current and Plane References

High frequency return signal/current is defined as the path that a signal follows back to its original source as all signals flow in a closed loop. Minimizing the loop area of the closed loop is beneficial for both EMI (Electro-Magnetic Interference) reduction and signal integrity.

The best way to minimize loop area is to always have a signal reference their nearest solid ground or power plane. Obstructions to the return signal will cause signal integrity problems like reflections, crosstalk, undershoot and overshoot.

Signals can reference either power or ground planes, but ground is preferred. Without solid plane references, single ended and differential impedance control is very hard to accomplish; crosstalk to other signals may happen as the return signals will have no other path. This type of crosstalk is difficult to troubleshoot.

Symmetric pairing of solid planes in the layer stackup can significantly reduce warping of the PCB during the manufacturing process. Warping of the PCB is crucial to minimize on boards that uses BGA components.

#### 11.2 Layout Example

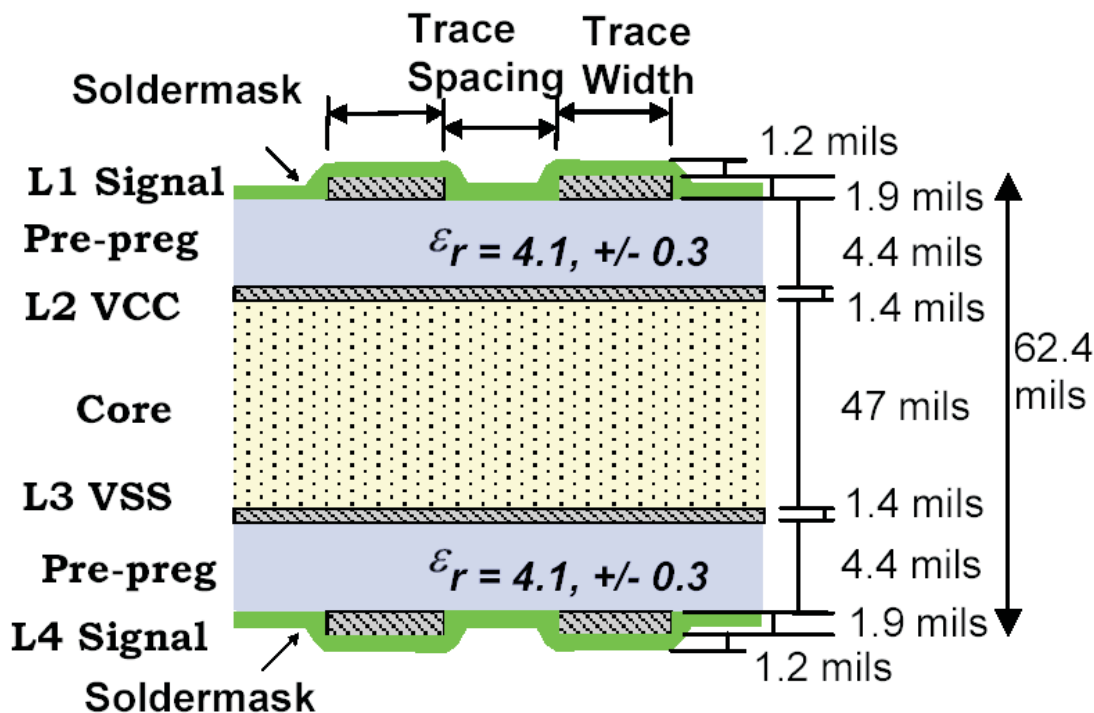


Figure 27. Printed Circuit Board Stackup (FR-4 Example)

## Layout Example (continued)

PCB layer configuration suggestions for stackup symmetry and signal integrity.

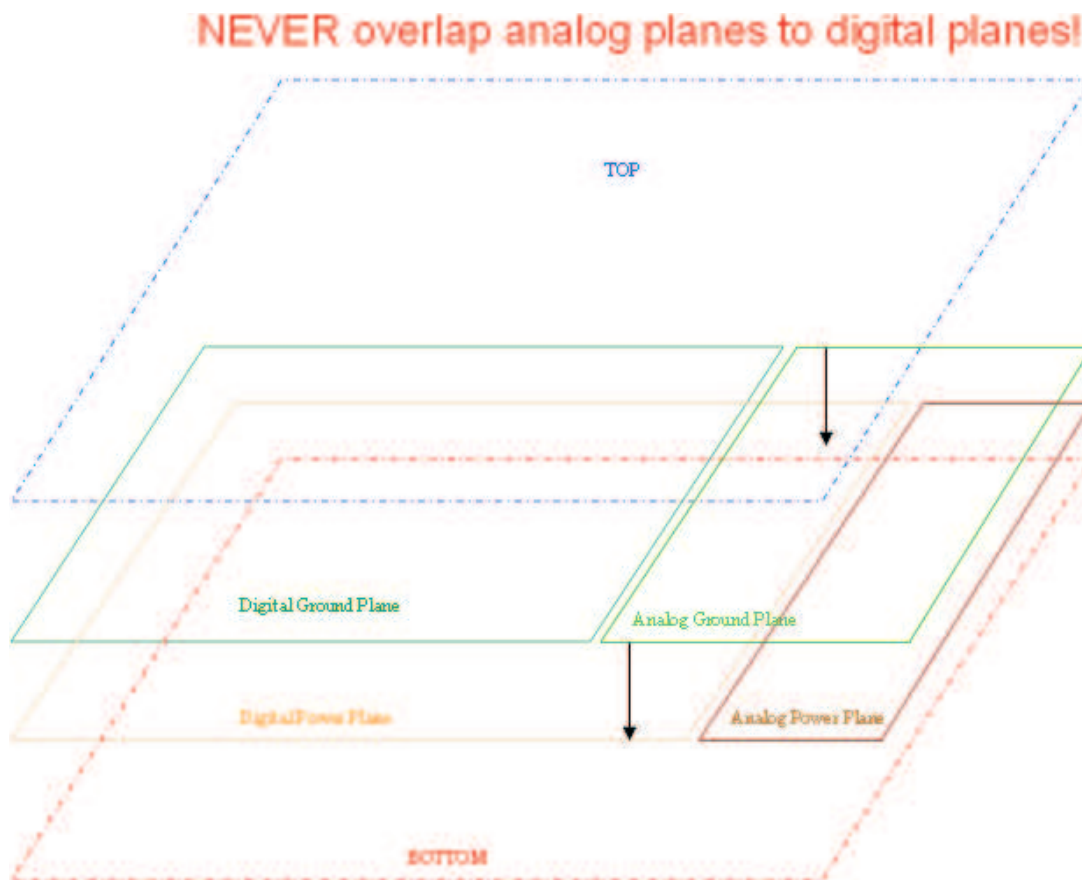
4 Layer		6 Layer		10 Layer	
Layer 1	(Top)	Layer 1	(Top)	Layer 1	(Top)
Layer 2	(GND)	Layer 2	(GND)	Layer 2	(GND)
Layer 3	(PWR)	Layer 3	(Signal)	Layer 3	(Signal)
Layer 4	(Bottom)	Layer 4	(Signal)	Layer 4	(Signal)
		Layer 5	(PWR)	Layer 5	(PWR)
		Layer 6	(Bottom)	Layer 6	(GND)
				Layer 7	(Signal)
				Layer 8	(Signal)
				Layer 9	(GND)
				Layer 10	(Bottom)

**Figure 28. PCB Layer Configuration Suggestions**

## Layout Example (continued)

### 11.2.1 Split Planes – What to Avoid

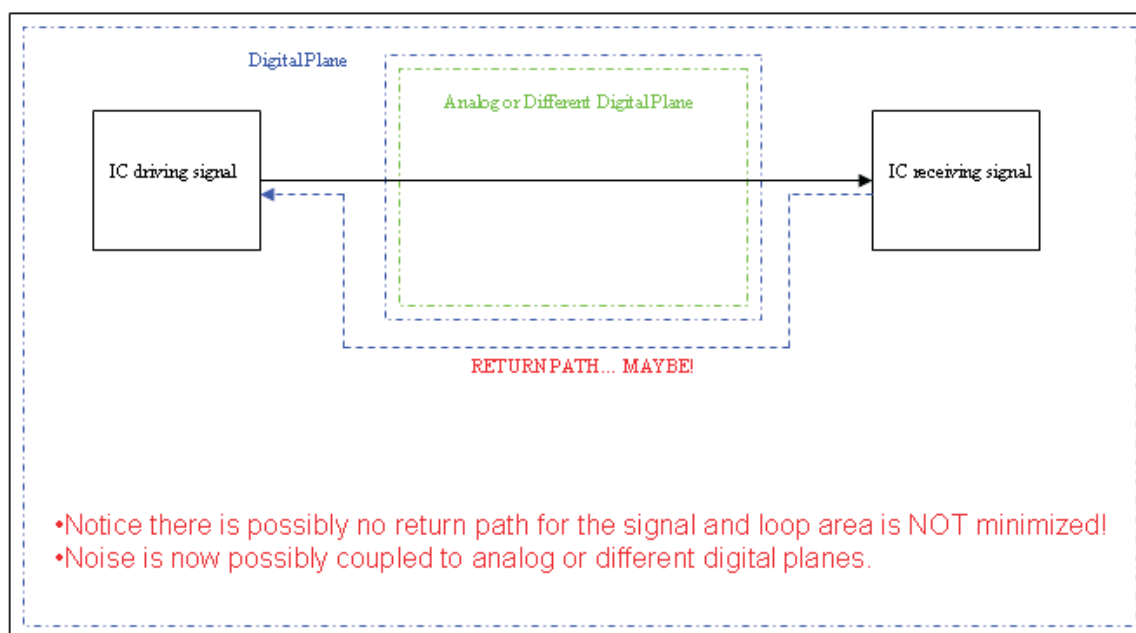
Never route signals over splits in their perspective reference planes.



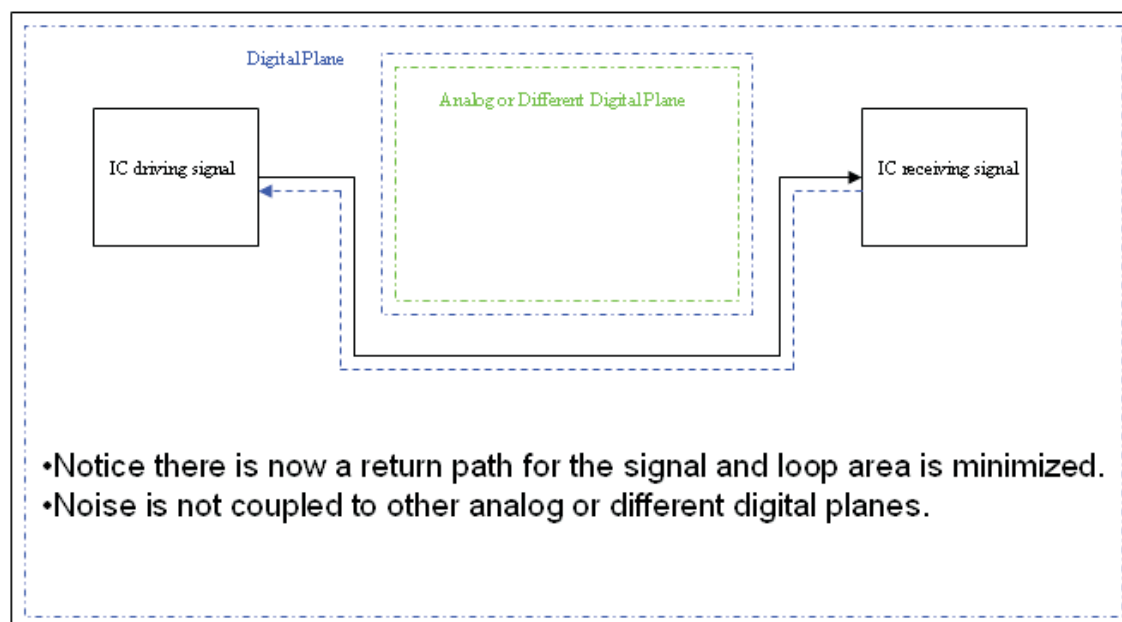
**Figure 29. Overlapping Analog and Digital Planes**

**Layout Example (continued)**

This type of routing will compromise signal integrity!!


**Figure 30. Incorrect Routing**

Proper way to route AROUND splits in planes


**Figure 31. Proper Routing**

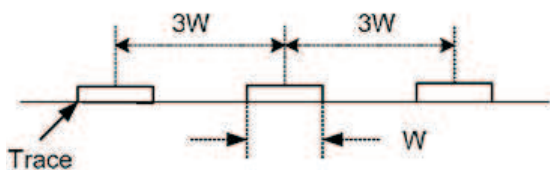


## Layout Example (continued)

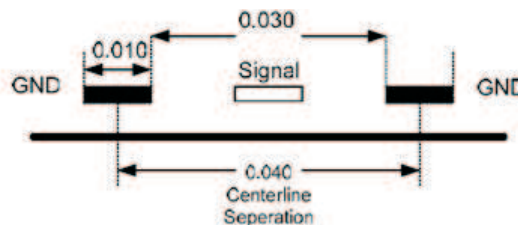
### 11.2.2 Avoiding Crosstalk

Crosstalk is defined as interference from one trace to another by either or both inductive and capacitive coupling. Best ways to avoid crosstalk are:

- Provide stable reference planes for all high speed signals (as noted in previous sections).
- Use the 3W rule (3 times the width of trace for separation) where applicable on all signals, but absolutely use on clock signals.
- Use ground traces/guards around either “victim” or “aggressor” signals prone to crosstalk.
- When constrained and space limited on areas of the PCB to route parallel buses, series and/or end termination resistors can be used to route traces closer than what is normally recommended. However, calculations and simulations must be done to validate the use of series or end termination resistors to eliminate crosstalk.



The “3W” rule



Example use of ground guard traces

**Figure 32. Ways to Avoid Crosstalk**

## 12 Device and Documentation Support

### 12.1 Trademarks

All trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVPE801DRFR	PREVIEW	WSO	DRF	8	3000	TBD	Call TI	Call TI	0 to 85	801	
SN65LVPE801DRFT	PREVIEW	WSO	DRF	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	801	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE801DRFT	WSO	DRF	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

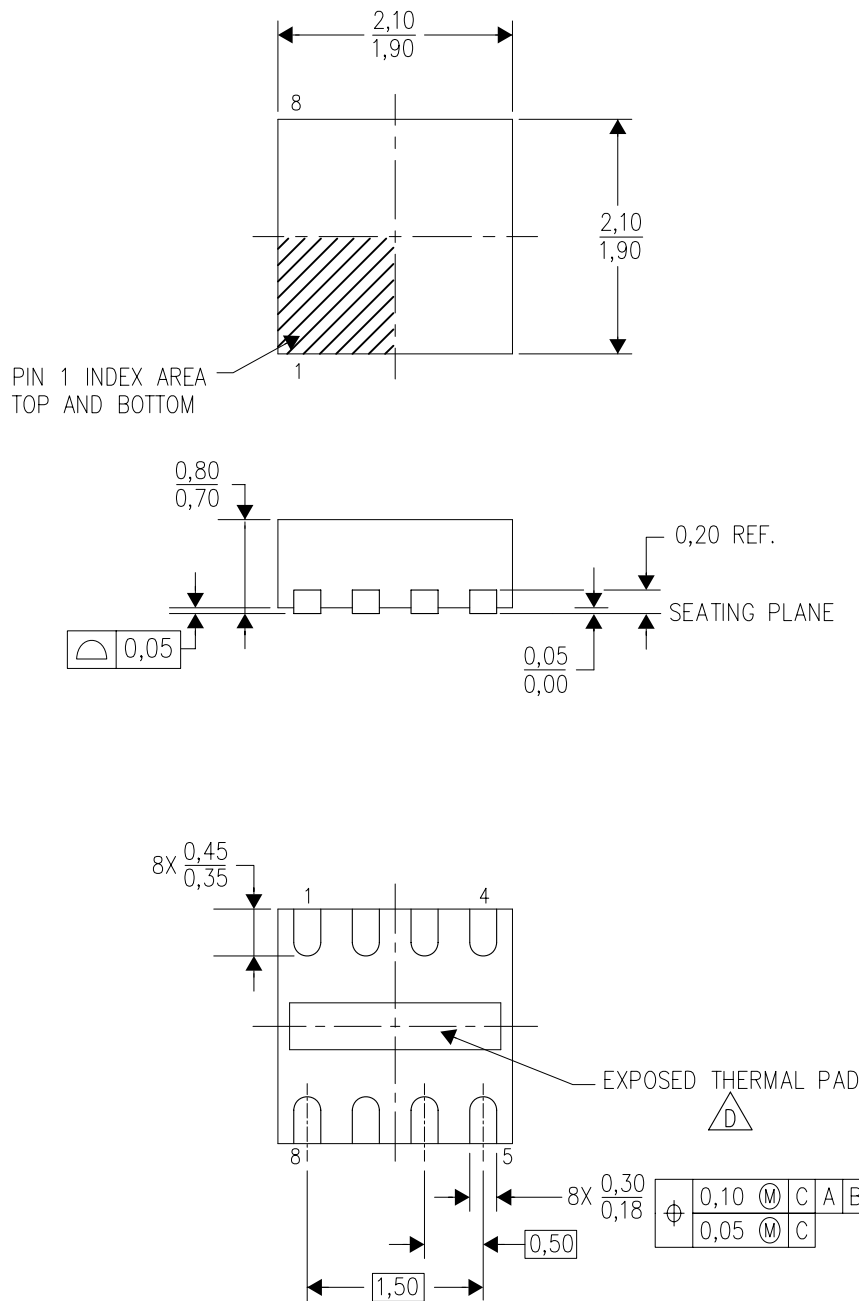


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE801DRFT	WSON	DRF	8	250	210.0	185.0	35.0

DRF (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4205287/E 10/10

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-Leads (QFN) package configuration.
  - D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
  - E. Falls within JEDEC MO-229.

DRF (S-PWSON-N8)

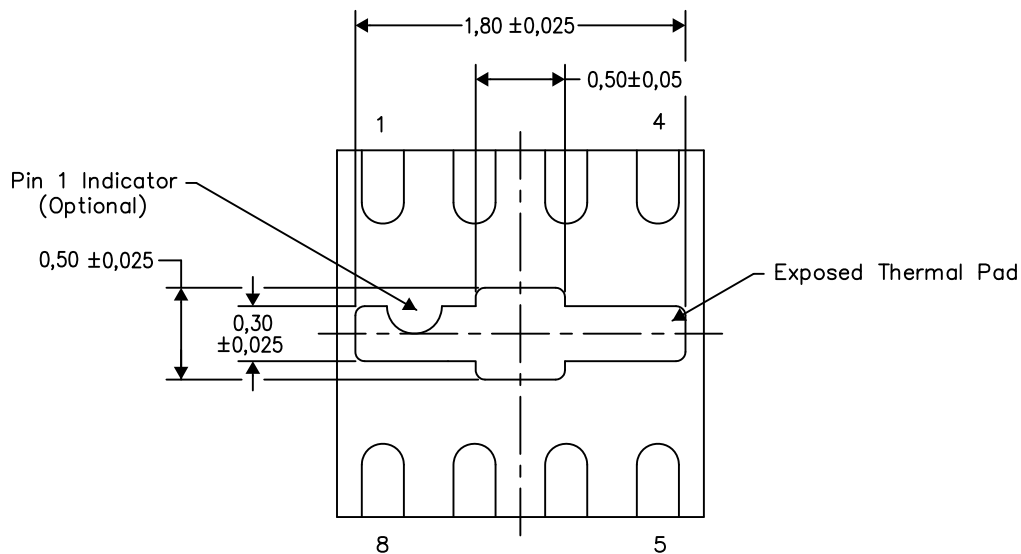
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

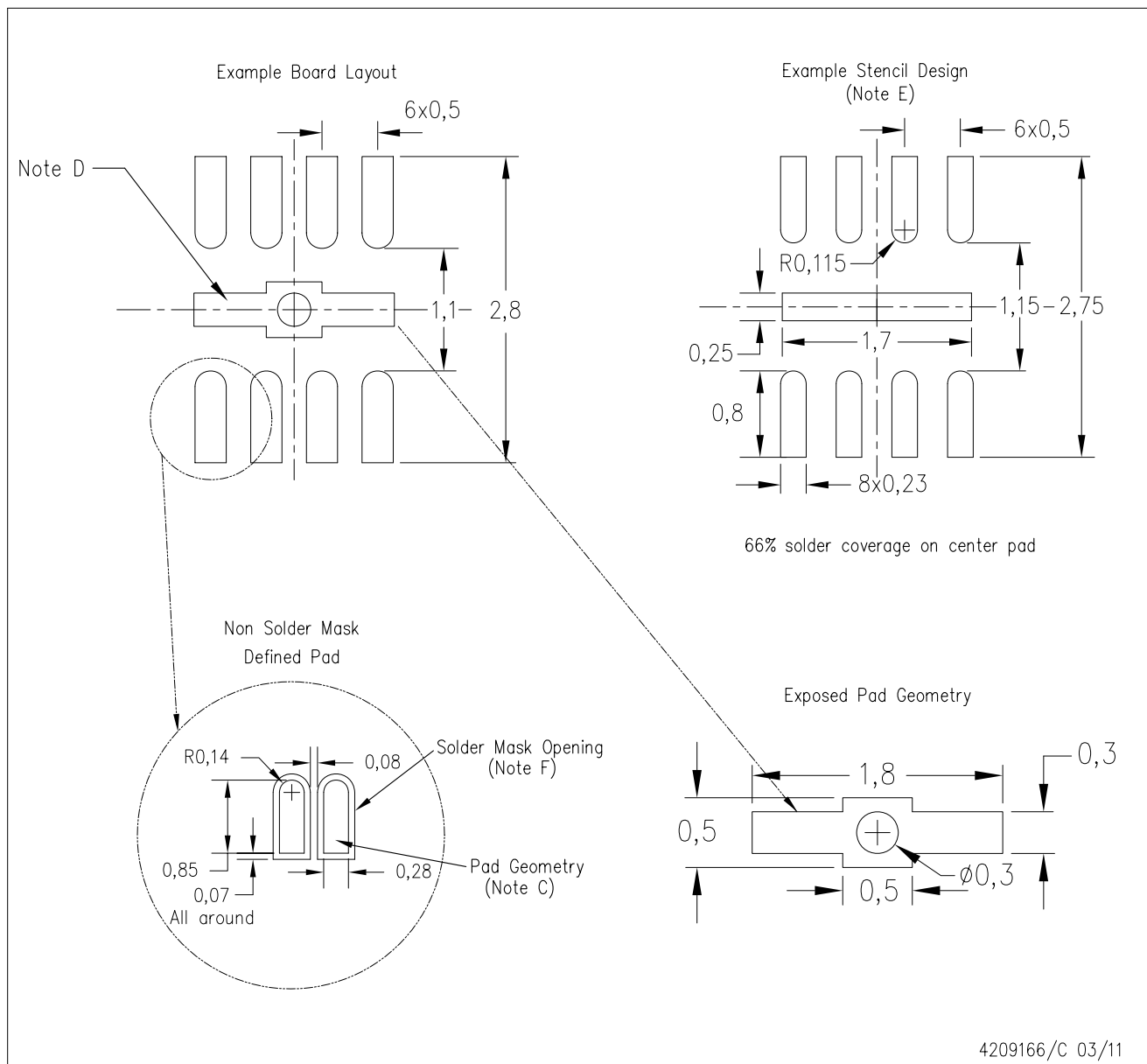
4206840/H 12/14

NOTE: A. All linear dimensions are in millimeters



DRF (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
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