



USB Audio Controller

Data Sheet

SN11220APF

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SN11220APF
USB Audio Controller
V1.03

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SN11220APF

I. Description

SONiX SN11220APF is an USB audio controller that suitable for USB headset applications. It can be used for PC as well as next generation game consoles like PS2 or other platforms. It supports many sampling rates ranging from 8KHz to 48KHz in analog playback and recording. In digital mode, three sampling rates, 32KHz, 44.1KHz and 48KHz are supported. It supports both AC'97 and I²S CODEC interfaces. Many features of SN11220APF can be enabled / disabled by external configuration pins. This provides a great flexibility for the system manufacturers to build different end products with just changing few resistors. Equipped with built-in PLLs, SN11220APF can provide digital quality audio without adding system cost. With so many features and low cost, SN11220APF is an ideal chip to build a PC/PS2 headset solution.

In digital playback mode, it receives audio stream from PC via USB interface and transmits audio data according to the AES/EBU, IEC60958, S/PDIF consumer interface standards. In analog playback mode, it supports 2 channels CODEC for analog playback.

In digital recording mode, it receives S/PDIF digital audio input and sends back to PC through USB. Three sampling rates; includes 32 KHz, 44.1 KHz and 48 KHz; are automatically locked internally.

In analog mode, all 8 sampling rates are supported by analog audio playback and recording.

Totally one control pipe, two isochronous pipes, and one interrupt pipe are supported by SN11220APF.



II. Features

USB

- Compliant with USB 2.0 Full Speed Operation
- Compliant with USB audio device class specification v1.0; and USB HID class specification v1.1
- Compatible with Win98 SE/ WinME/ Win2000/ WinXP and MacOS 9.2.1/MacOS10.2/MacOS10.4 without additional driver
- Plug-and-Play operation with Microsoft OS or MacOS default drivers
- USB bus power or self power option
- Full-duplex playback/ recording audio stream without sound card in PC
- USB audio function topology has four input terminals, three output terminals, one selector unit, one mixer unit and six feature units
- USB alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive
- Isochronous transfer uses adaptive, synchronous synchronization
- Claim variable max packet size for saving USB bandwidth; according to sampling rate under
- Transferring length up to each 16 bytes among PC to device and device to PC by USB HID
- 6MHz crystal input with on-chip PLL and embedded transceiver for USB

CODEC Interface

- Supports AC'97 component specification v2.1 and v2.2; AC link interface for external AC97 audio CODEC
- Supports 2ch CODEC with I²S, Left-justified serial interface format
- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM audio
- 32KHz, 44.1KHz and 48KHz sampling rates for 2 channels playback/recording in digital mode
- Conveys AC-3 data stream by S/PDIF output
- Supports SCMS (Serial Copy Management System) copy protection
- 8KHz, 11.025KHz, 16KHz, 22.05KHz, 24KHz, 32KHz, 44.1KHz and 48KHz sampling rates for 2 channels playback and recording



- Input pin control for volume up / down, play mute, and record mute
- Embedded Digital Volume Control of Line out / in for I²S interface mode
- On-chip PLL for synchronized with USB host for CODEC interface

Peripheral

- 3.3 V core operation and 5 V tolerant I/O
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps (Fast-mode)
- EEPROM interface for customized USB IDs and strings; CODEC registers programming
- EEPROM content can be read from HID pipe
- HID interrupt interval can be modified via EEPROM
- Features programmable by jumper pins and EEPROM values
- Supplied two GPIOs for LED indicator pins for playback and recording mute
- One GPIO pin controlled via USB HID
- Available in 48-pin LQFP (7x7 mm)

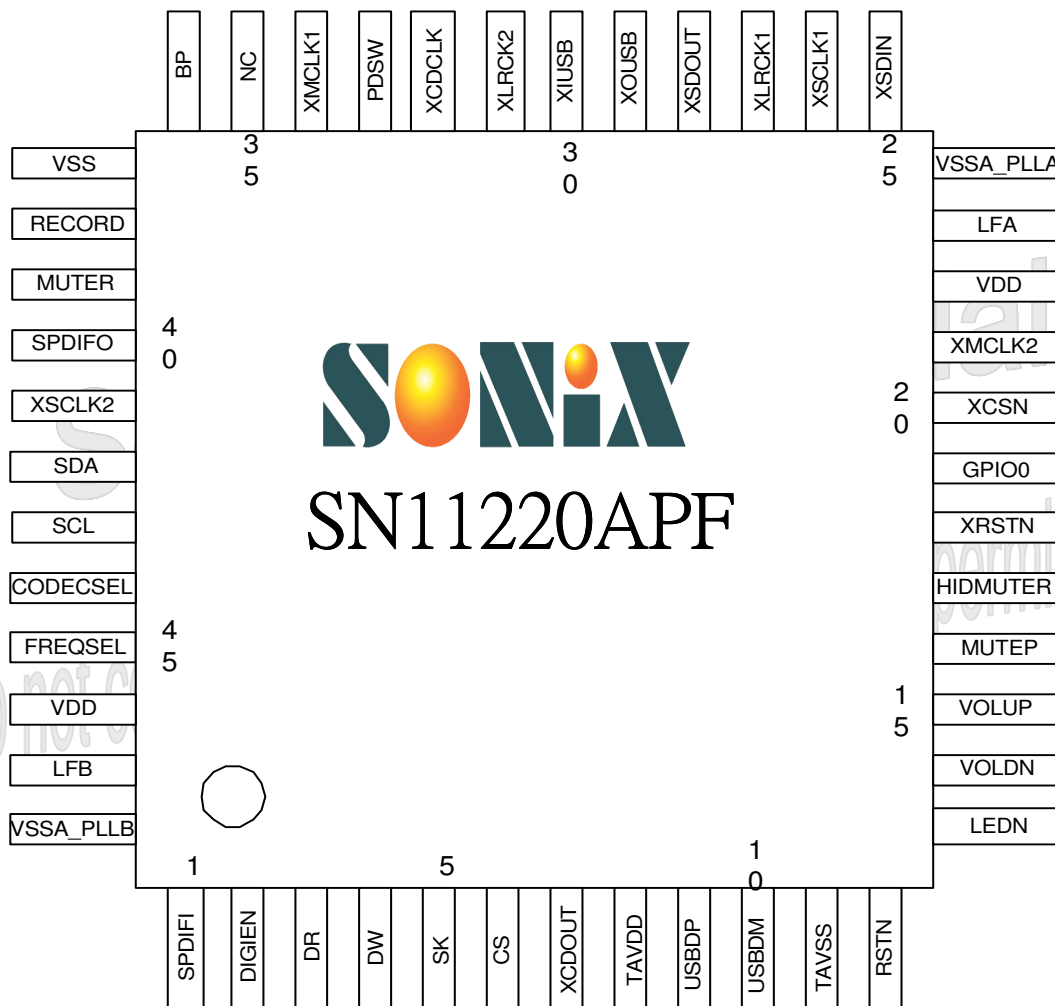


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III. Ordering information

SN11220APF : 48-pin LQFP (7x7x1.4 mm)



IV. Pin assignment and description (48-pin LQFP)

PIN No.	Pad Name	Pin Type	Description
1	SPDIFI	I, ST	Input pin for S/PDIF signal
2	DIGIEN	I, ST	Enable SPDIF In/Out in USB description, 1: enable, 0: disable (analog only)
3	DR(EEPROM_ DO)	I, ST	EEPROM data output
4	DW (EEPROM_ DI)	O, 4mA, SR	EEPROM data input
5	SK (EEPROM_ SK)	O, 4mA, SR	EEPROM clock pin
6	CS (EEPROM_ CS)	O, 4mA, SR	EEPROM chip select
7	XCDOUT	O, 4mA, SR	I ² S CODEC control data (Three-wire serial port DIN)
8	TAVDD	P	Power pin for USB transceiver
9	USBDP	I/O	USB data plus (D+)
10	USBDM	I/O	USB data minus (D-)
11	TAVSS	P	Power pin for USB transceiver
12	RSTN	I, ST	System reset pin, low enable. External pull-high resistor on this pin in operation.
13	LEDN	O, 8mA, SR	LED indicator pin, output low after power on reset, toggle during operation
14	VOLDN	I, ST	Volume down control, edge trigger with 64ms de-bouncing circuit
15	VOLUP	I, ST	Volume up control, edge trigger with 64ms de-bouncing circuit
16	MUTEP	I, ST	Playback mute control pin, edge trigger with 64ms de-bouncing circuit
17	HIDMUTER	O, 8mA, SR	Playback mute led indicator, when MUTER be enabled, driving high for indicating.
18	XRSTN	O, 4mA, SR	CODEC reset
19	GPIO0	I/O	General Purpose I/O 0



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20	XCSN	O, 4mA, SR	I ² S CODEC chip select (Three-wire serial port CS)
21	XMCLK2	O, 8mA, SR	I ² S CODEC master clock for record
22	VDD	P	3.3V power pin
23	LFA	I/O	Filter for internal PLL
24	VSSA_PLLA	P	GND pin
25	XSDIN/AC_DIN	I, ST	I ² S Din for record / AC-link Din
26	XSCLK1	O, 4mA, SR	I ² S SCLK for play
27	XLCK1/AC_SYNC	O, 4mA, SR	I ² S L/R frame for play / AC-link SYNC
28	XSDOUT/AC_DOUT	O, 4mA, SR	I ² S dout for play / AC-link dout
29	XOUSB	O	6 MHz clock osc pin for USB PLL
30	XIUSB	I	6 MHz clock osc pin for USB PLL
31	XLCK2	O, 4mA, SR	I ² S L/R frame for record
32	XCDCLK	O, 4mA, SR	I ² S CODEC control clock (Three-wire serial clock)
33	PDSW	O, 4mA, SR	Power down switch control -- 0: normal mode, 1: power down mode This pin is in power down mode when the device is in suspending mode.
34	XMCLK1/BITCLK	O, 8mA, SR	I ² S CODEC master clock for play / AC-link bit clock
35	NC	O	Not connect to anything
36	BP	I	Connect a bypass capacitor 1uF to GND
37	VSS	P	GND pin
38	RECORD	I, ST	Recording function enable (1) / disable (0)
39	MUTER	I, ST	Recording mute, edge trigger with 64ms de-bouncing circuit
40	SPDIFO	O, 8mA, SR	S/PDIF data output
41	XSCLK2	O, 4mA, SR	I ² S SCLK for record
42	SDA	I/O, 4mA, SR	Data pin of two-wire serial port for external MCU control This pin must be pull-high by resister.



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43	SCL	I, ST	Clock pin of two-wire serial port for external MCU control. This pin must be pull-high by resister.
44	CODECSEL	I, ST	CODEC interface selection, 0: AC-link, 1: I ² S
45	FREQSEL	I, ST	Frequency range selection, 1: 8 frequencies, 0: 3 frequencies
46	VDD	P	3.3V Power pin
47	LFB	I/O	Filter for internal PLL
48	VSSA_PLLB	P	GND pin

** All input pin are 5 volt tolerance, TTL level and Schmitt trigger

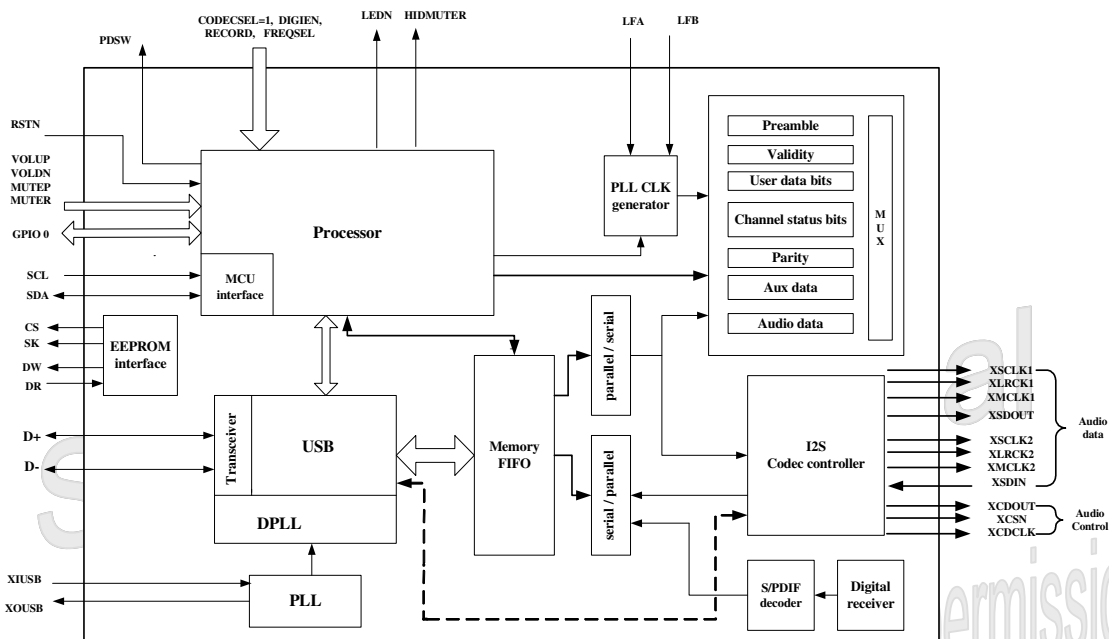
All output pins are slew rate control

I – input pin , **O** – output pin, **P** – power pin, **ST** – Schmitt trigger, **SR** – slew rate control,

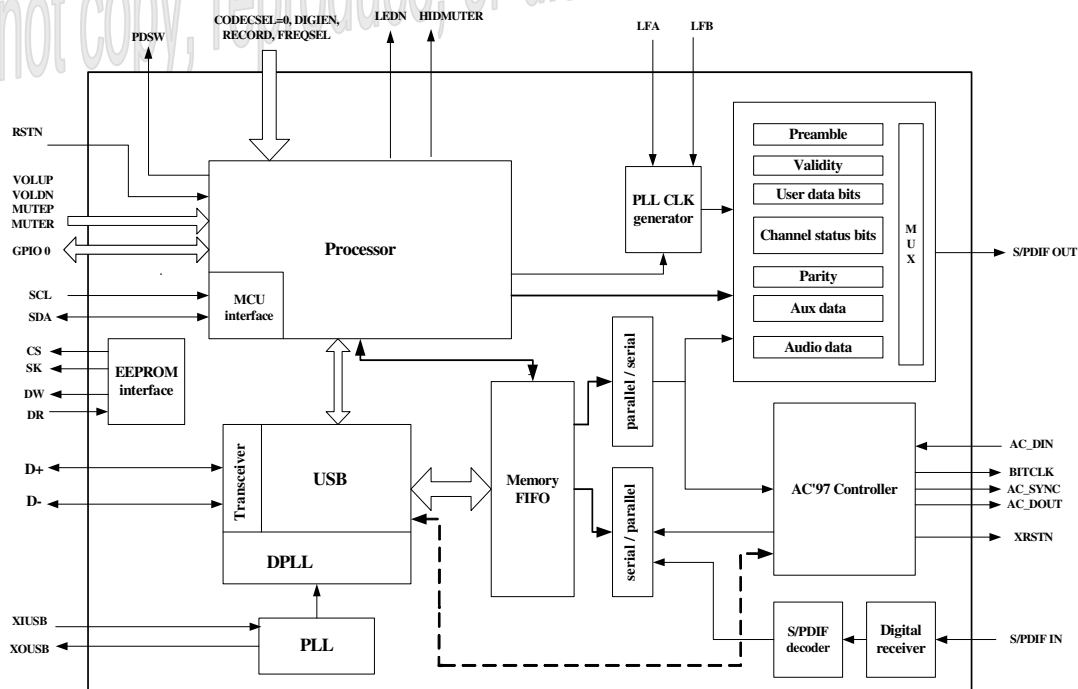
PU/PD – pull up or pull down

V. Block diagram

5.1 I²S interface



5.2 AC'97 interface





VI. EEPROM contents arrangement

The SN11220APF supports an external EEPROM (93C46 16-bit) to be installed for the system manufacturers to customize the USB VID, PID and the vendor/product strings being displayed in the OS to differentiate their own products with the others. The maximum length of the vendor and product string is 16 ASCII characters each. Some of the features supported by the chip can also be programmed through setting proper values in the EEPROM. The table below shows the format of the EEPROM. The detail is described in the following sub-section.

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Address	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0x00	Vendor ID (VID)															
0x01	Product ID (PID)															
0x02	Manufacture string 15								Manufacture string 14							
0x03	Manufacture string 13								Manufacture string 12							
0x04	Manufacture string 11								Manufacture string 10							
0x05	Manufacture string 9								Manufacture string 8							
0x06	Manufacture string 7								Manufacture string 6							
0x07	Manufacture string 5								Manufacture string 4							
0x08	Manufacture string 3								Manufacture string 2							
0x09	Manufacture string 1								Manufacture string 0							
0x0A	Product string 15								Product string 14							
0x0B	Product string 13								Product string 12							
0x0C	Product string 11								Product string 10							
0x0D	Product string 9								Product string 8							
0x0E	Product string 7								Product string 6							
0x0F	Product string 5								Product string 4							
0x10	Product string 3								Product string 2							
0x11	Product string 1								Product string 0							
0x12	Control word 1															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LEFT JSEL	SPIL 4	SPIL 3	SPIL 2	SPIL 1	SPIL 0	0	SELF POW	Manufacture string #				Product string #			
0x13	Control word 2															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved			0	0	0	0	0	HID interval							
0x14	Control word 3															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HID, MUTE R	FS, 512	cdcre g	0	regcnt 3	regcnt 2	regcnt 1	regcnt 0	chk7	chk6	chk5	chk4	chk3	chk2	chk1	chk0
0x15	Reg address (AC' 97) / Reg byte2 (I²S)								Don't care (AC' 97) / Reg byte1 (I²S)							
0x16	Reg dataH (AC' 97) / Reg byte0 (I²S)								Reg dataL (AC' 97) / Don' care (I²S)							
0x17	Reg address (AC' 97) / Reg byte2 (I²S)								Don't care (AC' 97) / Reg byte1 (I²S)							
0x18	Reg dataH (AC' 97) / Reg byte0 (I²S)								Reg dataL (AC' 97) / Don' care (I²S)							

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USB VID and PID :

The default USB VID of SN11220APF is 0x0C45. The default PID is composed by the configurations as below {0, 0, 0, 1, 1, 1, 0, 1, 0, DIGIEN, FREQSEL, CODECSEL, 1, RECORD, POWER_BIT, CODECSEL}. If pin2 tie to high, DIGIEN will equal "1". If pin45 tie to high, FREQSEL will equal "1". If pin44 tie to high, CODECSEL will equal "1". If pin38 tie to high, RECORD will equal "1". The POWER_BIT is used to indicate that the MaxPower in USB descriptor ("1" is 100mA, "0" is 500mA) . Using EEPROM can change the VID and PID. Word address 0x00 is the VID value. Word address 0x01 is the PID value. The bit1 (POWER_BIT) of the PID value will affect the MaxPower in USB descriptor. For example, PID=0x1D22, the bit1=1, this device will be enumerate to a low power device (100mA), or PID=0x1D20, the bit1=0, this device will be enumerate to a high power device (500mA). It should be noted that forbids the VID and PID values cannot be set to 0x0000 or 0xFFFF.

Manufacturer and Product String :

The default manufacturer string is "GENERIC". It can be changed by programming word 0x02 to 0x09 in EEPROM and set the length of it in word 0x12, bit 4 to 7. Manufacturer string length = manufacturer string number + 1 (manufacturer string number = 0x0F means manufacturer string length = 16 bytes) .

There are total of three default product strings in SN11220APF, depending on the features selected. They are listed in the table below.

RECORD	DIGIEN	Product String
0	0	USB Speaker
1	0	USB Headset
X	1	USB Audio Device (S/PDIF in/out device)

The product string can be changed by programming words 0x0A to 0x11 in EEPROM and set the length of it in word 0x12, bit 0 to 3. Product string length = product string number + 1 (product string number = 0x0F means product string length = 16 bytes) .

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Control word 1 :

The control word 1 is located in word 0x12 of EEPROM.

Bit 0 to 7 is the length of USB strings and has been explained in previous paragraphs.

Bit 8 is used to set the self-power bit in the USB descriptor.

Bit 10 to 14 is used to define the length (bits number) of SPI protocol used for programming I²S CODEC. It is named SPIL [4:0]. For the detail information, please refer to below 'CODEC Initial Setting'.

Bit 15 is to enable the left-justify format in I²S mode.

Control word 2 :

The control word 2 is located in word 0x13 of EEPROM.

Bit 0 to 7 is the interval of USB HID Report IN. For example, bit 0 to 7 = 0x0A means that the interval of USB HID Report IN is 10ms and this is default value.

Bit 13 to 15 are reserved for future using and influence no function of SN11220APF.

Bit 8 to 12 should all be set to 0 or SN11220APF will work incorrectly.

Control word 3 :

The control word 3 is located in word 0x14 of EEPROM.

Bit 0 to 7 is the magic word that validated the CODEC controlled data after word 0x14. It is named chk [7:0]. It should always be filled with value 0xAB.

Bit 8 to 11 is the number of the registers being programmed via EEPROM for initiated CODEC. It is named regcnt [3:0]. For AC'97 CODEC, when there is no register to be programmed, these bits should be set to 0. For I²S CODEC, these bits can never be set to 0 even there is no register to be programmed. For the detail information, please refer to below 'CODEC Initial Setting'.

Bit 12 it must be set to 0.

Bit 13 selects whether the values programmed to CODEC registers coming from EEPROM (0) or internal default (1) .

Bit 14 select 512 times sampling rate for I²S interface.

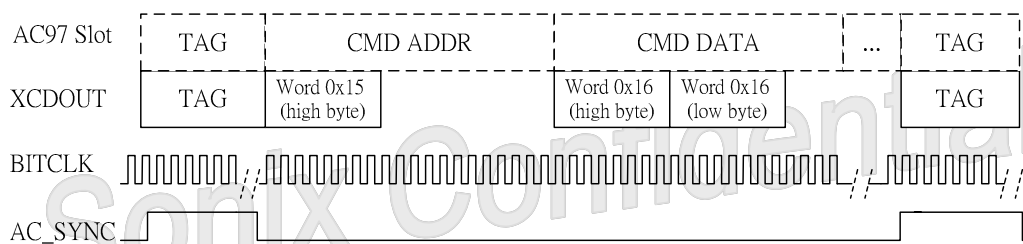
Bit 15 defines the behavior of record mute button for AC'97 CODEC.

CODEC Initial Setting

In AC'97 CODEC mode:

The value of regcnt [3:0] must between the capacity of EEPROM limitation and 1. The high byte of word 0x15 is the address of AC'97 CODEC's register except MSB. The word 0x16 is the data of the register. The MSB of word 0x15 select read/write command. After word 0x17 also do for this reason. For example,

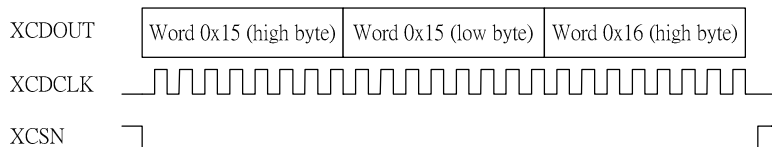
regcnt [3:0] = 1



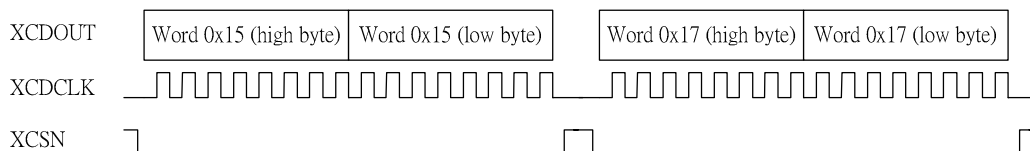
In I²S CODEC mode:

The value of SPIL [4:0] must between 24 and 1. The value of regcnt [3:0] must between the capacity of EEPROM limitation and 1. The word 0x15 and high byte of word 0x16 organize the first of register data. After word 0x17 also do for this reason. There are two examples as below,

SPIL [4:0] = 24
regcnt [3:0] = 1



SPIL [4:0] = 16
regcnt [3:0] = 2



If you have no need to initial the CODEC, bit 13 of control word 3 should be set to 1

or chk [7:0] be not set to 0xAB.

VII. HID bytes arrangement :

The SN11220APF is equipped with a special feature to let the host software to communicate with the USB downstream devices via the HID pipe. Using this feature, the system manufacturers can easily upgrade or increase the functions of their product by just updating the software installed on the PC. There are 16 bytes each for HID in and HID out. They will be explained in the paragraphs below separately.

PC receives the data from two-wire serial port and button/GPIO status from the SN11220APF, there are two ways. The first is to receive the HID report of the HID pipe regularly. If any button/GPIO value changes or data received from the two-wire serial port, the new values will be sent to the host every HID interval time (defined in word 0x13 bit 0 to 7 on EEPROM and default is 10ms) . The second way is to issue a HID class request “Get Report” to get the input report. To send data to the USB audio controller, the host software should issue a HID class request “Set Report” to send the output report. There are total of 16 bytes of both output report and input report. The format of them is described as below.

Report In Bytes (SN11220 to PC by USB HID)

Byte 0	Buttons	Bit 0	Vol up
		Bit 1	Vol down
		Bit 2	Mute play
		Bit 3	Mute rec (OS can't do this)
		Bit 4	GPIO0 state (low="0", high="1")
		Bit 5	GPIO1 (uncontrollable)
		Bit 6	GPIO2 (uncontrollable)
		Bit 7	GPIO3 (uncontrollable)
Byte 1	MCU byte 0	Bit 7~0	Two-wire serial port input register 0
Byte 2	MCU byte 1	Bit 7~0	Two-wire serial port input register 1
Byte 3	SPDIF category	Bit 7~0	SPDIF category

Byte 4	SPDIF freq/resolution	Bit 7~4	SPDIF symbol size
		Bit 3~0	SPDIF sampling rate
Byte 5	CODEC/EEPROM reg data1	Bit 7~0	Reg 1 data/reg data [15:8] 16-bit
Byte 6	CODEC/EEPROM reg data0	Bit 7~0	Reg 0 data/reg data [7:0]
Byte 7	MCU byte 2	Bit 7~0	Two-wire serial port input register 2
Byte 8	MCU byte 3	Bit 7~0	Two-wire serial port input register 3
Byte 9	MCU byte 4	Bit 7~0	Two-wire serial port input register 4
Byte A	MCU byte 5	Bit 7~0	Two-wire serial port input register 5
Byte B	MCU byte 6	Bit 7~0	Two-wire serial port input register 6
Byte C	MCU byte 7	Bit 7~0	Two-wire serial port input register 7
Byte D	MCU byte 8	Bit 7~0	Two-wire serial port input register 8
Byte E	MCU byte 9	Bit 7~0	Two-wire serial port input register 9
Byte F	Used by SONiX	Bit 7~0	Fixed 0x00

Byte 0 :

Byte 0 is used to report the button and GPIO status of the USB device.

Bit 0 and 1 are linked to the master volume control bar of the audio control panel in the OS.

Bit 2 is linked to the master playback mute checkbox of the audio control panel in the OS.

Bit 3 is used to mute the recording, but there is no this command in OS. SONiX design this function in the SN11220.

Bit 4 to 7 is corresponding to the value of GPIO 0 to 3. Note that GPIO1, GPIO2 and GPIO3 are uncontrollable of SN11220APF.

Byte 1 :

Byte 1 is used to return the register 0 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 2 :

Byte 2 is used to return the register 1 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.



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Byte 3 :

Byte 3 returns the SPDIF category field decoded from the SPDIF port of SN11220APF.

Byte 4 :

Byte 4 returns the audio data form carried by the SPDIF. Bit 7 to 4 indicates the audio symbol size and bit 3 to 0 indicates the audio sampling rate.

Byte 5 :

Byte 5 returns the high byte of the register content being read from CODEC in 16-bit mode or the lower address register content in 8-bit mode. When 'HID mode' set to read EEPROM with address, Byte 5 is replaced the high byte data [15:8] at this address in EEPROM.

Byte 6 :

Byte 6 returns the low byte of the register content being read from CODEC in 16-bit mode or the higher address register content in 8-bit mode. When 'Report out' send "read EEPROM command" with address, this byte is replaced the low Byte data [7:0] at this address in EEPROM.

Byte 7 :

Byte 7 is used to return the register 2 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 8 :

Byte 8 is used to return the register 3 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 9 :

Byte 9 is used to return the register 4 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte A :

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Byte A is used to return the register 5 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte B :

Byte B is used to return the register 6 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte C :

Byte C is used to return the register 7 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte D :

Byte D is used to return the register 8 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte E :

Byte E is used to return the register 9 value received by the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte F :

Byte F is used by SONiX for the special purpose. In SN11220APF, it will be set to 0x00 at any time.

Report Out Bytes (PC to SN11220 by USB HID)

Byte 0	SPDIF Setting	Bit 0	PCM (0) / non-audio or AC3 (1)
		Bit 1	Copy not allowed (0) /copy allowed (1)
		Bit 2	Disable SCMS (0) / enable SCMS (1)
		Bit 3	SPDIF default setting (0) / programmable setting (1)
		Bit 4	GPIO 0 Out/In select / Reg program length 0
		Bit 5	SN11220APF ignore / Reg program length 1
		Bit 6	SN11220APF ignore / Reg program length 2
		Bit 7	SN11220APF ignore / Reg program length 3



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Byte 1	SPDIF category	Bit 7~0	SPDIF category field
Byte 2	MCU byte 0	Bit 7~0	Two-wire serial port output register 0
Byte 3	GPIO out	Bit 0	GPIO 0 (set “1” to high, set “0” to low)
		Bit 1	SN11220APF ignore
		Bit 2	
		Bit 3	
	Mode setting	Bit 6~4	HID control mode setting
	Volume control setting	Bit 7	Digital volume control enable (0) / disable (1)
Byte 4	CODEC reg / start address	Bit 7~0	Reg addr(AC97) / three-wire reg 1 data[24:16] (24-bit), data[15:8] (16-bit)/EEPROM start address
Byte 5	CODEC reg data1	Bit 7~0	Reg 1 data[15:8] (16-bit AC97) / three-wire reg 2 data[15:8] (24-bit), data[7:0] (16-bit)/ EEPROM high byte data
Byte 6	CODEC reg data0	Bit 7~0	Reg 2 data[7:0] (AC97) / three-wire reg 3 data[7:0] (24-bit), reserved (16-bit)/ EEPROM low byte data
Byte 7	MCU byte 1	Bit 7~0	Two-wire serial port output register 1
Byte 8	MCU byte 2	Bit 7~0	Two-wire serial port output register 2
Byte 9	MCU byte 3	Bit 7~0	Two-wire serial port output register 3
Byte A	MCU byte 4	Bit 7~0	Two-wire serial port output register 4
Byte B	MCU byte 5	Bit 7~0	Two-wire serial port output register 5
Byte C	MCU byte 6	Bit 7~0	Two-wire serial port output register 6
Byte D	MCU byte 7	Bit 7~0	Two-wire serial port output register 7
Byte E	MCU byte 8	Bit 7~0	Two-wire serial port output register 8
Byte F	MCU byte 9	Bit 7~0	Two-wire serial port output register 9

Byte 0 :

Byte 0 is used to control the SPDIF port and GPIO/CODEC register accessing modes.
Bit 0 selects whether the SPDIF out port carries a normal audio stream or and AC-3 data stream.

Bit 1 selects if the output SPDIF stream can be copied.

Bit 2 enable/disable the SCMS setting of SPDIF stream.

Bit 3 selects if the output SPDIF stream should use the chip default setting or the values set in bit 0 to 2.

Bit 4 to 7 has two definitions, when the HID is used to control the GPIOs, they select the directions of GPIO pins. The settings of GPIO1, GPIO2 and GPIO3 control nothing of SN11220APF. When the HID is used to access the CODEC registers, they indicate the data length being read from/written to the CODEC. When the CODEC control interface is AC-link, the values of bit 4 to 7 have no meaning. When the CODEC control interface is three-wire, bit 4 to 7 indicates the total bit data length processed by the three-wire serial interface.

Bit 7 ~ 4	Total bit data length
0x00	0x09
0x01	0x0A
0x02	0x0B
0x03	0x0C
0x04	0x0D
0x05	0x0E
0x06	0x0F
0x07	0x10
0x08	0x11
0x09	0x12
0x0A	0x13
0x0B	0x14
0x0C	0x15
0x0D	0x16
0x0E	0x08
0x0F	0x18

When used as register bit length, bit 4 to 7 are only meaningful for HID programming CODEC and should be considered with bit 4 to 6 in byte 3 at the same time. When HID mode set 'program EEPROM', the bit 4 to 7 are ignored because this mode is fixed the format with 16-bit register value.

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Byte 1 :

Byte 1 is used to set the SPDIF category fields sent out by SN11220APF.

Byte 2 :

Byte 2 is used to set data to the register 0 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 3 :

Considering together with byte 0, byte 3 is used to control the GPIO ports and the CODEC interface of SN11220APF. Bit 0 to 3 is used to set the values of GPIO ports. Bit 4 to 6 is used to set the control mode of HID.

Bit 6 ~ 4	HID mode setting
000	Byte 0 bit 4 to 7 means reg length
001	HID program EEPROM
010	Don't use
011	Don't use
100	HID read EEPROM
101	GPIO control
110	HID program CODEC
111	HID read CODEC

HID program EEPROM:

Send 'Report Out' with Byte 4 (EEPROM address), Byte 5 (MSB) and Byte 6 (LSB).

HID read EEPROM:

Send 'Report Out' with Byte 4 (EEPROM address).

Get 'Report in' to read Byte 5 (MSB) and Byte 6 (LSB).

Bit 7 is used to disable the internal digital volume control feature of SN11220APF.

Byte 4 :

Byte 4 sets the register starting address for AC97 CODEC or the highest bytes of the three-wire serial port data.



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Byte 5 :

Byte 5 sets the high byte of register data for AC97 CODEC or the second bytes of the three-wire serial port data. When 'HID mode' set to program EEPROM, Byte 5 is set the programming high byte data [15:8].

Byte 6 :

Byte 6 sets the low byte of register data for AC97 CODEC or the third bytes of the three-wire serial port data. When 'HID mode' set to program EEPROM, Byte 6 is set the programming low byte data [7:0].

Byte 7 :

Byte 7 is used to set data to the register 1 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 8 :

Byte 8 is used to set data to the register 2 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte 9 :

Byte 9 is used to set data to the register 3 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte A :

Byte A is used to set data to the register 4 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte B :

Byte B is used to set data to the register 5 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte C :

Byte C is used to set data to the register 6 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte D :

Byte D is used to set data to the register 7 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte E :

Byte E is used to set data to the register 8 of the two-wire serial port of SN11220APF. Please refer to section VIII.

Byte F :

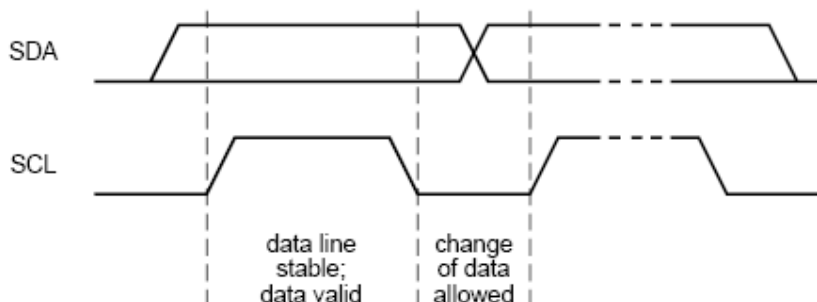
Byte F is used to set data to the register 9 of the two-wire serial port of SN11220APF. Please refer to section VIII.

VIII. Two-wire serial port definition

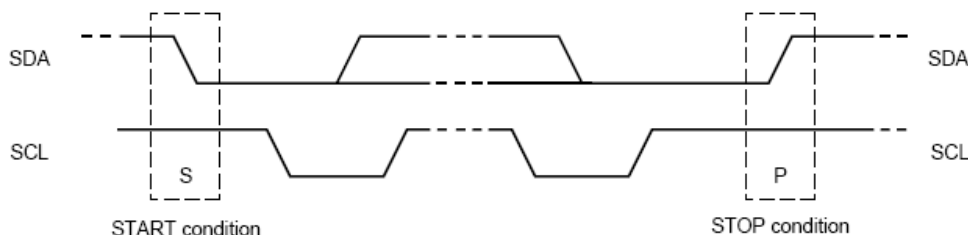
To provide extension capability, SN11220APF contains a two wire series bus circuitry as an interface to MCU. The two wire series bus serves as a slave device with bit rate up to 400Kbps (fast mode) . MCU can write ten bytes to the SN11220APF with 8-bit register address 0x38. MCU can also read ten bytes from SN11220APF with 8-bit register address 0x39.

This section just provides simple description of the two-wire series bus. It is compatible with the I²C slave mode. User can get more detail explanation form the I²C specification.

The input pin “SCL” is used to get the two wire series bus clock form MCU, and the open-drain output pin “SDA” is used to send or receive serial signal to/from MCU. As shown below, “SDA” should be stable when “SCL” is high, and can have transition only when “SCL” is low.

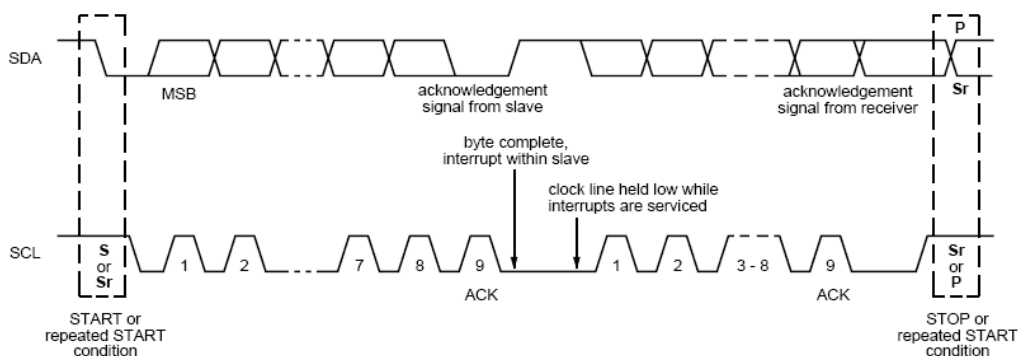
Bit transfer on the I²C-bus.

START and STOP conditions shown below are the exception. Every transaction begins from a START, and ends with a STOP, or another START (repeated START).

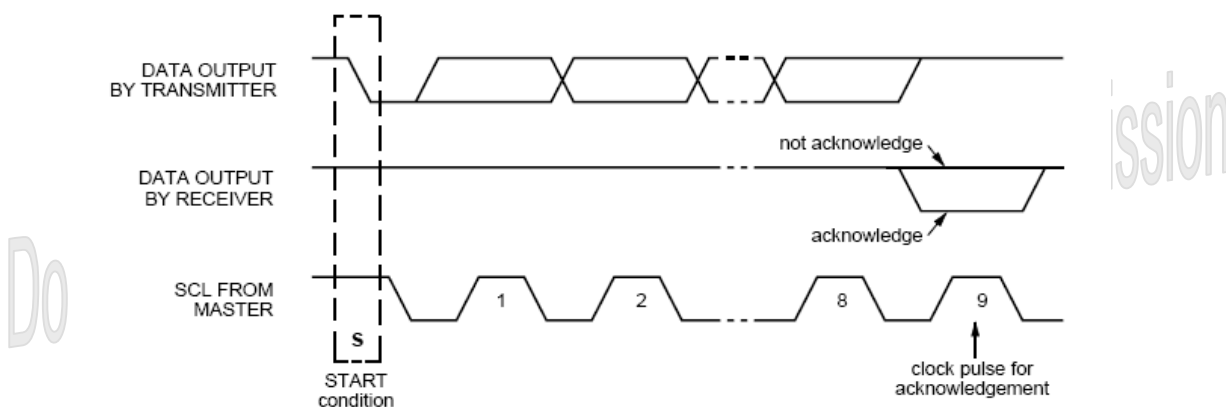


START and STOP conditions.

The figure below demonstrates a typical two-wire serial bus transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement, a STOP or repeated START should follow. The next figure shows more detailed about acknowledgement bit. Note that “SCL” is always driven by the master.



Data transfer on the I²C-bus.



Acknowledge on the I²C-bus.

The figure below shows a complete data transfer. After a STRAT, MCU should send 7-bit slave address (7'b0011100) first, and then the 8th bit denotes a read transfer when it's 1 ; or a write transfer when it's 0.

Note that address 0x0b is the indicator to notice SN11220APF to update the data written by MCU to PC via USB HID. Writing any thing to address 0x0b means the SN11220APF can transfer all the data to PC. Before address 0x0b be written, SN11220APF will transfer the last data which the last indicator launched.

SN11122 READ :

S	Slave Addr (R)	A	D0	\bar{A}	P
---	----------------	---	----	-----------	---

New READ :

S	Slave Addr (\bar{W})	A	Pointer	A	Sr	Slave Addr (R)	A	D0	A	D1	A	D2	A	D3	A	D4	A	D5	A	D6	A	D7	A	D8	A	D9	\bar{A}	P
---	--------------------------	---	---------	---	----	----------------	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	-----------	---

NOTE:

1. S : START
2. Sr : Repeated START
3. Slave Addr (\bar{W}) : Slave Address (Write) = 0x38
4. Slave Addr (R) : Slave Address (Read) = 0x39
5. Pointer : Register0 Pointer = 0x00
6. A : Acknowledge
7. \bar{A} : Not Acknowledge
8. D0 : Data Length (Byte0)
9. D1 ~ D8 : Data (Byte1 ~ Byte8)
10. D9 : Rolling Code (Byte9)
11. P : STOP
12. ☒ : From Master to Slave
13. ☐ : From Slave to Master

READ

SN11122 WRITE :

S	Slave Addr (\bar{W})	A	Pointer	A	D0	A	D1	A	P
---	--------------------------	---	---------	---	----	---	----	---	---

New WRITE :

S	Slave Addr (\bar{W})	A	Pointer	A	D0	A	D1	A	D2	A	D3	A	D4	A	D5	A	D6	A	D7	A	D8	A	D9	A	DA	A	DB	A	P
---	--------------------------	---	---------	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	----	---	---

NOTE:

1. S : START
2. Slave Addr (\bar{W}) : Slave Address (Write) = 0x38
3. Pointer : Register0 Pointer = 0x00
4. D0 : Data Length (Byte0)
5. D1 ~ D8 : Data (Byte1 ~ Byte8)
6. D9 : Rolling Code (Byte9)
7. DA ~ DB : Dummy Byte (ByteA ~ ByteB)
8. A : Acknowledge
9. P : STOP
10. ☒ : From Master to Slave
11. ☐ : From Slave to Master

WRITE

IX. Operating rating and electrical characteristics

9.1 Absolute maximum rating

Symbol	Parameter	value	unit
Dvmin	min digital supply voltage	DGND – 0.3	V
Dvmax	max digital supply voltage	DGND + 3.6	V
Avmin	min analog supply voltage	AGND – 0.3	V
Avmax	max analog supply voltage	AGND + 3.6	V
Dvinout	voltage on any digital input or output pin	DGND –0.3 to 3.6	V
Avinout	voltage on any analog input or output pin	AGND –0.3 to Avdd + 0.3	V
T _{stg}	storage temperature range	-40 to +125	°C
ESD (HBM)	ESD human body mode	2000	V
ESD (MM)	ESD machine mode	200	V
I _{latch}	minimum latch up current	200	mA

9.2 Operation conditions

Symbol	Parameter	value	unit
DVdd	digital supply voltage	+3.3 (typ)	V
Avdd	analog supply voltage	+3.3 (typ)	V
T _A	operating ambient temperature range	25 (typ)	°C

9.3 DC electrical characteristics

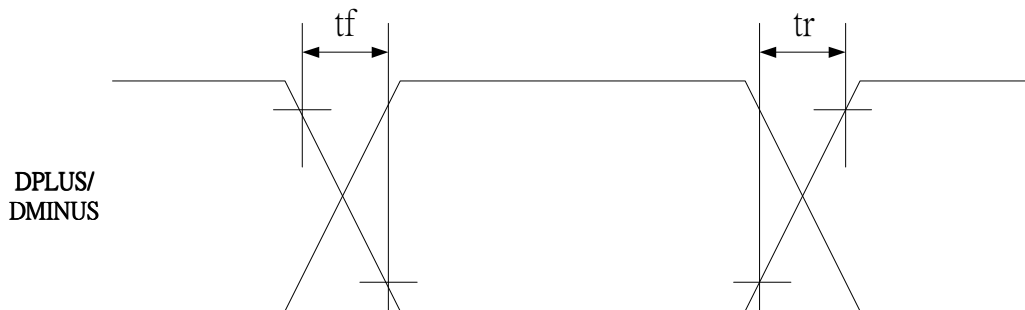
Symbol	parameter	test condition	Value	unit
V_{DI}	differential input sensitivity	$ (D+) - (D-) $	0.2 (min)	V
V_{CM}	differential common mode range	Included V_{DI} range	0.8 (min) 2.5 (max)	V
V_{SE}	single ended receiver threshold		0.8 (min) 2.0 (max)	V
V_{IH}	high level input voltage		2.0 (min)	V
V_{IL}	low level input voltage		0.8 (max)	V
I_{OH}	drive current	$V_{OH} = 2.3V$	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{OL}	sink current	$V_{OL} = 0.5V$	4 (typ) for 4mA pads 8 (typ) for 8mA pads	mA
I_{DD}	input supply current		30 (max)	mA
$I_{suspend}$	supply current in suspend		300 (max)	μA

9.4 AC electrical characteristics

9.4.1 Operation clocks

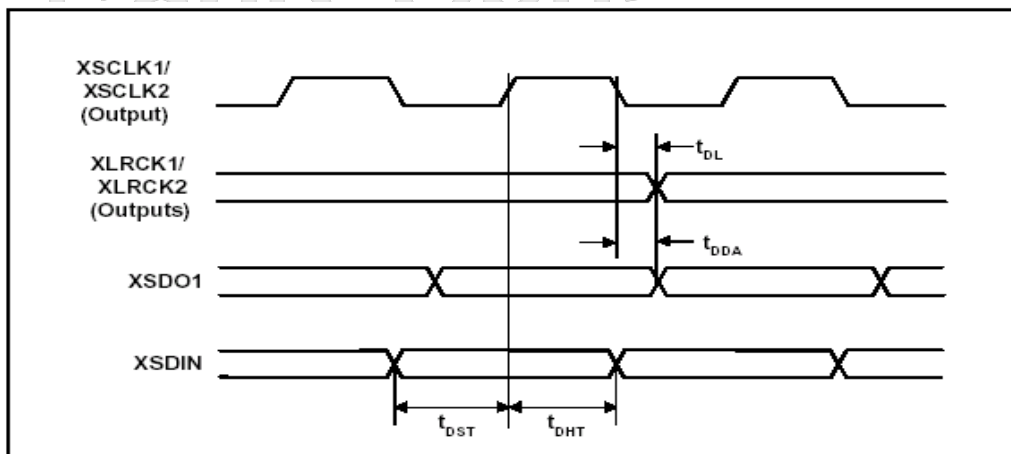
symbol	parameter	value	unit
CLKin	system clock input to PLL	6 (typ)	MHz
	CLKin duty cycle	50 ± 2	%

9.4.2 USB transceiver signal (full speed mode)



symbol	parameter	test condition	Min	max	unit
Tr	transition rise time for USBDP or USBDM		4	20	ns
Tf	transition fall time for USBDP or USBDM		4	20	ns
Trfm	rise / fall time matching	(Tr / Tf) * 100	90	110	%
Vo(crs)	signal crossover voltage		1.3	2.0	V

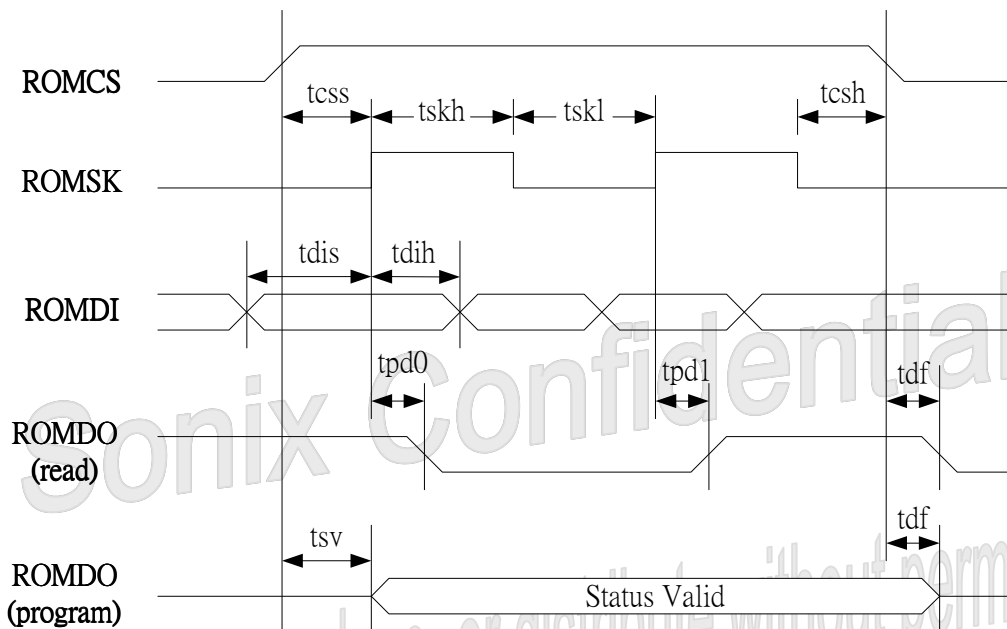
9.4.3 I²S CODEC interface timing



Fs = 48kHz, XMCLK1/XMCLK2 = 256fs, XSCLK1/XSCLK2 = 64fs

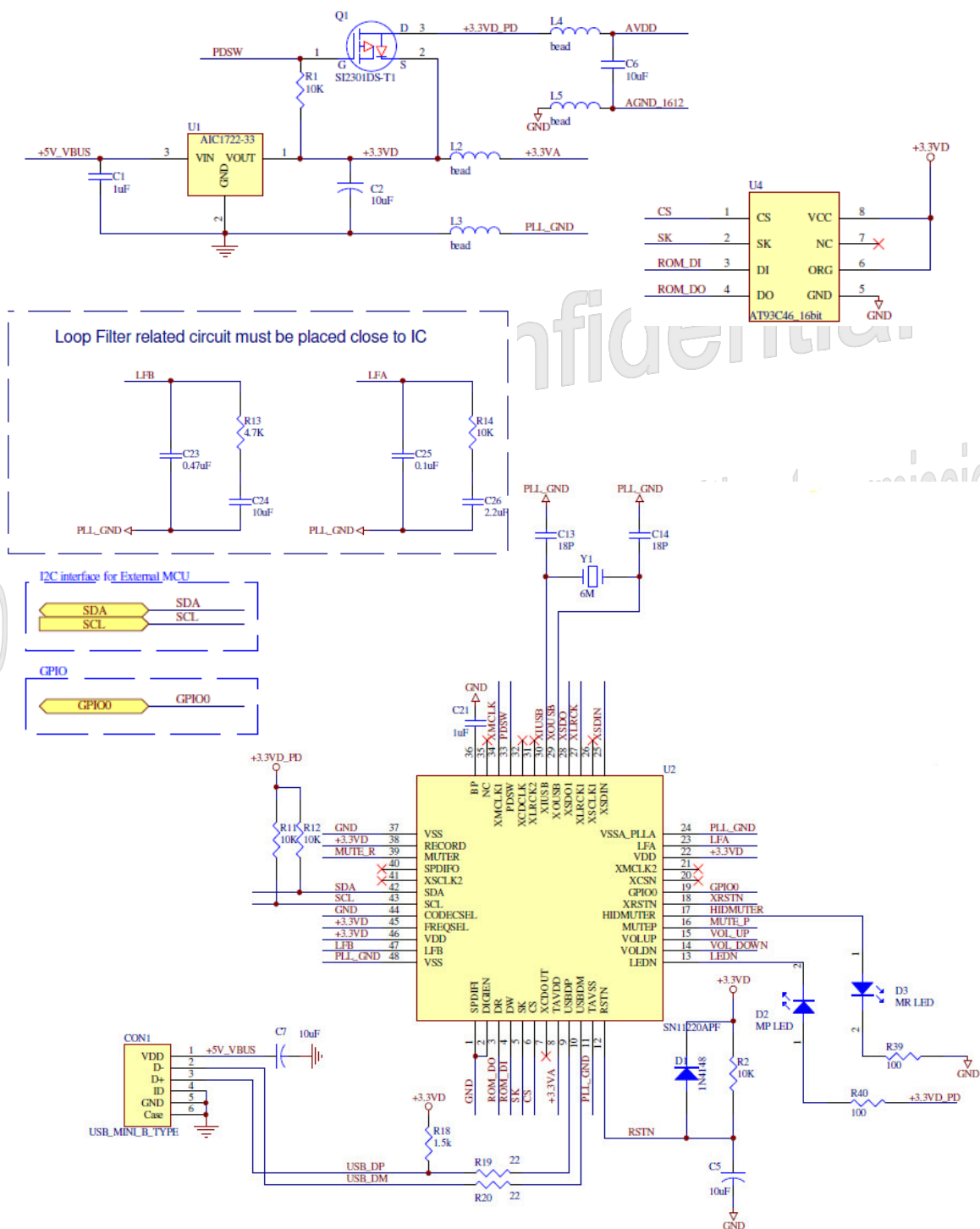
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
XLRCK1/XLRCK2 propagation delay from XSCLK1/XSCLK2 falling edge	t _{DL}		0		10	ns
XSDO1 propagation delay from XSCLK1 falling edge	t _{DDA}		0		10	ns
XSDIN setup time to XSCLK2 rising edge	t _{DST}		10			ns
XSDIN hold time from XSCLK2 rising edge	t _{DHT}		10			ns

9.4.4 EEPROM Interface



symbol	parameter	min	typ	max	unit
tsk	ROMSK clock frequency	-	400	-	kHz
tskh	ROMSK high time		1200		ns
tskl	ROMSK low time		1200		ns
tcs	Minimum ROMCS low time		2400		ns
tcss	ROMCS setup time		2400		ns
tdis	ROMDI setup time		1200		ns
tcsch	ROMCS hold time		1200		ns
tdih	ROMDI hold time		1200		ns
tpd1	ROMDO delay to "1"			250	ns
tpd0	ROMDO delay to "0"			250	ns
tsv	ROMCS to status valid			250	ns
tdf	ROMCS to ROMDO high impedance			250	ns

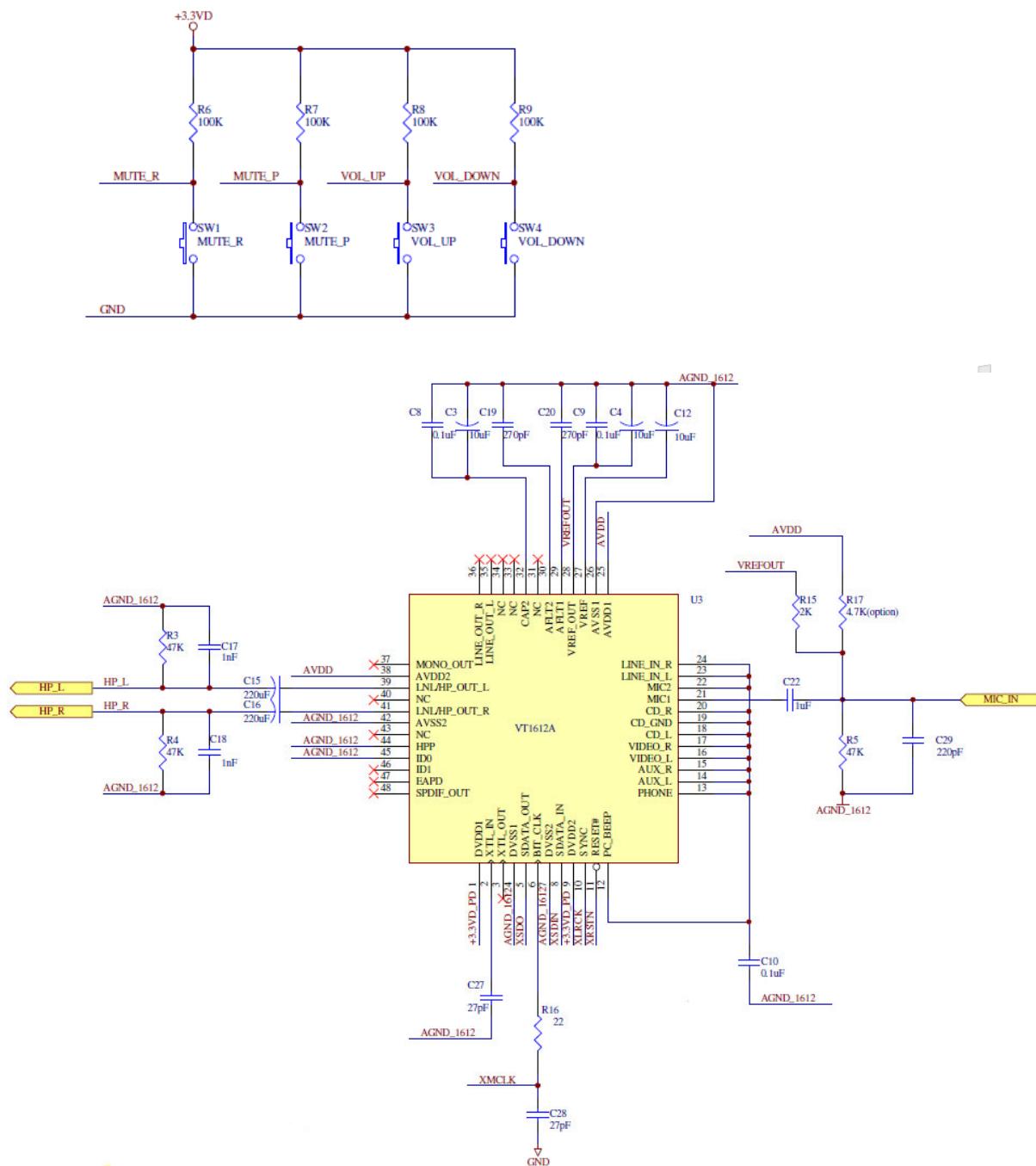
X. Reference design:





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XI. Naming rule

(1)		(2)					(3)	(4)	(5)	(6)
S	N	1	1	2	2	0	A	P	F	

(1) SONiX chip

(2) USB audio controller 11220 series

(3) Hardware version

A: The first version, B: The second version, C: The third version, etc.

(4) Series code

Series Code	Name	Description
C	DECT	I ² S, PCM interface and for DECT solution. No 3-wire control pin. One frequency mode.
P	Public	I ² S, AC'97 and S/PDIF. Support different sampling rate to playback and recording.

(5) Package type

Package type	Description
F	LQFP

(6) Green Package

Green Package	Description
G	It achieve the requirement of SS-00259 (level-3)
R	It achieve the requirement of SS-00259 (level-3)
	Non-green package

(7) Date code

(a)		(b)	(c)	(d)		(e)	(f)	(g)
Y	Y	M	D	A	O	V_B	V_O	S

(a) “Y” for year; 2003=“03”

(b) “M” for month; 1~9, A=10, B=11, C=12

(c) “D” for days; 1~9, A=10, B=11, C=12, D=13 ...

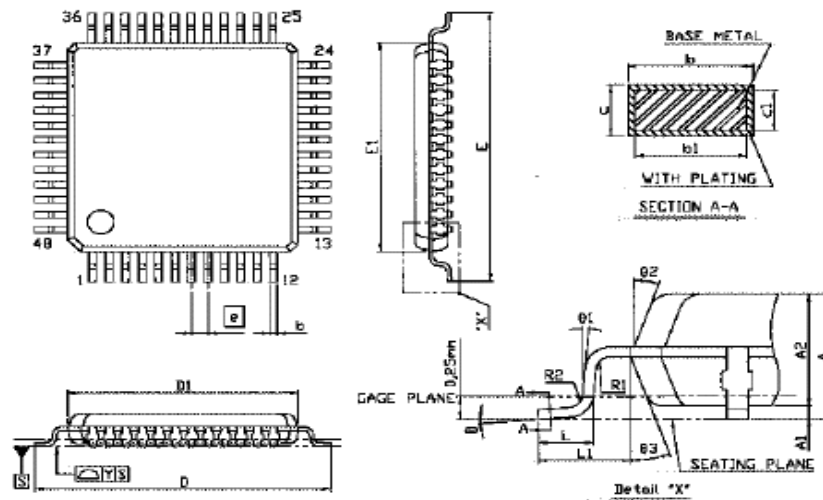


- (d) "A", "O" SONIX internal used.
- (e) "V_B" body reversion, for example 0, 1, 2, 3...etc.
- (f) "V_O" SONIX internal used.
- (g) "S" serial number.

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XII. Package dimension



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
W	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	100 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:

1. REFER TO JEDEC MS-026/BBC

2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION, INCLUDING MOLD MISMATCH.

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

4. ALL DIMENSIONS IN MILLIMETERS.



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Revision History

Revision	Revision Date	Description of changes
Preliminary	Dec 20, 2005	Preliminary
V1.0	July 20, 2006	Detail description Add section 10 Add section 11
V1.01	July 27, 2007	1. Feature description is modified to read easily. 2. Pin12 description. In page 5. 3. Pin35, Pin36 pin name and description. In page 6. 4. Block diagram description. Embed regulator used is not recommend. In page7. 5. Modify X. Reference design 6. Modify XI. Item4 series R is removed.
V1.02	Sep 6, 2007	VII. HID bytes arrangement: Add detail explain of EEPROM read and program by <u>Report in</u> and <u>Report out</u>
V1.03	Aug 5, 2009	1. Modify X. Reference design 2. Add XI. Naming rule (7)



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