SN11112

USB AUDIO CONTROLLER

Data Sheet

2001 Aug 17th, Version 1.05

I. Description

SONiX SN11112 is an USB audio controller. It supports 32KHz (which needs driver or application software support), 44.1KHz or 48KHz sampling rate in digital recording; 48 KHz sampling in analog recording; and 48KHz in digital/analog audio playback.

In digital playback mode, it receives audio stream from PC via USB interface and transmits audio data according to the AES/EBU, IEC60958, S/PDIF consumer interface standards. In analog playback mode, it supports AC 97 Codec for analog playback.

In digital recording mode, it receives S/PDIF digital audio input and sends back to PC through USB. Three sampling rates; includes 32 KHz, 44.1 KHz, and 48 KHz; are automatically locked internally. In analog recording mode, fixed 48 KHz sampling rate is supported by analog audio recording.

Totally one control pipe, two isochronous pipes, and one interrupt pipe are supported by SN11112.

II. Features

- Supports AES/EBU, IEC60958, S/PDIF consumer formats for stereo PCM data
- Fixed 48KHz sampling rate for 2 channel stereo playback
- Supports digital recording function with 32KHz, 44.1KHz and 48KHz sampling rate
- Supports analog recording function with fixed 48KHz sampling rate
- Supports SCMS (Serial Copy Management System) copy protection
- Full-duplex playback/ recording audio stream without sound card in PC
- Compatible with Win98 SE/ WinME/ Win2000/ WinXP beta2 and MacOS 9.1 without additional driver
- Plug-and-Play operation with Windows default drivers
- Compliant with USB specification v1.1
- Compliant with USB audio device class specification v1.0
- Supports USB full speed 12Mbits/s serial data transmission
- USB bus power or self power option
- Supports suspend/resume and remote wake-up
- 6MHz crystal input with on-chip PLL and embedded transceiver for USB
- USB audio function topology has three input terminals, three output terminals, one selector unit, one mixer unit, and four feature units

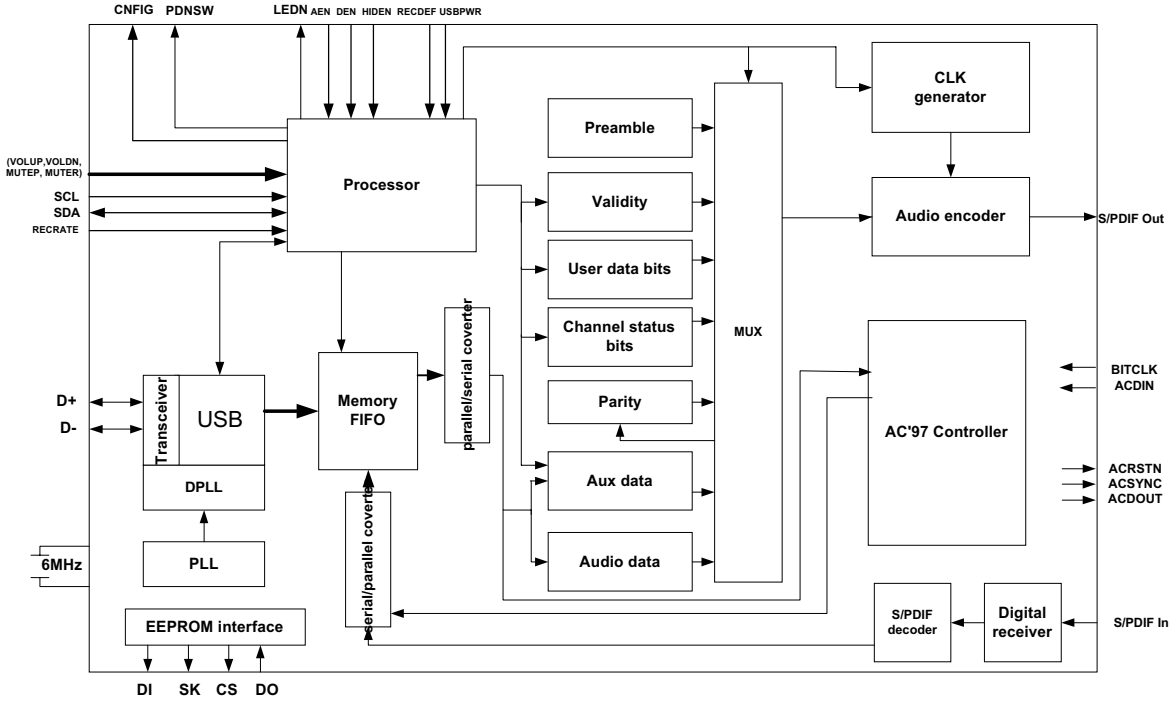
- Alternate setting0 is a zero-bandwidth setting; used to release the claimed bandwidth on the bus when this device is inactive
- Isochronous transfer uses adaptive and asynchronous synchronization
- Supports AC'97 component specification v2.1; AC link interface for external AC97 audio Codec
- Compliant with USB HID class specification v1.1; pin control for volume up / down, play mute, and record mute
- Supports two wire series bus interface; slave only interface with transfer speed up to 400Kbps(Fast-mode)
- EEPROM interface for customized USB IDs and Codec programming
- 3.3 V core operation and 5 V tolerant I/O
- Available in 64-pin LQFP(10x10 mm) and 64-pin TQFP(10x10 mm)
- System on chip solution: low cost and easy implementation without external memory
- LED indicator pin
- Features programmable by jumper pins

III. Ordering information

SN11112F : 64-pin LQFP (10x10x1.4 mm)

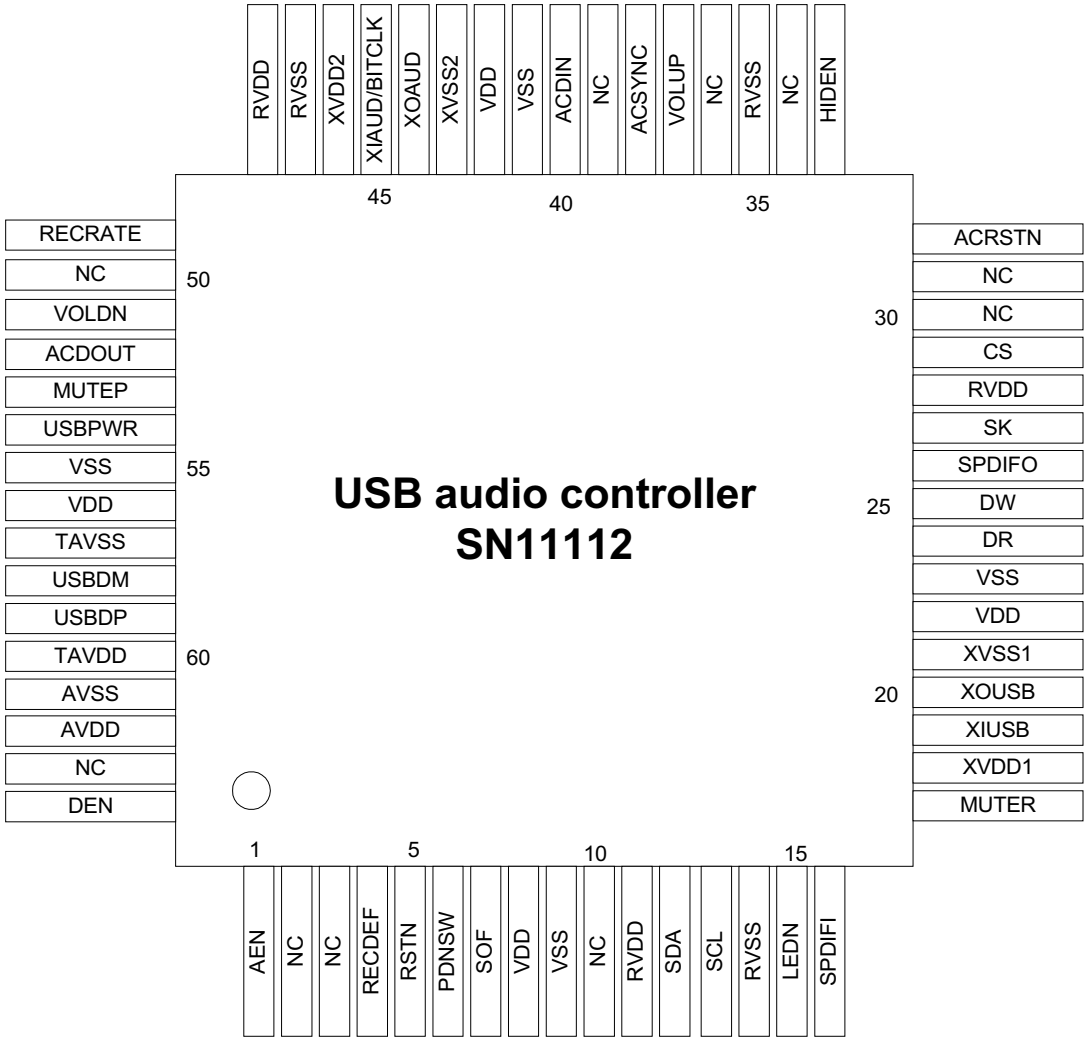
SN11112T : 64-pin TQFP (10x10x1.0 mm)

IV. Block diagram



V. Pin description

5.1 SN11112 pin chart (64-pin LQFP/TQFP)



5.2 pin assignment and description (64-pin LQFP/TQFP)

Pin No.	Pin Name	Pin Type	Description
1	AEN	I, ST	Analog playback and recording function on (=1)
2	NC		
3	NC		
4	RECDEF	I, ST	0: default is digital recording 1: default is analog recording
5	RSTN	I, ST, PU	System reset pin, pull low to reset
6	PDNSW	O, 4mA, SR	Power down switch control -- 0: normal mode, 1: power down mode

7	SOF	O, 4mA, SR	USB SOF (Start of Frame) pin output which provides 1KHz signal
8	VDD	P	Power pin
9	VSS	P	Power pin
10	NC		
11	RVDD	P	Power pin for pad
12	SDA	I/O, 4mA, SR	Two wire series bus data pin for external MCU control
13	SCL	I, ST	Two wire series bus clock pin for external MCU control
14	RVSS	P	Power pin for pad
15	LEDN	O, 8mA, SR	LED indicator pin, output low after power on reset, toggle during operation
16	SPDIFI	I, ST	Input pin for SPDIF signal
17	MUTER	I, ST	Recording mute, edge trigger with 64ms de-bouncing circuit
18	XVDD1	P	Power pin for USB external crystal
19	XIUSB	I	6 MHz clock osc pad for USB PLL
20	XOUSB	O	6 MHz clock osc pad for USB PLL
21	XVSS1	P	Power pin for USB external crystal
22	VDD	P	Power pin
23	VSS	P	Power pin
24	DR	I, ST	EEPROM data input Fixing this pin to H or L sets USB vendor ID to SONiX USB vendor ID (hex 0C45); PU or PD is used for different product ID
25	DW	O, 4mA, SR	EEPROM data output
26	SPDIFO	O, 8mA, SR	SPDIF data output
27	SK	O, 4mA, SR	EEPROM clock pin
28	RVDD	P	Power pin for pad
29	CS	O, 4mA, SR	EEPROM chip select
30	NC		
31	NC		
32	ACRSTN	O, 4mA, SR	AC'97 Codec reset
33	HIDEN	I, ST	USB HID function on(=1)
34	NC		
35	RVSS	P	Power pin for pad
36	NC		
37	VOLUP	I, ST	Volume up control, edge trigger with 64ms de-bouncing circuit
38	ACSYNC	O, 4mA, SR	AC'97 Codec sync (48 kHz) signal
39	NC		
40	ACDIN	I, ST	AC'97 Codec serial data input
41	VSS	P	Power pin
42	VDD	P	Power pin
43	XVSS2	P	Power pin for external crystal
44	XOAUD	O	12.288 MHz Crystal output
45	XIAUD/BITCLK	I, ST	12.288 MHz Crystal input / AC' 97 Codec BIT clock input
46	XVDD2	P	Power pin for external crystal
47	RVSS	P	Power pin for pad
48	RVDD	P	Power pin for pad
49	RECRATE	I, ST	Digital mode recording sampling rate 1: 48KHz , 0: 44.1KHz
50	NC		
51	VOLDN	I, ST	Volume down control, edge trigger with 64ms de-bouncing circuit
52	ACDOUT	O, 4mA, SR	AC'97 Codec serial data

53	MUTEP	I, ST	Playback mute control pin, edge trigger with 64ms de-bouncing circuit
54	USBPWR	I, ST	USB power mode -- 0: bus power 1: self power
55	VSS	P	Power pin
56	VDD	P	Power pin
57	TAVSS	P	Power pin for USB transceiver
58	USBDM	I/O	USB data minus
59	USBDP	I/O	USB data plus
60	TAVDD	P	Power pin for USB transceiver
61	AVSS	P	Power pin for PLL
62	AVDD	P	Power pin for PLL
63	NC		
64	DEN	I, ST	Digital playback and recording function on (=1)

** All input pin are 5 volt tolerance, TTL level and Schmitt trigger

All output pins are slew rate control

I – input pad , O – output pad, P – power pad, ST – Schmitt trigger, SR – slew rate control, PU/PD – pull up or pull down

VI. Operating rating and electrical characteristics

6.1 Absolute maximum rating

symbol	Parameter	value	unit
Dvmin	min digital supply voltage	DGND – 0.3	V
Dvmax	max digital supply voltage	DGND + 4.6	V
Avmin	min analog supply voltage	AGND – 0.3	V
Avmax	max analog supply voltage	AGND + 4.6	V
Dvinout	voltage on any digital input or output pin	DGND –0.3 to 5.5	V
Avinout	voltage on any analog input or output pin	AGND –0.3 to Avdd + 0.3	V
T_{stg}	storage temperature range	-40 to +125	^{0}C
ESD (HBM)	ESD human body mode C=100pF, R=1.5KΩ	5000	V
ESD (MM)	ESD machine mode	20 0	V
I_{off}	leakage current	10	uA
I_{latch}	minimum latch up current	100	mA

6.2 Operation conditions

symbol	parameter	value	unit
DVdd	digital supply voltage	+3 to +3.6	V
Avdd	analog supply voltage	+3 to +3.6	V
T_A	operating ambient temperature range	0 to 70	^{0}C
T_J	operating junction temperature range	0 to 115	^{0}C

6.3 DC electrical characteristics

symbol	parameter	test condition	value	unit
V_{DI}	differential input sensitivity	| (D+) – (D-) |	0.2 (min)	V
V_{CM}	differential common mode range	Included V_{DI} range	0.8 (min) 2.5 (max)	V
V_{SE}	single ended receiver threshold		0.8 (min) 2.0 (max)	V
V_{IH}	high level input voltage		2.0 (min)	V
V_{IL}	low level input voltage		0.8 (max)	V
V_{OH}	high level output voltage	I_{OH} = -4 mA	2.0 (min)	V
V_{OL}	low level output voltage	I_{OL} = 4 mA	0.8 (max)	V
I_{IL}	low level input current	V_I = 0 V	RSTN pin : - 50.0 (max) the other pins : - 3.0 (max)	µA

I_{IH}	high level input current	V_I = 3.6 V	SPDIFI, XSDIN pins : 50.0 (max) the other pins : 3.0 (max)	µA
I_{DD}	input supply current		20 (max)	mA
Isuspend	supply current in suspend		20 (max)	µA

6.4 AC electrical characteristics

6.4.1 USB transceiver signal (full speed mode)

symbol	parameter	test condition	min	max	unit
Tr	transition rise time for DP or DM		4	20	ns
Tf	transition fall time for DP or DM		4	20	ns
Trfm	rise / fall time matching	(Tr / Tf) * 100	90	110	%
Vo(crs)	signal crossover voltage		1.3	2.0	V

6.4.2 Operation clocks

symbol	parameter	value	unit
CLKin	XIAUD/XOAUD crystal value BITCLK serial data clock	12.288 (typ)	MHz
	CLKin duty cycle	50 ± 2	%
USBCLKin	XIUSB/XOUSB crystal value	6 (typ)	MHz
	USBCLKin duty cycle	50 ± 2	%

6.4.3 External EEPROM interface

symbol	parameter	value	unit
Fsk	SK pin clock frequency	200	kHz

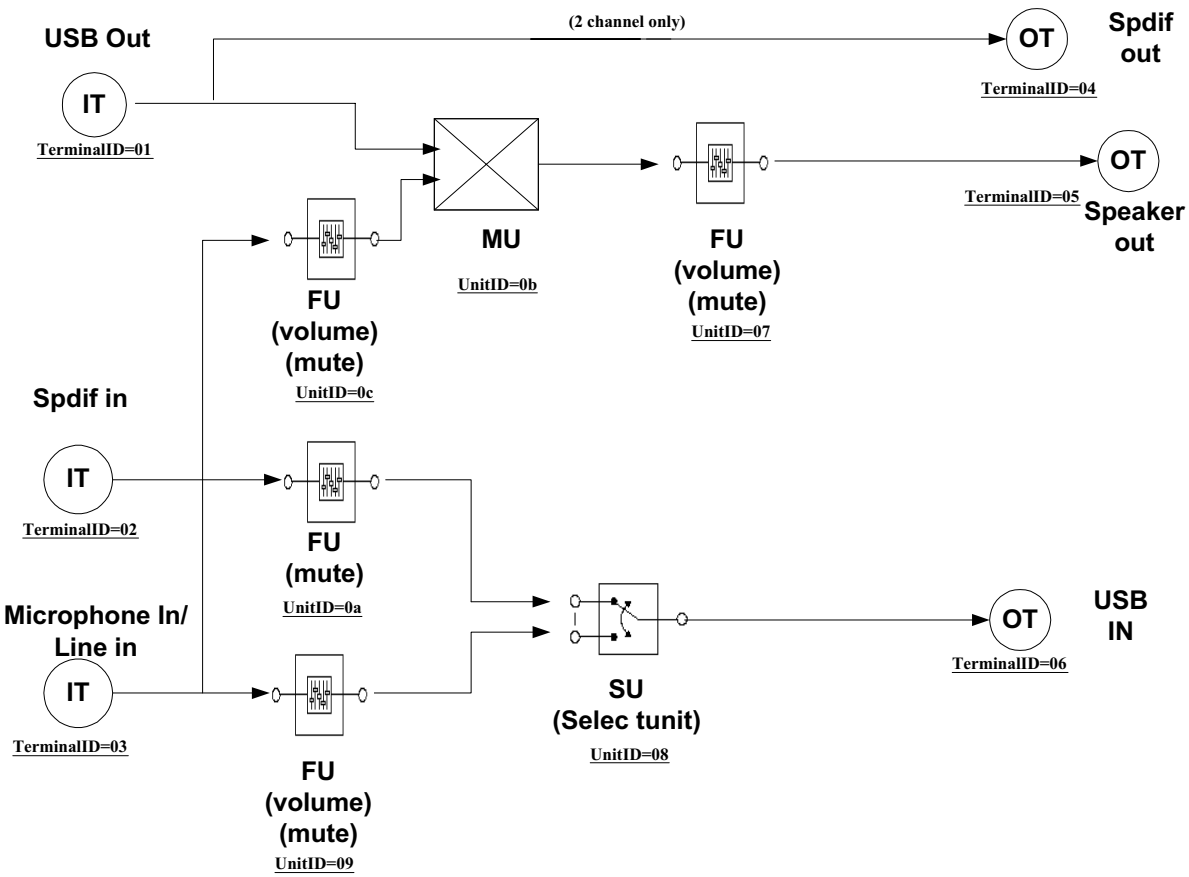
6.4.4 AC'97 Audio Codec interface timing

Please refer to AC'97 component specification ver2.1

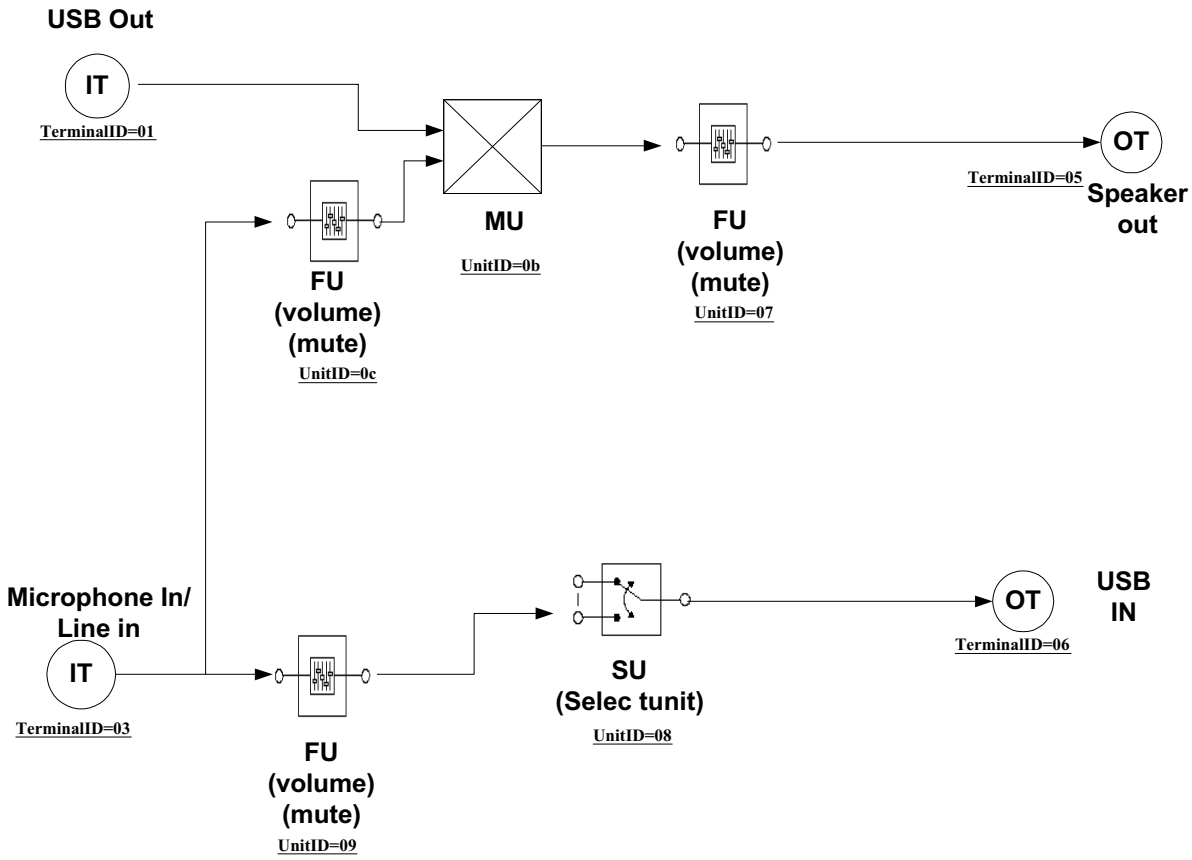
VII. Function and control register description

7.1 Controller topology

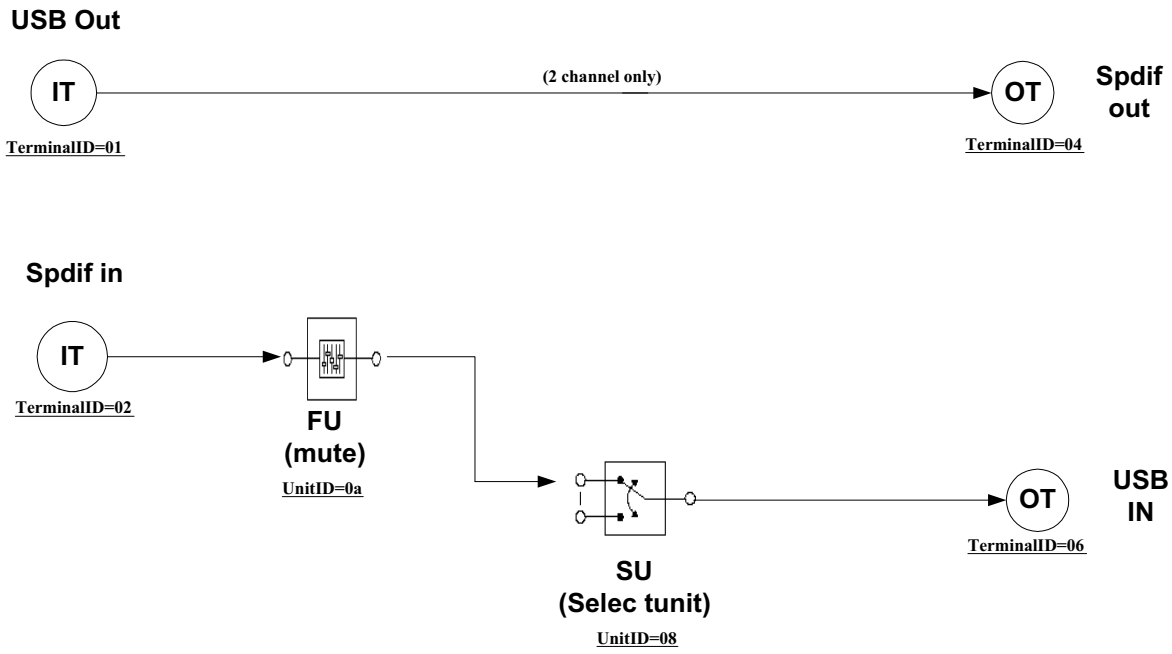
(a) AC-97 analog / digital playback and recording



(b) AC-97 analog playback and recording only



(c) AC-97 digital playback and recording only



7.2 Topology setting and button function

7.2.1 Topology setting

pin / Topology	**AEN** (analog playback and recording function)	**DEN** (digital playback and recording function)	**HIDEN** (HID function)	**RECRATE** (recording sampling rate in digital mode)
(a) AC-97 full set	1	1	1/0	DON'T CARE Recording : fixed 48KHz
(b) AC-97 analog	1	0	1/0	DON'T CARE Recording : fixed 48KHz
(c) AC-97 digital	0	1	0	Playback : 48 KHz Recording : 1 : 48 KHz 0 : 44.1 KHz

'HIDEN' pin is used to enable/disable button feature which uses USB HID(Human Interface Devices). In AC-97 digital mode, 44.1KHz sample rate for recording can be supported by pull-down 'RECRATE' pin.

7.2.2 button function

The SN11112 has four buttons to control playback and recording volume. It supports volume up, volume down, play mute, and recording mute. Button function is only effective in analog terminal. 1M pull-up resistors connected to 3.3V are recommended for these pins.

7.2.3 LED indicator

A LED pin is used to indicate the operation condition. It is flashing in a 256ms period during playback and recording.

7.2.4 SOF pin

SOF pin provides a 1 KHz signal output which comes from USB 1 ms frame rate. With external circuit, it can be used for a reference for USB synchronization.

7.3 Fixed sample rate codec configuration

It can support 48KHz sample rate for playback and recording

Alternate setting for playback channel:

Alternate setting 0 : zero bandwidth

Alternate setting 1 : Adaptive synchronization, 16-bit PCM stereo

Alternate setting for recording channel:

Alternate setting 0 : zero bandwidth

Alternate setting 1 : Asynchronous synchronization, 16-bit PCM stereo

(In AC-97 digital mode, it can supports 44.1KHz sample rate for recording by pull-down RECRATE pin)

7.4 Audio output

SN11112 supports 16-bit stereo PCM audio data output at 48KHz sample rate. The audio data sent from USB is sent to both SPDIF out terminal (digital out) and Speaker out terminal (analog out). AC'97 Codec can be used at the Speaker out terminal to get analog audio sound.

7.5 Audio input

SN11112 can record 16~24 bits stereo PCM audio data at 32, 44.1 and 48KHz sample rate via S/PDIF input. It converts incoming audio data format to 16 bits PCM data. In digital recording, SN11112 supports SCMS (serial copy management system); if incoming digital audio data has copyright protection enabled, it will not record this audio data and send silent audio data to PC.

Because the digital audio data has its original data format (16~24bits) and sample rate, sample rate in recording software on PC should be set as the same rate when user wants to record this digital audio data. For analog audio data recording, recording sample rate is fixed at 48KHz.

7.6 EEPROM data storage pattern

EEPROM address	High byte (MSB to LSB)	Low byte (MSB to LSB)	remark
0	idVendor high byte	idVendor low byte	
1	idProduct high byte	idProduct low byte	
2	Control word high byte	Control word low byte	Refer to the next table
3			Programming data
4			Programming data
5			Programming data
6			Programming data

** 16 bit per word at each address

control word (address 02)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	cdcreg	R	R	R	R	R	Chk7	Chk6	Chk5	Chk4	Chk3	Chk2	Chk1	Chk0

bit 15, bit 14 R – reserved

bit 13 cdcreg – 0: not default register value for Codec, programming by SN11112

1: using SN11112 built-in programming value for Codec

bit 12 – bit8 R – reserved

bit 7 – bit 0 Chk(7:0) – EPROM magic code (Hex AB), used to check EEPROM existence

Starting from word 3 – programming data

- AC97 Codec (sequence and number are fixed)

Word 3 – master volume data

Word 4 – line in volume data

Word 5 – PCM out volume data

Word 6– record gain data

default setting for each Codec (when bit 13 in control word is set to 1 so programming data is ignored)

AC97

address	Setting value
02	0000
10	8808
18	0808
1C	0000
others	Codec default setting

* If no Codec is connected, input pin “ACDIN” must be tied to high.

EEPROM read sequence:

idVendor (MSB to LSB) → idProduct (MSB to LSB) → Control word → Programming data …

7.7 SPDIF

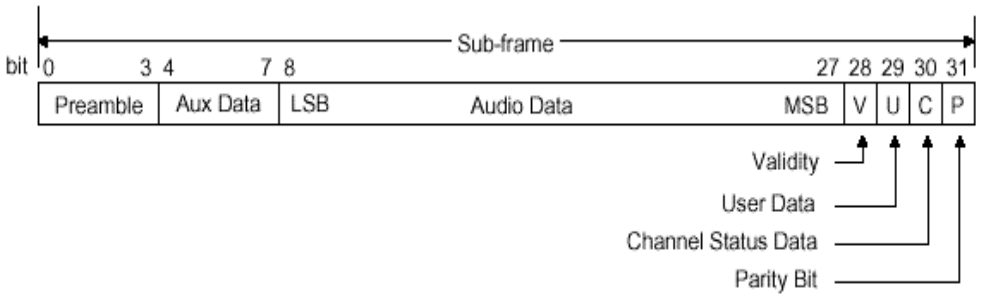


Figure 1. Sub-frame Format

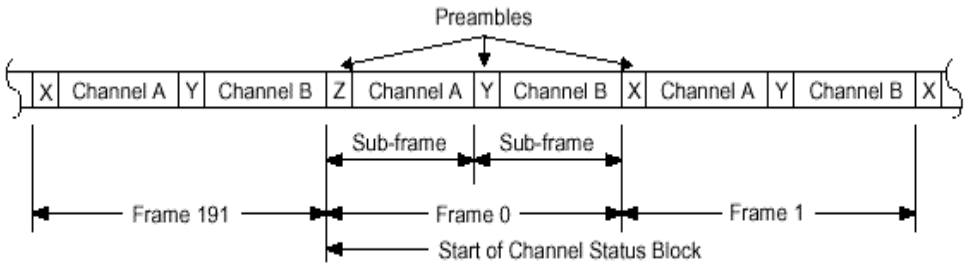


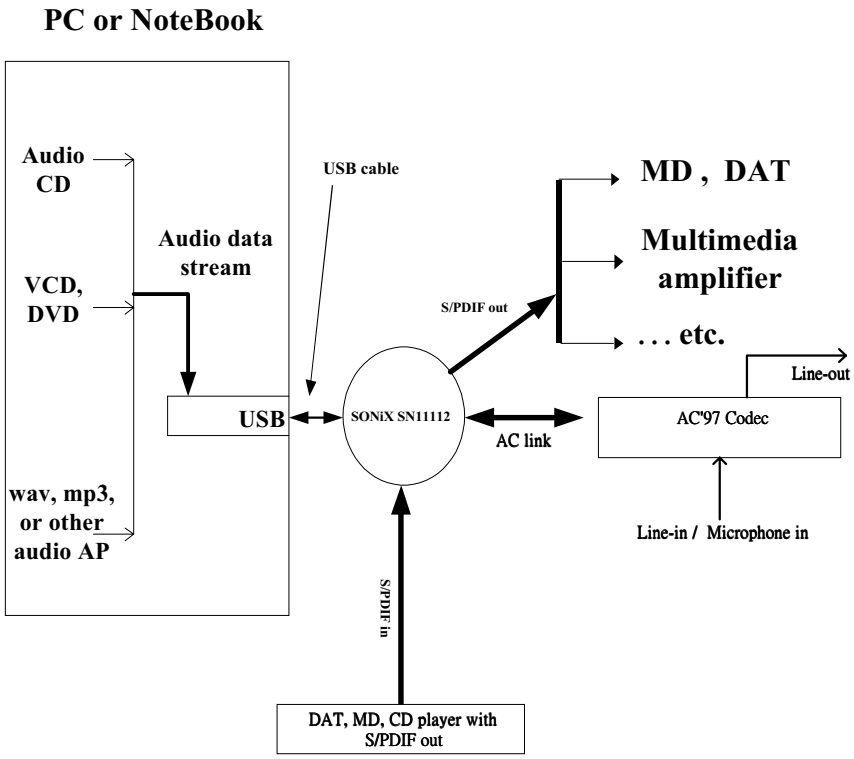
Figure 2. Frame/Block Format

SPDIF Channel Status Block Structure

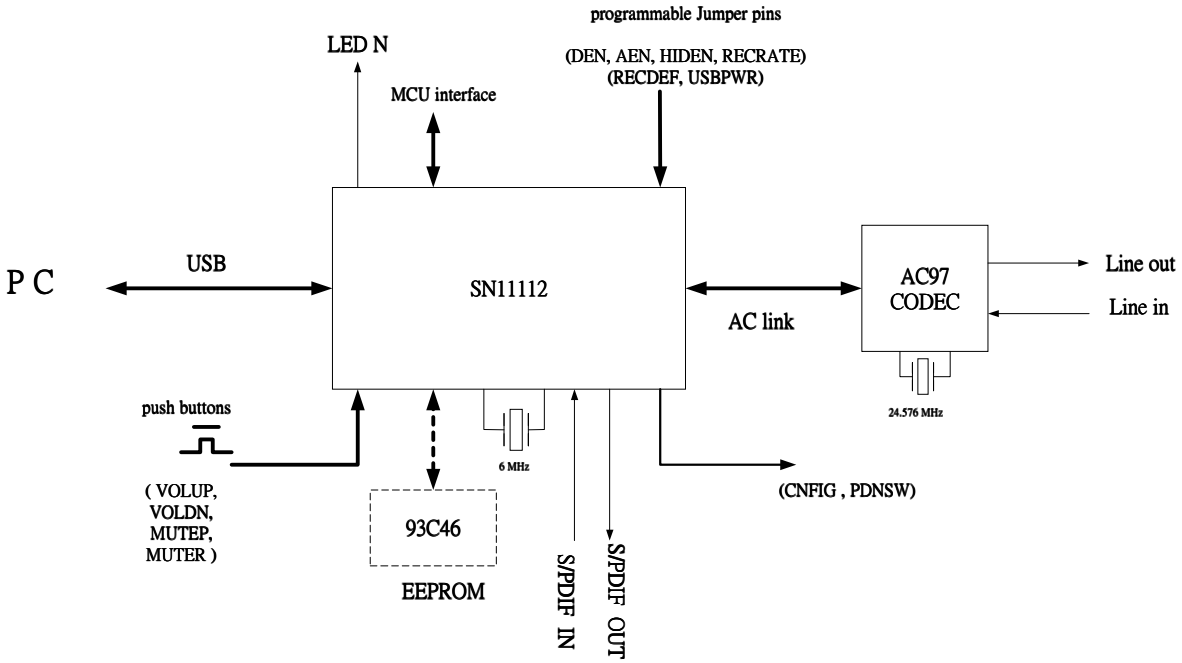
	bit0	bit1	bit2	bit3	bit4	bit5	bit6	bit7	
Byte0	consumer	audio	copy	emphasis			mode		
	0	0	1	0	0	0	0	0	
Byte1	category code							L	
	0	0	0	0	0	0	0	0	
Byte2	source number				channel number				
	1	0	0	0	1	0	0	0	(A channel)
					0	1	0	0	(B channel)
Byte3	sampling frequency				clock accuracy		reserved		
48KHz	0	1	0	0	0	0	0	0	
Byte4	word length								
	0	0	0	0					

VIII. Application

8.1 Application example

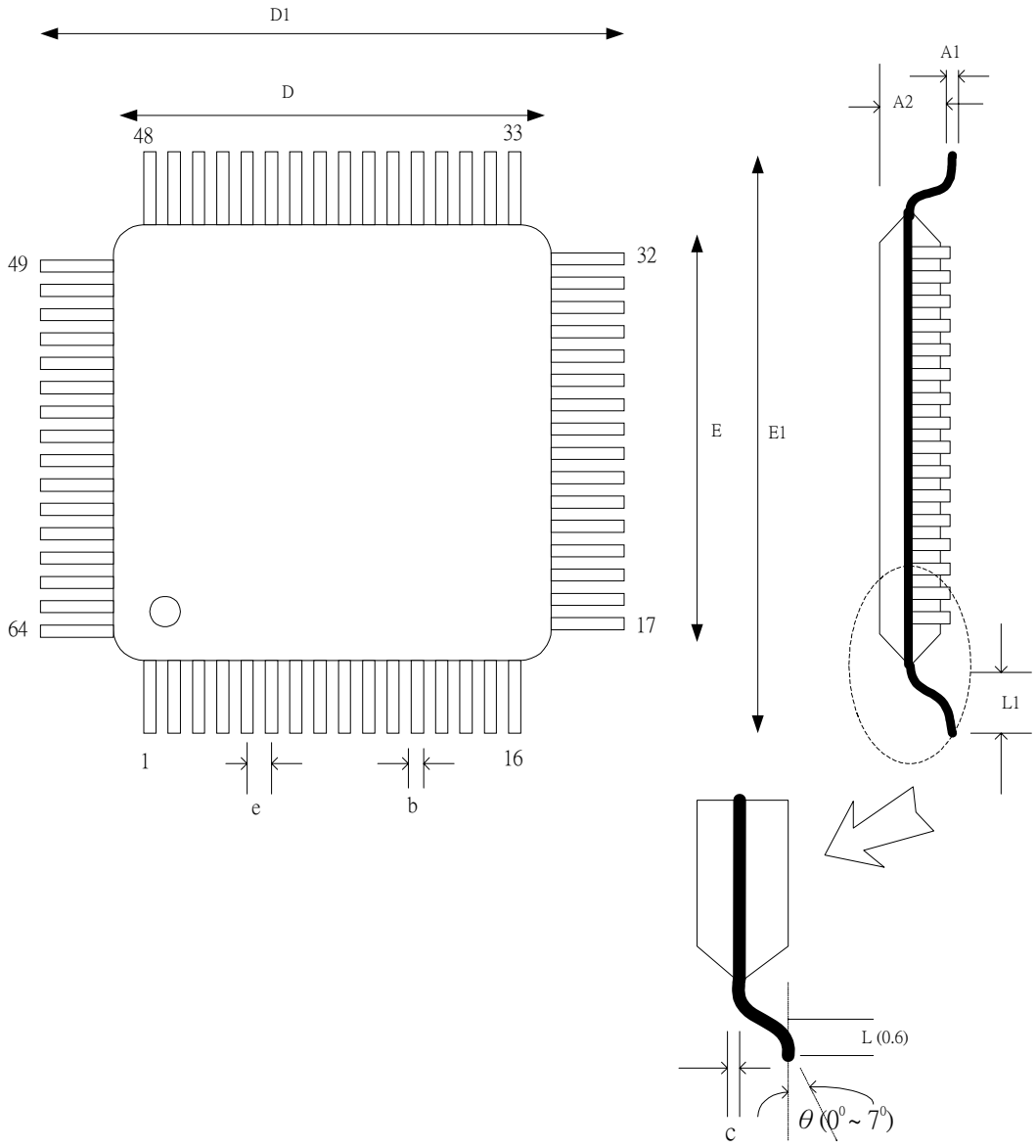


8.2 Brief application circuit chart



* detail application circuit is available by customer request

IX. Package Specification

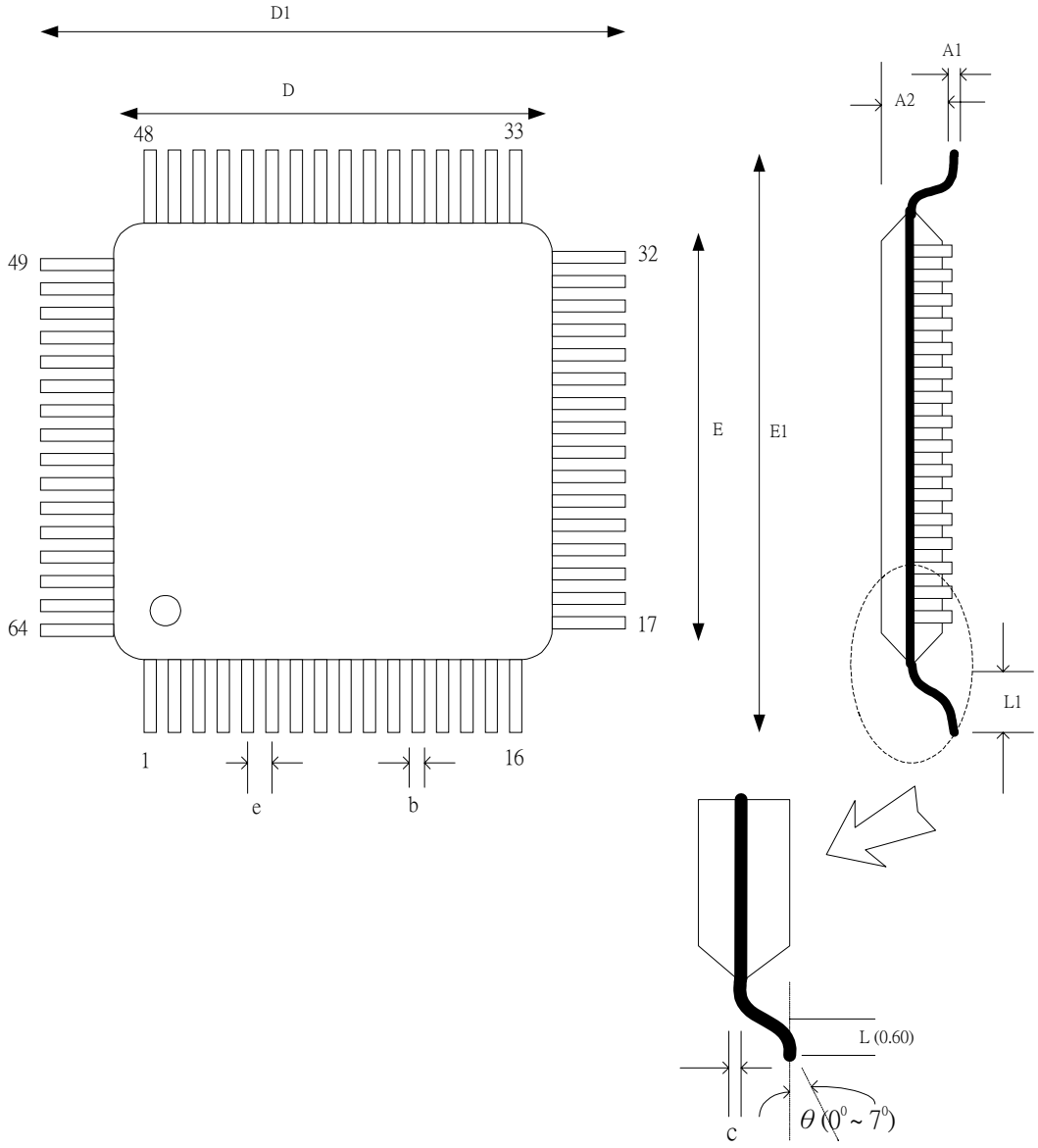


64-pin LQFP package

Lead Count	Body Size			
64	D	E	D1	E1
	10.00	10.00	12.00	12.00

Stand-off	Body Thk	Lead Length	Lead Width	Lead Thk	Lead Pitch
A1	A2	L1	b	c	e
0.10	1.40	1.00	0.24	0.125	0.50

Unit : mm



64-pin TQFP package

Lead Count	Body Size			
64	D	E	D1	E1
	10.00	10.00	12.00	12.00

Stand-off	Body Thk	Lead Length	Lead Width	Lead Thk	Lead Pitch
A1	A2	L1	b	c	e
0.10	1.00	1.00	0.20	0.127	0.50

Unit : mm

Appendix A

AC-97 digital mode note

When the SN11112 is implemented as a product containg only digital functions. Please note the switch ‘S1’ on ‘spdif connection diagram’ of application circuit.

There will be some noise problem when playing audio CD on PC using software like WINAMP or JetAudio. The reason is these softwares will send USB IN Token to device for getting audio CD spectrum when users play audio CD and turn on spectrum display function. But if users play audio CD by InterVideo WINRIP, MS Window default CD player or media player, it is o.k..

There are two ways to solve this problem. One method is to advise users to turn off spectrum display function when using WINAMP or JetAudio to play audio CD.

The other way is to implement a switch at ‘SPDFIN’ input pin of SN11112. When users want to play audio CD by WINAMP or JetAudio and turn on spectrum display function, please switch ‘S1’ to ‘SPDIF_LB’ signal. That will connect ‘SPDIF_O’ pin to ‘SPDFIN’ pin directly and let audio CD being played loop back to PC. Then these playback applications can get audio CD spectrum. When users want to record digital audio source from external instrument like DAT player or CD player with SPDIF digital out, please switch ‘S1’ to ‘DIGAUD_IN’ signal and let external digital audio source flow into SPDFIN pin. Afterward PC can record this digital audio source.

If the product is made as a SPDIF download cable(playback only), just connecting ‘SPDIF_O’ pin to ‘SPDFIN’ pin can solve this noise problem when playing CD with WINAMP or JetAudio.

The SN11112 provides two recording sampling rates, 48KHz and 44.1KHz, when configured as a digital function only device. It can support 44.1KHz recording sampling rate by pulling ‘RECRATE’ pin to GND. 48KHz recording sampling rate is active by pulling ‘RECRATE’ pin to 3.3V.

At WINDOW Millennium or WINDOW XP beta2 version , there will be a speaker icon at task bar when the device containg digital function only is attached, but no speaker icon at WIN98SE or WIN2000. If you want to see a speaker icon on WIN98SE or WIN2000 task bar when the device with digital function only is attached, the SN11112 must be configured as an AC97 full set device. But there will be some dummy functions like speaker volume control,

recording source selector, and analog recording volume control when you use AC97 full set to implement a digital function only device. At AC97 full set configuration, the sampling rates of playback and recording are only 48KHz.

It is depended on what you want to configure SN11112.

Appendix B

Two wire series bus in SN11112

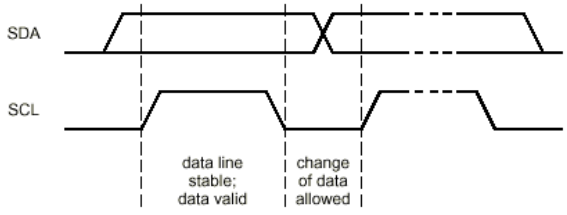
To provide extension capability, SN11112 contains a two wire series bus circuitry as an interface to MCU. The two wire series bus serves as a slave device with bit rate up to 400Kbps (fast mode). MCU can write two bytes to SN11112 with 8-bit register address 8'bxxxxxxx0 and 8'bxxxxxxx1; where 'x' means either '0' or '1'. MCU can also read one byte from SN11112 by any register address. The 7-bit slave address of SN11112 is assigned as 7'b0111000.

With 'HIDEN' activated, SN11112 will transfer the two bytes to the USB host via an additional interrupt pipe when any byte is written to it by MCU. Accompany with the two bytes two wire series bus data, SN11112 will also send one byte of button status. The sequence of the upward HID report is the button status first (LSB), then register with address 8'bxxxxxx0, then register with address 8'bxxxxxx1 (MSB). The USB host will keep polling the upward HID report every 32mS. When there is any button pressed or released, or two wire series bus data coming, SN11112 will transfer the three bytes of HID report to the USB host.

SN11112 can also transfer one byte data from the USB host to its register when 'HIDEN' is active. This is accomplished by a 'Set Output Report' HID class request via default control pipe. MCU can get this downward byte by polling. That is, MCU should read the byte at its favorite rate.

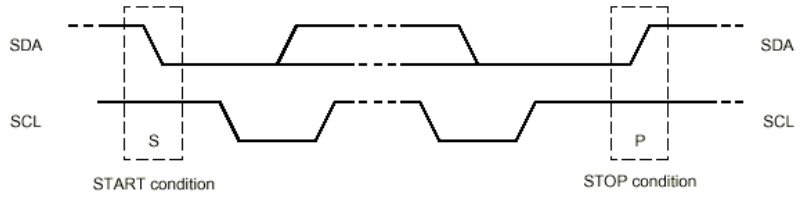
This document just provides simple description of the two wire series bus. User can get more detailed explanation from the specification.

SN11112 has one input pin 'SCL' where it gets two wire series bus clock from MCU, and one open-drain output pin 'SDA' where it sends or receives serial signal to/from MCU. As shown below, 'SDA' should be stable when 'SCL' is high, and can have transition only when 'SCL' is low.



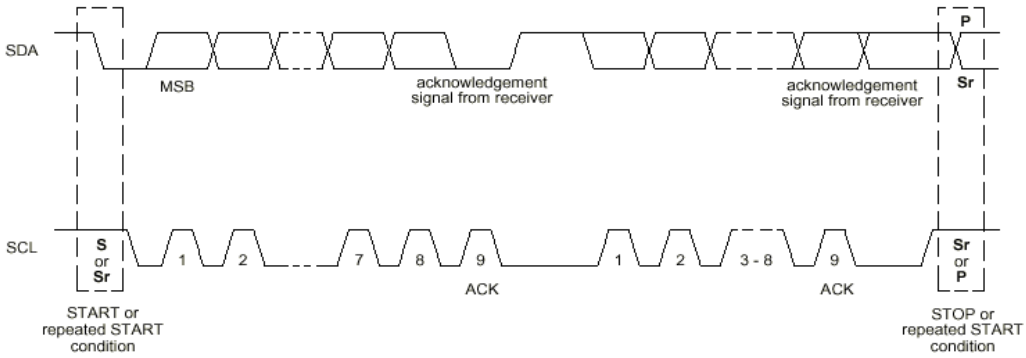
bit transfer on two wire series bus

START and STOP conditions shown below are the exception. Every two wire series bus transaction begins from a START, and ends with a STOP, or another START (repeated START).

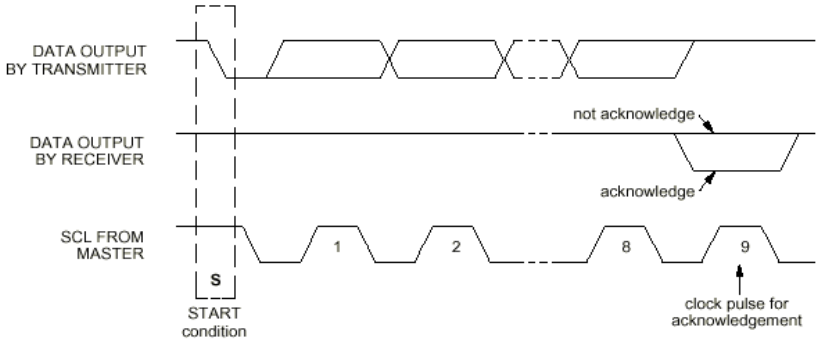


START and STOP conditions.

The figure below demonstrates a typical two wire series bus transaction. After every 8 bits sent by the transmitter, the receiver should send one bit low for positive acknowledgement or one bit high for negative acknowledgement. After the negative acknowledgement, a STOP or repeated START should follow. The next figure shows more detailed about acknowledgement bit. Note that 'SCL' is always driven by the master.

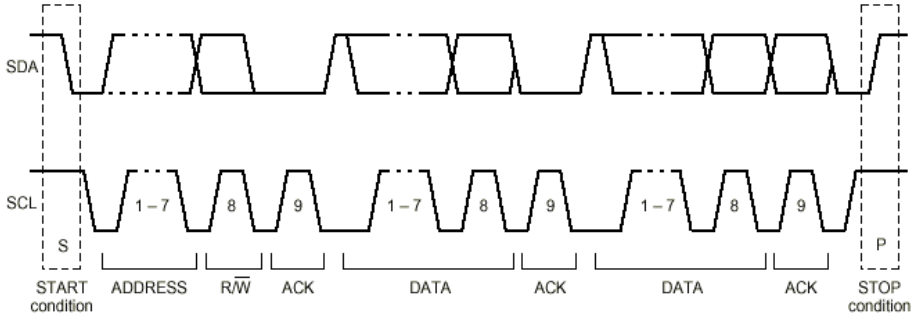


data transfer on two wire series bus



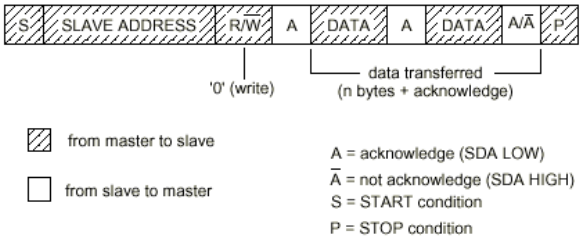
acknowledge on two wire series bus

The figure below shows a complete data transfer. After a START, MCU should send 7-bit slave address (7'b0111000) first, and then the 8th bit denotes a read transfer when it's high; or a write transfer when it's low. The first acknowledgement is always a duty of SN11112.



A complete data transfer.

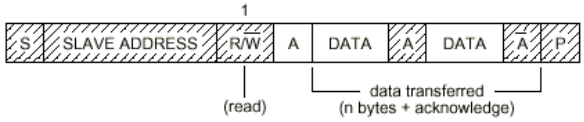
In the write transfer, MCU keep acting as the master and the transfer direction is not changed. The following figure gives an example of one byte write transfer.



A master-transmitter addressing a slave receiver with a 7-bit address.
The transfer direction is not changed.

SN11112 regards the first DATA byte as the register address. The second DATA byte is the content that MCU would like to write at the register address. If there is the third DATA byte, SN11112 will record this byte to the other register address. Note that the register address is auto-increment.

The figure below shows an example of two bytes read transfer. Because SN11112 has only one byte register to be read, the second DATA byte will be the same as the first one.



A master reads a slave immediately after the first byte.

Please note that the USB host try to get new HID data every 32mS. It's quite slow. If the continuous two wire series bus write transfers are too close in time, the former transfer may have no effect.

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