SMX1J

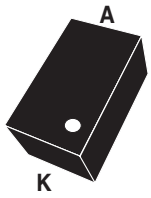
Transil™

Features

- Peak pulse power:
  - 85 W (10/1000 µs)
  - 800 W (8/20 µs)
- Stand off voltage 7.5 V
- Unidirectional
- Low leakage current:
  - 1 µA at 25 °C
  - 2 µA at 85 °C
- Operating Tj max: 150 °C
- High power capability at $T_j$max: 78 W

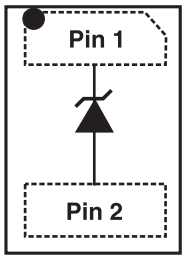
Complies with the following standards

- IEC 61000-4-2 level 4
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883G - Method 3015-7 Class 3B
  - 25 kV HBM (human body model)



µQFN 2L

Figure 1. Functional diagram (top view)



Description

The SMX1J7.5A Transil has been designed to protect sensitive equipment against electro-static discharges according to IEC 61000-4-2, MIL STD 883 Method 3015, and electrical over stress such as IEC 61000-4-4 and 5. They are generally for surges below 85 W 10/1000 µs.

The Planar technology makes it compatible with high-end equipment and SMPS where low leakage current and high junction temperature are required to provide reliability and stability over time.

The SMX1J7.5A is packaged in µQFN 2 leads.

TM: Transil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
P_{PP}	Peak pulse power dissipation (1)	T_j initial = T_{amb}	85	W
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Operating junction temperature range		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

1. For a surge greater than the maximum values, the diode will fail in short-circuit.

Figure 2. Electrical characteristics (definitions)

Symbol		Parameter
V_{BR}	=	Breakdown voltage
I_{RM}	=	Leakage current @ V_{RM}
V_{RM}	=	Stand-off voltage
V_{CL}	=	Clamping voltage
R_d	=	Dynamic impedance
I_{PP}	=	Peak pulse current
I_R	=	Breakdown current
αT	=	Voltage temperature coefficient
V_F	=	Forward voltage drop

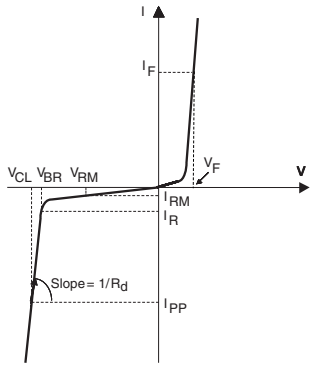


Table 2. Electrical characteristics - parameter values (T_{amb} = 25 °C)

Type	I_{RM} max@V_{RM}			V_{BR} @I_R min(1)		V_{CL} @I_{PP}(2) 10/1000 µs		R_D (3) 10/1000 µs	V_{CL} @I_{PP}(2) 8/20 µs		R_D (3) 8/20 µs	αT (4)
	25 °C	85 °C		min		max			max			max
	µA		V	V	mA	V	A	Ω	V	A	Ω	10-4/ °C
SMX1J7.5A	1	2	7.5	8.3	1	14	6.2	0.3	20	40	0.2	6.5

1. Pulse test : t_p < 50 ms
2. Surge capability given for both directions for unidirectional and bidirectional types
3. To calculate maximum clamping voltage at other surge level, use the following formula $V_{CLmax} = V_{CL} - R_D \times (I_{PP} - I_{PPappli})$ where $I_{PPappli}$ is the surge current in the application
4. To calculate V_{BR} or V_{CL} versus junction temperature, use the following formule:
   V_{BR} @ $T_j = V_{BR}$ @ 25 °C x $(1 + \alpha T \times (T_j - 25))$
   V_{CL} @ $T_j = V_{CL}$ @ 25 °C x $(1 + \alpha T \times (T_j - 25))$

Figure 3. Pulse waveform

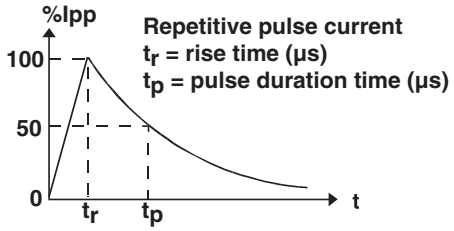


Figure 4. Peak pulse power dissipation versus initial junction temperature

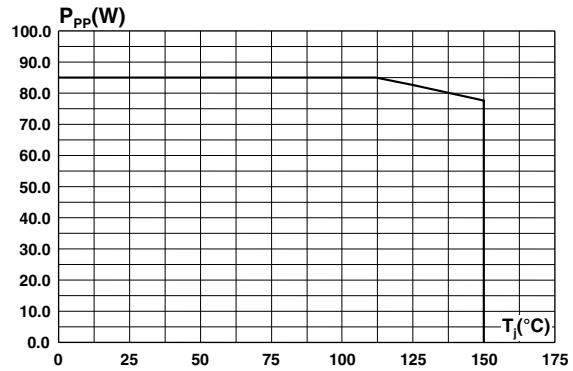


Figure 5. Peak pulse power versus exponential pulse duration

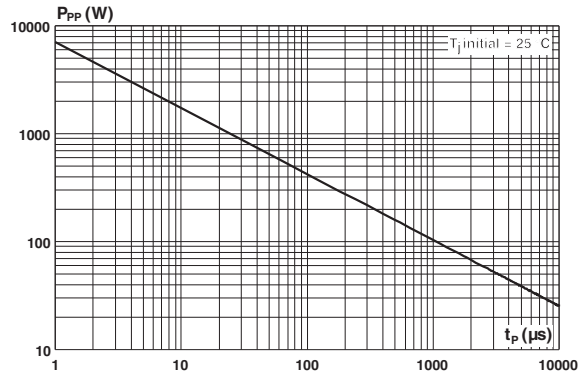


Figure 6. Clamping voltage versus peak pulse current (exponential waveform, typical values)

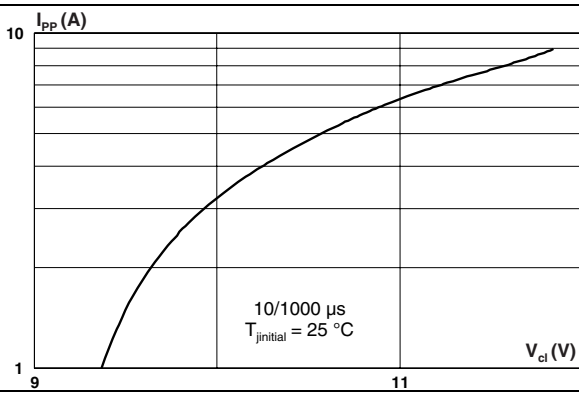


Figure 7. Junction capacitance versus reverse applied voltage (typical values)

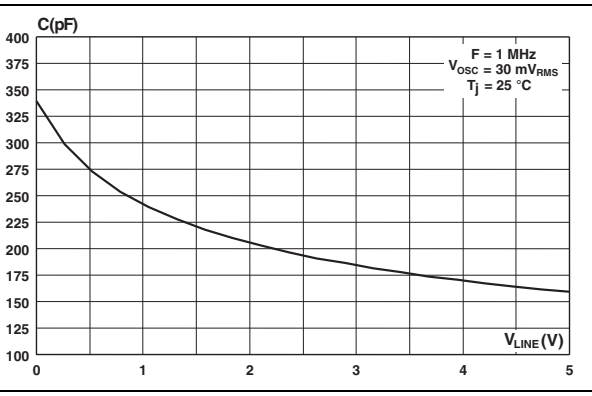


Figure 8. Forward voltage drop versus peak forward current (typical values)

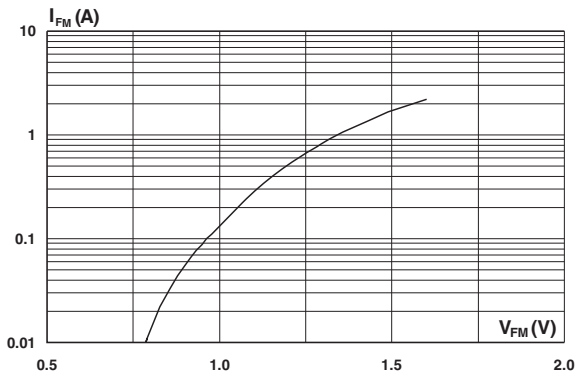
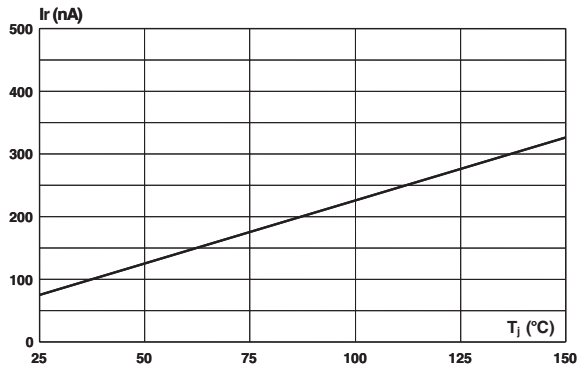
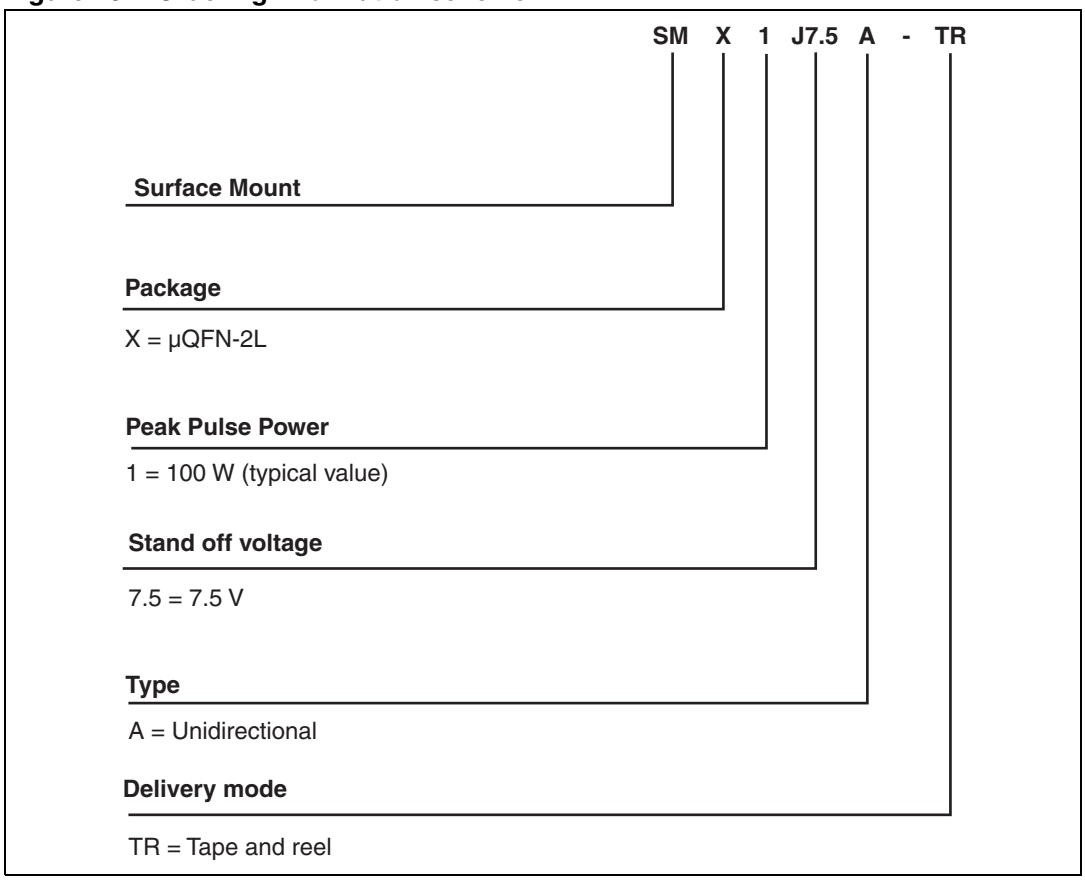


Figure 9. Leakage current versus junction temperature (typical values)



2 Ordering information scheme

Figure 10. Ordering information scheme

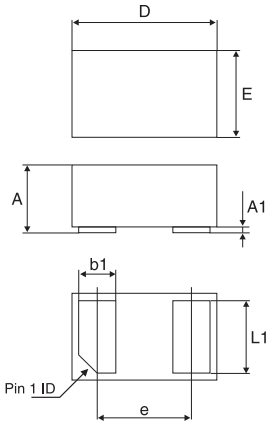


3 Package information

- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Flammability: Epoxy is rated UL94V-0
- RoHS package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 3. µQFN 2L dimensions



Ref	Dimensions					
	Millimetres			Inches		
	Min	Typ	Max	Min	Typ	Max
A	0.51	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b1	0.25	0.30	0.35	0.010	0.012	0.014
D		1.45			0.057	
E		1.00			0.039	
e	0.95	1.00	1.05	0.037	0.039	0.041
L1	0.75	0.80	0.85	0.030	0.031	0.033

Figure 11. Footprint dimensions in mm (inches)

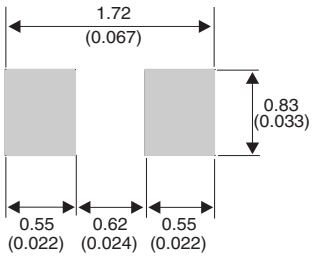
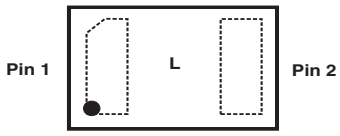
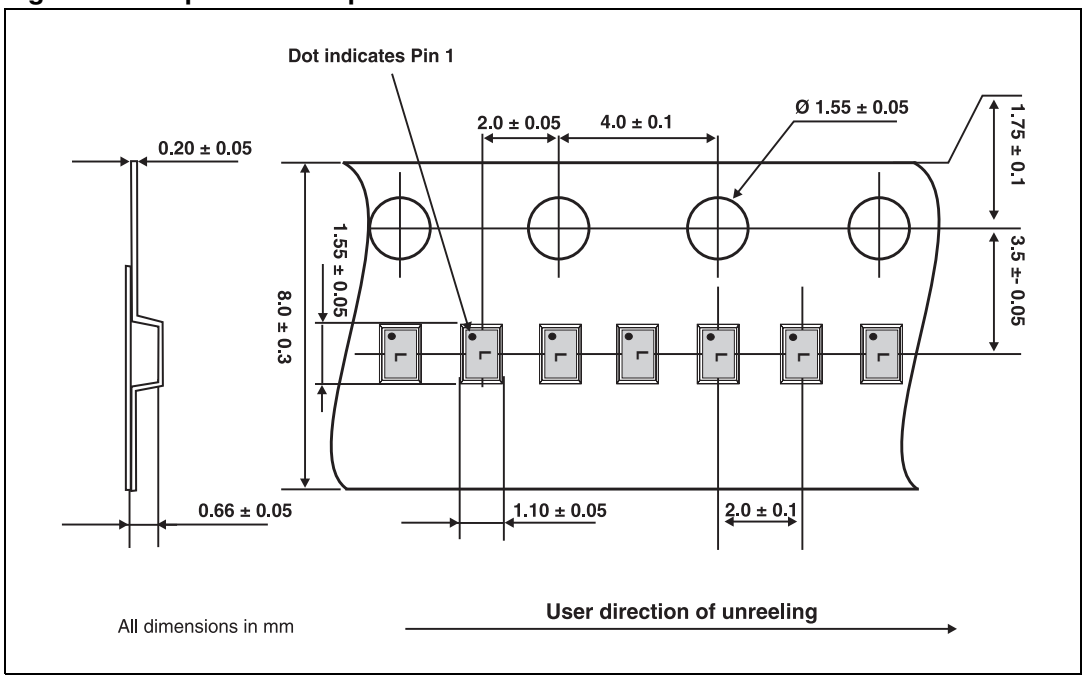


Figure 12. Marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose

Figure 13. Tape and reel specifications

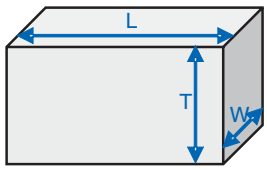


4 Recommendation on PCB assembly

4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 14. Stencil opening dimensions



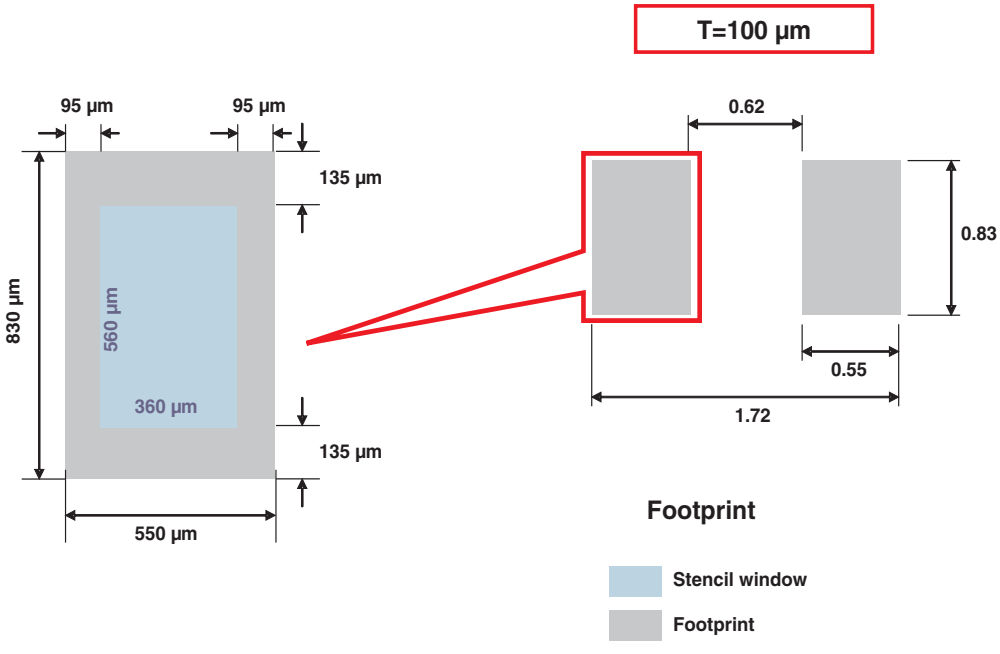
   b) General design rule
   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L+W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio - between 65% and 70%.

Figure 15. Recommended stencil windows position



4.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. Solder paste without cleaning flux is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

4.3 Placement

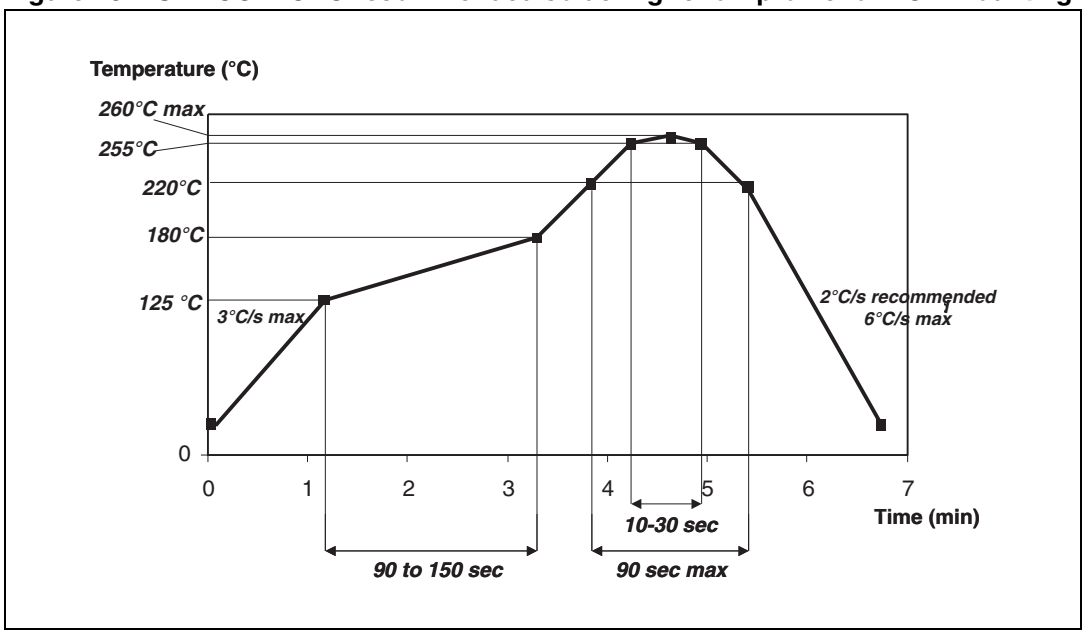
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

4.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

4.5 Reflow profile

Figure 16. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
SMX1J7.5A	L	µQFN-2L	2.2 mg	3000	Tape and reel

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
26-Oct-2009	1	First issue.
03-Nov-2009	2	Updated *: Features*, *Table 2*, *Table 4* and *Figure 11*.

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