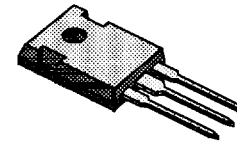
Siliconix incorporated

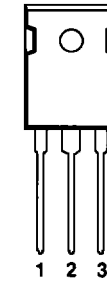
SMW45N10

N-Channel Enhancement Mode Transistor

TO-247 AD



TOP VIEW



1 GATE
2 DRAIN
3 SOURCE

1 2 3

PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
100	0.040	45

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25°C	I_D	45	A
	T_C = 100°C		27	
Pulsed Drain Current[1]		I_{DM}	180	
Avalanche Current (See Figure 9)		I_{AR}	45	
Avalanche Energy	L = 0.3 mH	E_A	300	mJ
Repetitive Avalanche Energy[2]	L = 0.02 mH	E_{AR}	20	
Power Dissipation	T_C = 25°C	P_D	150	W
	T_C = 100°C		60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		0.83	K/W
Junction-to-Ambient	R_{thJA}		40	
Case-to-Sink	R_{thCS}	0.35		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%, T_C = 25°C.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		100		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V, V_{GS} = 0 V			25	µA
		V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V		45		A
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 27 A	0.030		0.040	Ω
		V_{GS} = 10 V, I_D = 27 A, T_J = 125°C	0.058		0.072	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 27 A		15		S
DYNAMIC						
Input Capacitance	C_{lss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	3000			pF
Output Capacitance	C_{oss}		750			
Reverse Transfer Capacitance	C_{rss}		150			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 45 A	72		100	nC
Gate-Source Charge[2]	Q_{gs}		26		35	
Gate-Drain Charge[2]	Q_{gd}		31		40	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 1.1 Ω, $I_D \simeq$ 45 A, V_{GEN} = 10 V, R_G = 2.5 Ω	17		30	ns
Rise Time[2]	t_r		80		120	
Turn-Off Delay Time[2]	$t_{d(off)}$		40		60	
Fall Time[2]	t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				45	A
Pulsed Current[3]	I_{SM}				180	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5	V
Reverse Recovery Time	t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	130			ns
Reverse Recovery Charge	Q_{rr}		0.31			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

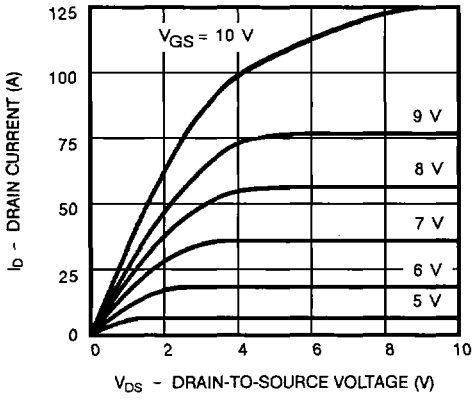


Figure 2. Transfer Characteristics

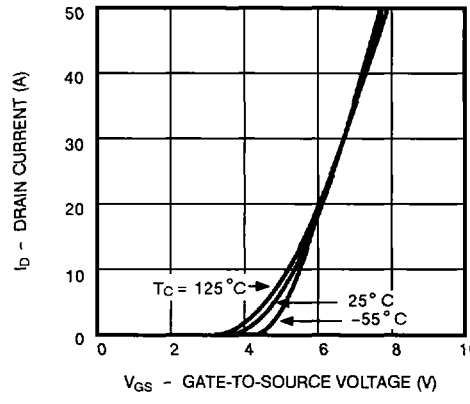


Figure 3. Transconductance

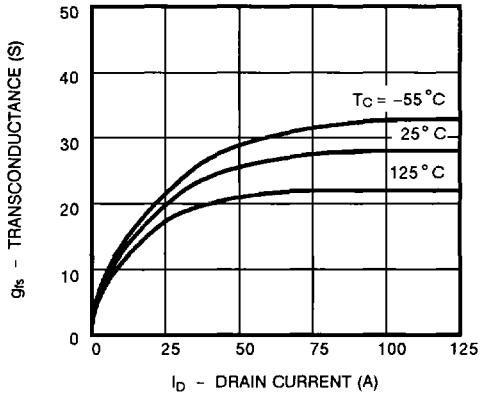


Figure 4. On-Resistance

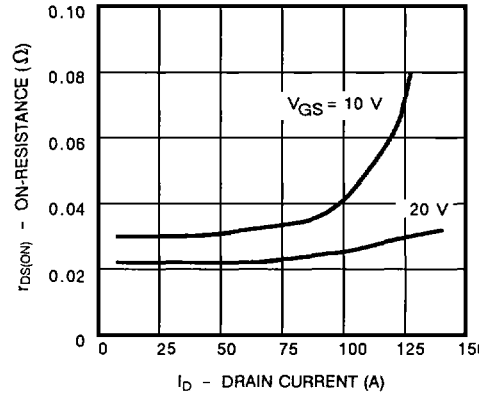


Figure 5. Capacitance

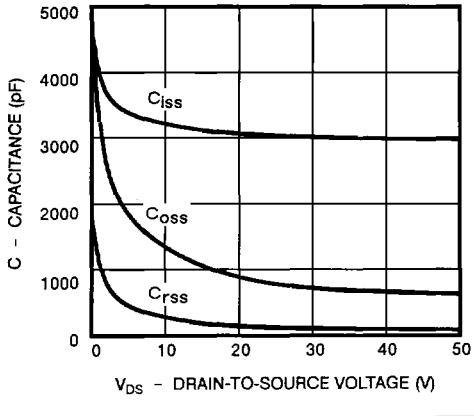
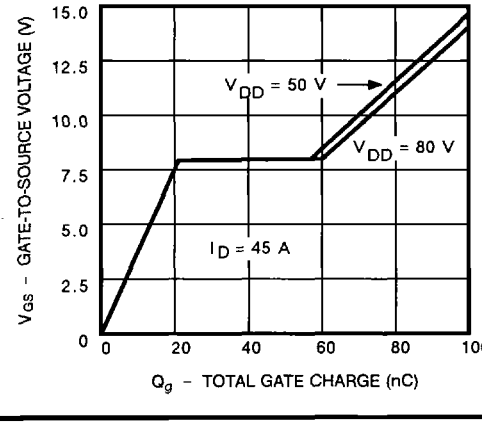


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

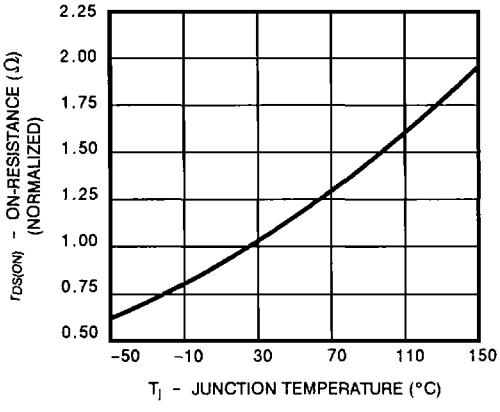
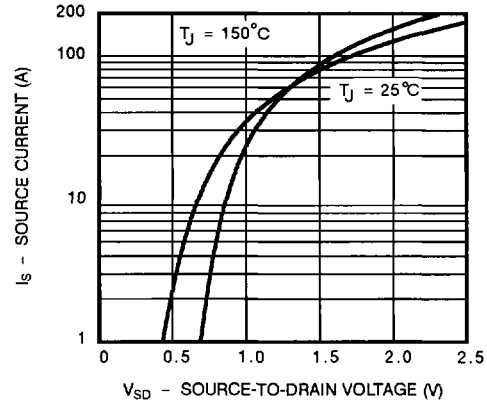


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

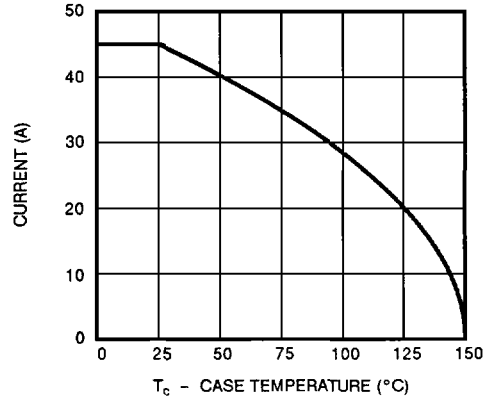
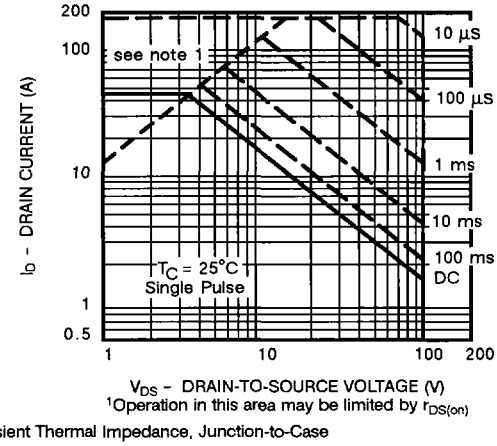


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case