

20V N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SMC8205AW is the Dual N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, advanced trench technology to provide excellent $R_{DS(ON)}$.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in small outline surface mount package.

SMC8205AW-TRG ROHS Compliant This is Halogen Free

FEATURE

- ◆ **20V/6.0A, $R_{DS(ON)} = 21m\Omega (typ.) @ V_{GS} = 4.5V$**
- ◆ **20V/5.2A, $R_{DS(ON)} = 25m\Omega (typ.) @ V_{GS} = 2.5V$**
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability

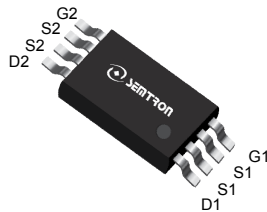
APPLICATIONS

- ◆ Power Management in Note book
- ◆ Portable Equipment
- ◆ Battery Powered System

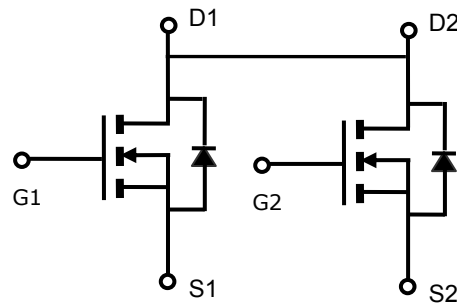


N-Channel Enhancement Mode MOSFET

PIN CONFIGURATION



TSSOP-8
Top View



PART NUMBER INFORMATION

SMC 8205A W - TR G a b c d e	a : Company name. b : Product Serial number. c : Package code d : Handling code e : Green produce code
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ORDERING INFORMATION

Part Number	Package Code	Handling Code	Shipping
SMC8205AW-TRG	W : TSSOP-8	TR : Tape&Reel	3K/Reel

※ Year Code : 0 ~ 9, 2010 : 0

※ Week Code : A(1~2) ~ Z(53~54)

※ TSSOP-8 : Only available in tape and reel packaging.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		20	V
V _{GSS}	Gate-Source Voltage		±12	V
I _D	Continuous Drain Current (T _C =25°C) ^A	V _{GS} =4.5V	6.0	A
	Continuous Drain Current (T _C =70°C)		5.0	A
I _{DM}	Pulsed Drain Current ^B		20	A
P _D	Power Dissipation	T _A =25°C	1.5	W
		T _A =70°C	1.0	
T _J	Operation Junction Temperature		-55 to150	°C
T _{STG}	Storage Temperature Range		-55 to150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

THERMAL DATA

Symbol	Parameter		Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient ^A	Steady-State	-	100	$^{\circ}\text{C}/\text{W}$
$R_{\theta JL}$	Thermal Resistance Junction to Lead ^A	Steady-State	-	75	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS($T_J = 25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V,I _D =250μA	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} ,I _D =250μA	0.5	0.7	1.2	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V,V _{GS} =±12V			±100	nA
I _{DSS}	Zero Gate Voltage, Drain-Source Leakage Current	V _{DS} =16V,V _{GS} =0V T _J =25°C			1	μA
		V _{DS} =16V,V _{GS} =0V T _J =55°C			5	
R _{DS(ON)}	Drain-source On-Resistance ^B	V _{GS} =4.5V,I _D =6.0A V _{GS} =2.5V,I _D =5.2A		21 25	25 28	mΩ
G _{fs}	Forward Transconductance	V _{DS} =15V,I _D =3.6A		10		S
Source-Drain Doide						
V _{SD}	Diode Forward Voltage	I _S =1.0A,V _{GS} =0V		0.75	1.0	V
I _S	Continuous Source Current ^{AD}				10	A
Dynamic Parameters						
Q _g (4.5V)	Total Gate Charge	V _{DS} =10V V _{GS} =4.5V I _D ≡6.0A		17		nC
Q _{gs}	Gate-Source Charge			0.7		
Q _{gd}	Gate-Drain Charge			3.4		
C _{iss}	Input Capacitance	V _{DS} =10V V _{GS} =0V f=1MHz		850		pF
C _{oss}	Output Capacitance			142		
C _{rss}	Reverse Transfer Capacitance			112		
t _{d(on)}	Turn-On Time	V _{DD} =10V I _D =6A V _{GEN} =4.5V R _G =3.3Ω		6.5		nS
t _r				12		
t _{d(off)}	Turn-Off Time			32		
t _f				7.3		

Note:

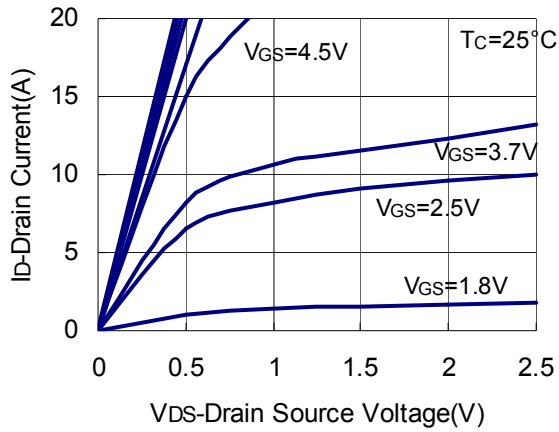
- The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_C=25^{\circ}\text{C}$.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.1mH$.
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date

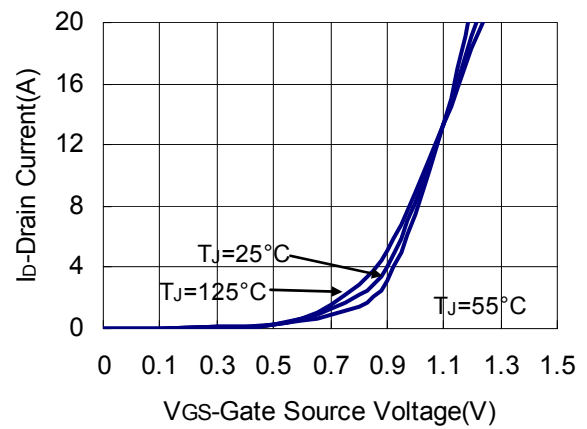
We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

TYPICAL CHARACTERISTICS (25°C Unless Note)

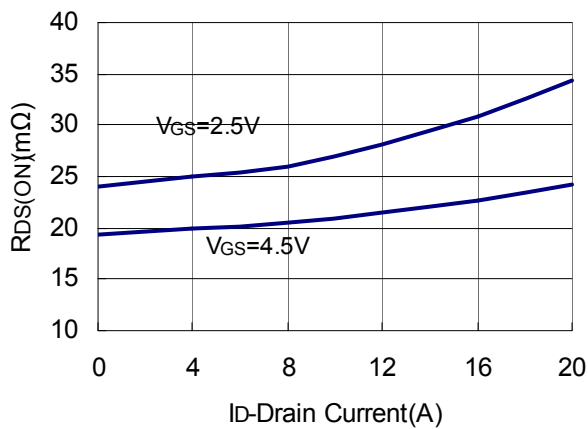
Output Characteristics



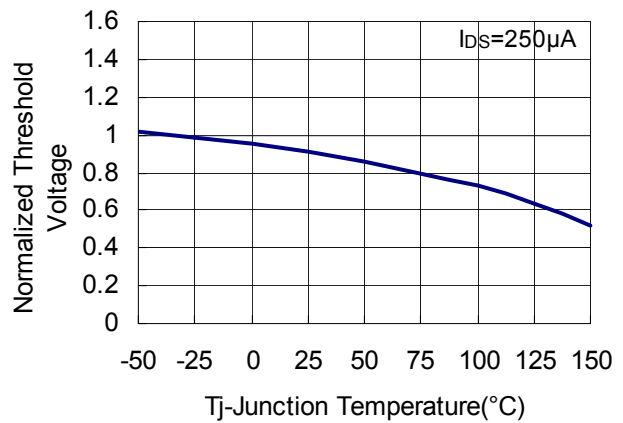
Drain-Source On Resistance



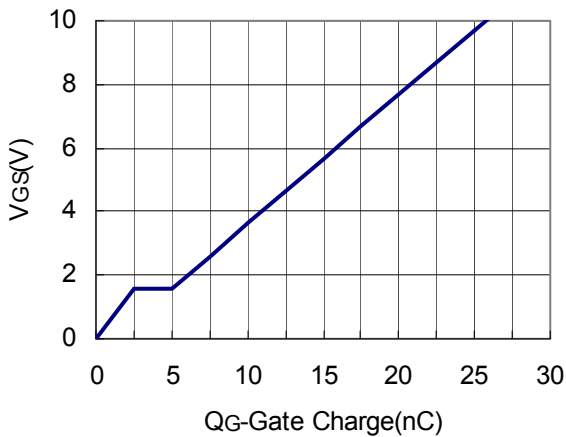
Transfer Characteristics



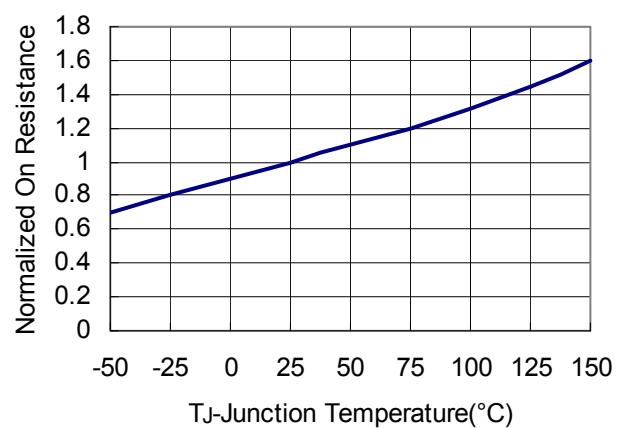
Gate Threshold Voltage



Gate Charge

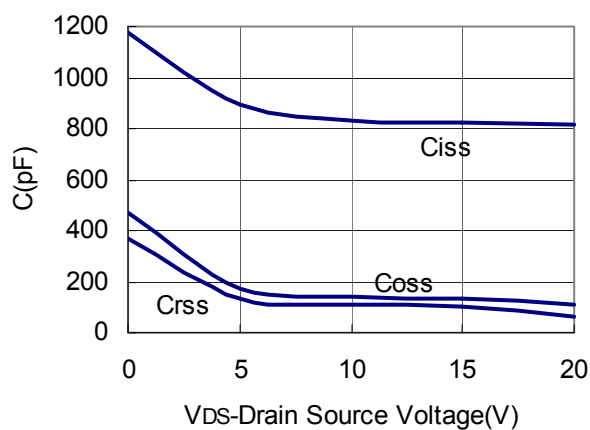


Drain Source On Resistance

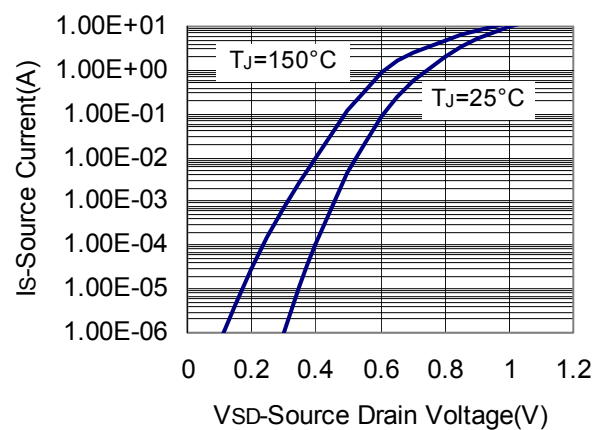


TYPICAL CHARACTERISTICS (25°C Unless Note)

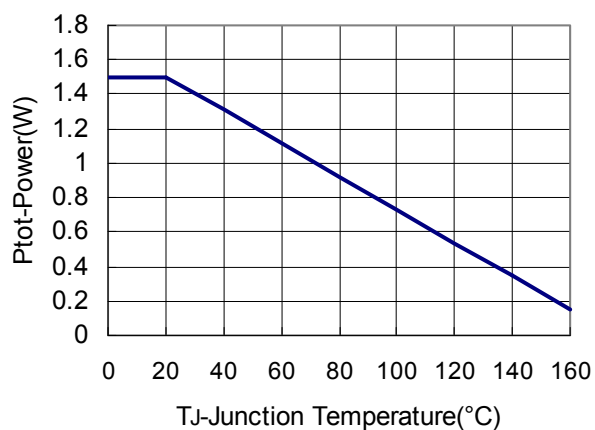
Capacitance



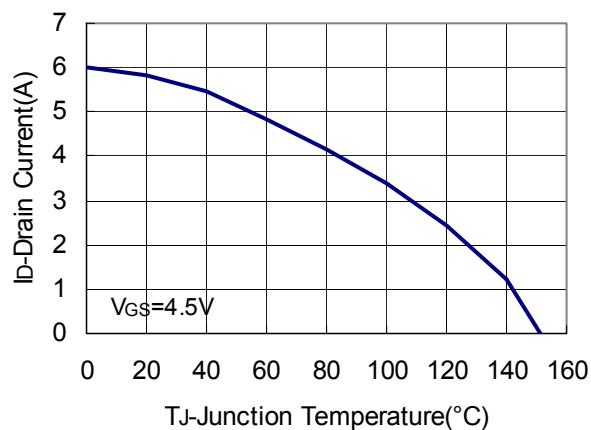
Source Drain Diode Forward



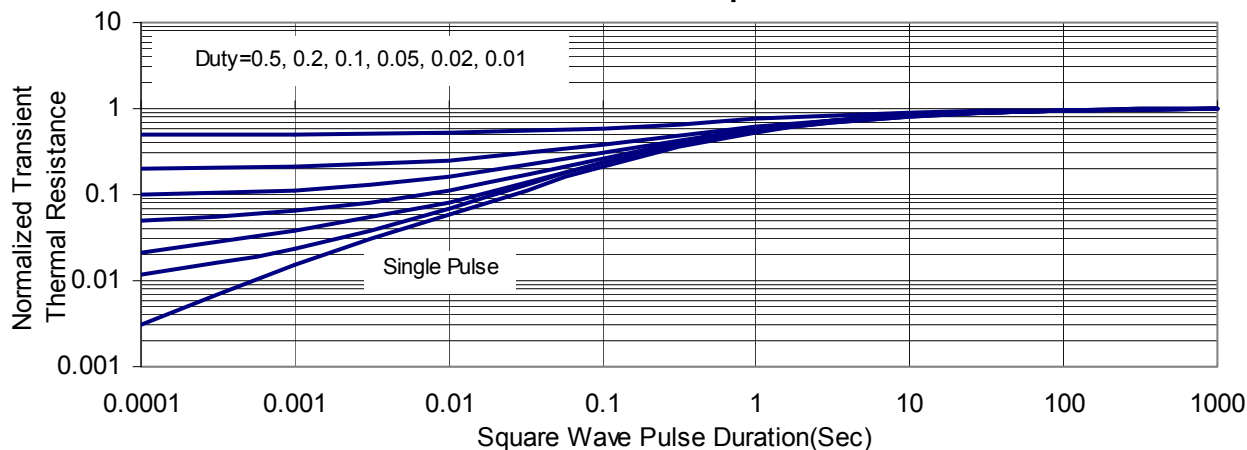
Power Dissipation



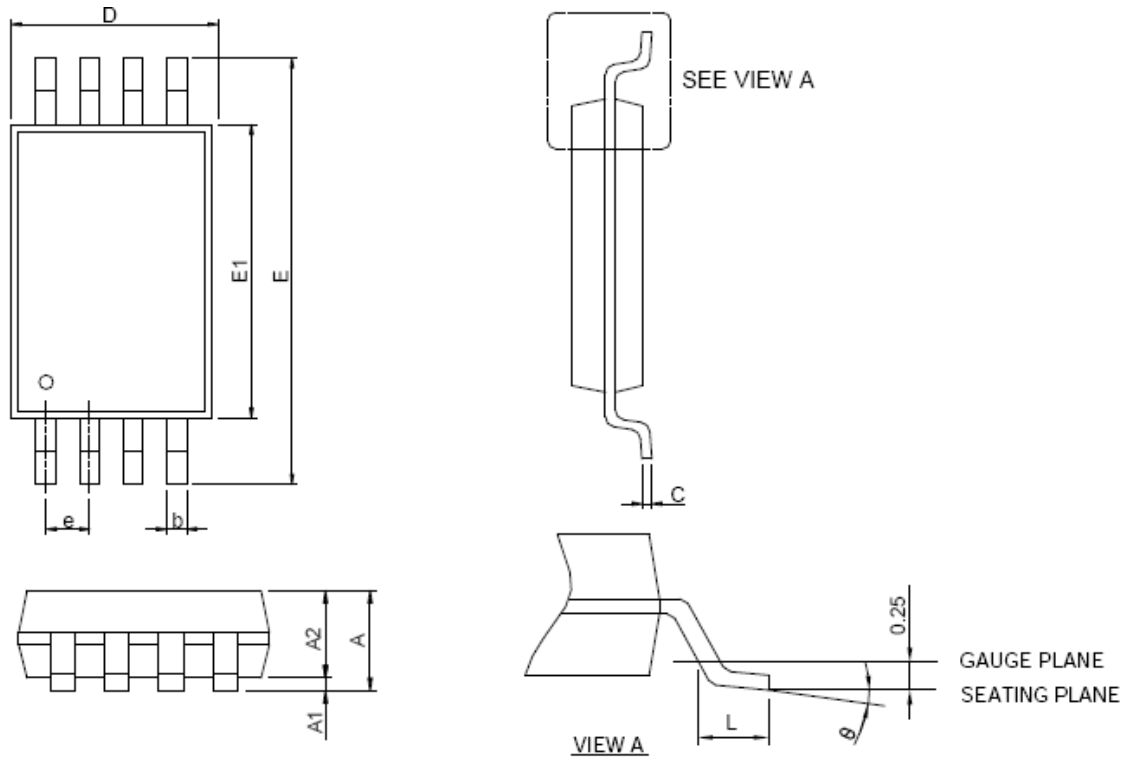
Drain Current



Thermal Transient Impedance



TSSOP-8 PACKAGE DIMENSIONS



SYMBOL	TSSOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.20		0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.031	0.041
b	0.19	0.30	0.007	0.012
c	0.09	0.20	0.004	0.008
D	2.90	3.10	0.114	0.122
E	6.20	6.60	0.244	0.260
E1	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
L	0.45	0.75	0.018	0.030
θ	0°	8°	0°	8°