

Single P-Channel MOSFET

■ DESCRIPTION

SMC4207PA is the P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior, fast switching performance. These devices are well suited for high efficiency fast switching applications.

■ PART NUMBER INFORMATION

SMC 4207 PA - TR G

a	b	c	d	e
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a : Company name.

b : Product Serial number.

c : Package code PA:DFN5X6A-8

d : Handling code TR:Tape&Reel

e : Green produce code G:RoHS Compliant

■ FEATURES

$V_{DS}=-40V$, $I_D=-55A$

$R_{DS(ON)}=9.5m\Omega$ (Typ.)@ $V_{GS}=-10V$

$R_{DS(ON)}=13m\Omega$ (Typ.)@ $V_{GS}=-4.5V$

◆ Low Gate Charge

◆ High switching speed

■ APPLICATIONS

◆ Power Applications

◆ LED Lighting



■ ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Symbol	Parameter	Rating	Units	
V_{DSS}	Drain-Source Voltage	-40	V	
V_{GSS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current	$T_c=25^{\circ}\text{C}$	-55	A
		$T_c=100^{\circ}\text{C}$	-35	A
I_{DM}	Pulsed Drain Current ^B	-220	A	
I_D	Continuous Drain Current	$T_A=25^{\circ}\text{C}$	-15.4	A
		$T_A=70^{\circ}\text{C}$	-12.3	A
P_D	Power Dissipation ^A	$T_A=25^{\circ}\text{C}$	5	W
		$T_A=70^{\circ}\text{C}$	3.2	W
I_{AS}	Single Pulse Avalanche Current ^B	-30	A	
E_{AS}	Single Pulse Avalanche energy L=0.1mH ^B	45	mJ	
P_D	Power Dissipation ^C	$T_c=25^{\circ}\text{C}$	62.5	W
		$T_c=100^{\circ}\text{C}$	25	W
T_J	Operation Junction Temperature	-55/150	$^{\circ}\text{C}$	
T_{STG}	Storage Temperature Range	-55/150	$^{\circ}\text{C}$	

■ THERMAL RESISTANCE

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ^A	$t \leq 10\text{s}$	25	$^{\circ}\text{C/W}$
	Thermal Resistance Junction to Ambient ^{AC}	Steady-State	60	
$R_{\theta JC}$	Thermal Resistance Junction to Case		2	

ELECTRICAL CHARACTERISTICS($T_A=25^\circ\text{C}$ Unless otherwise noted)

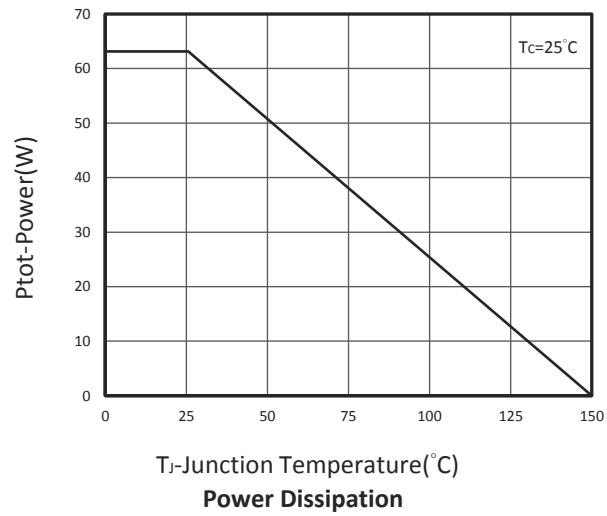
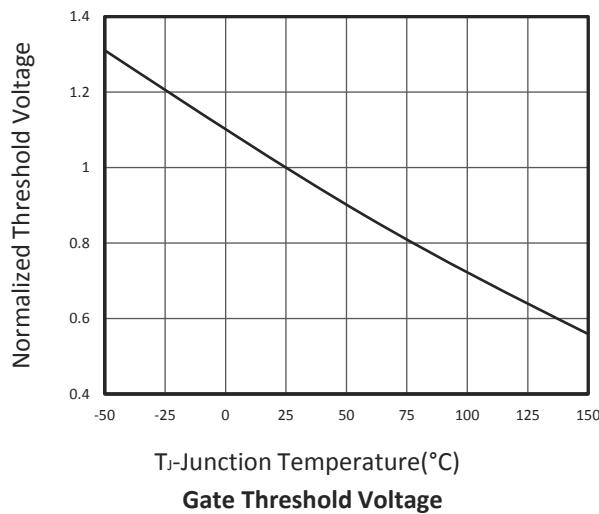
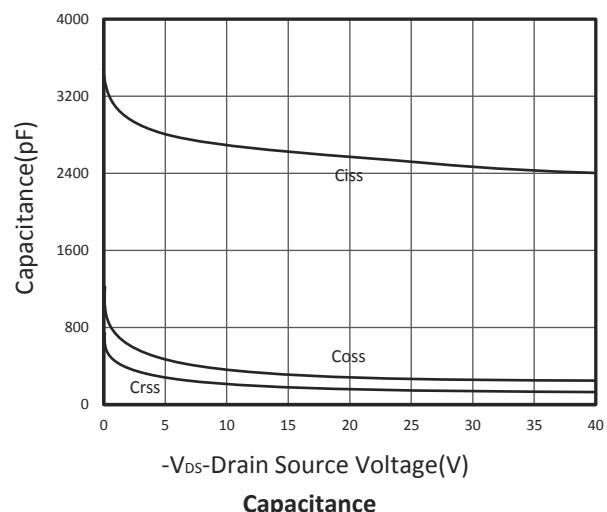
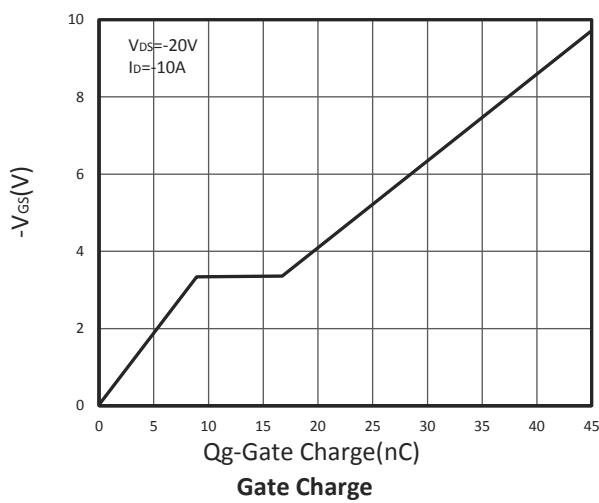
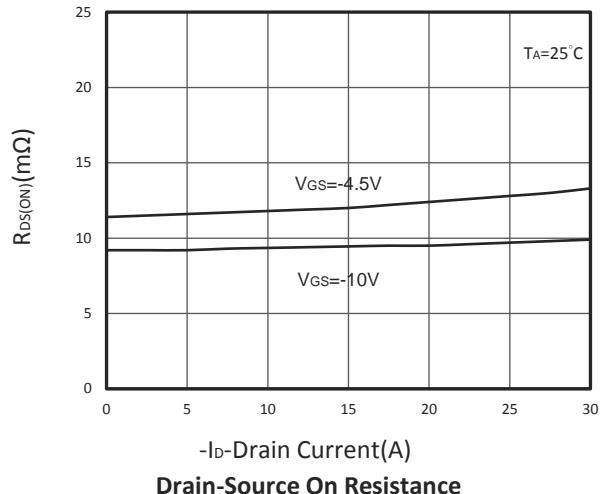
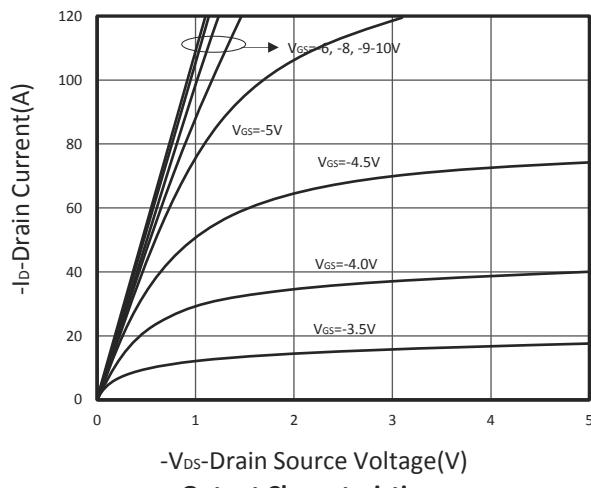
Symbol	Parameter	Condition	Min	Typ	Max	Unit	
Static Parameters							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=-250\mu\text{A}$	-40			V	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-1.6	-2.5	V	
I_{GSS}	Gate Leakage Current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-40\text{V}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$			-1	μA	
		$V_{DS}=-32\text{V}, V_{GS}=0\text{V}, T_J=75^\circ\text{C}$			-10		
$R_{DS(\text{ON})}$	Drain-source On-Resistance ^D	$V_{GS}=-10\text{V}, I_D=-15.4\text{A}$		9.5	12	$\text{m}\Omega$	
		$V_{GS}=-4.5\text{V}, I_D=-12\text{A}$		13	17		
G_f	Forward Transconductance	$V_{DS}=-10\text{V}, I_D=-10\text{A}$		38		S	
Diode Characteristics							
V_{SD}	Diode Forward Voltage ^D	$I_S=-1\text{A}, V_{GS}=0\text{V}$			-1	V	
I_S	Diode Continuous Forward Current				-55	A	
Dynamic and Switching Parameters^E							
Q_g	Total Gate Charge	$V_{DS}=-20\text{V}, V_{GS}=-10\text{V}$ $I_D=-10\text{A}$		47.1	63.5	nC	
Q_g	Total Gate Charge (4.5V)			22			
Q_{gs}	Gate-Source Charge			8			
Q_{gd}	Gate-Drain Charge			9			
C_{iss}	Input Capacitance	$V_{DS}=-20\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$		2750		pF	
C_{oss}	Output Capacitance			255			
C_{rss}	Reverse Transfer Capacitance			145			
$t_{d(on)}$	Turn-On Time	$V_{DD}=-20\text{V}, V_{GEN}=-10\text{V}$ $R_G=6\Omega I_D=-1\text{A}$		24	46	nS	
t_r				12	23		
$t_{d(off)}$	Turn-Off Time			47	89		
t_f				28	53		

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

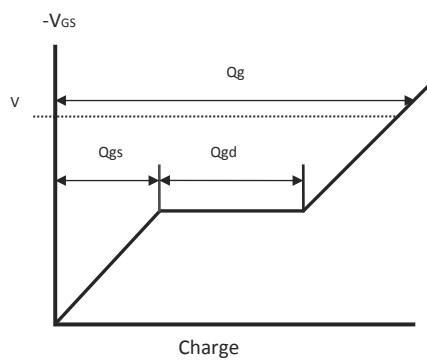
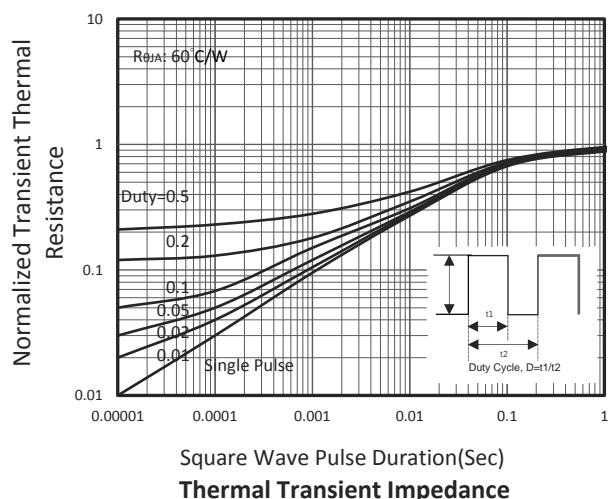
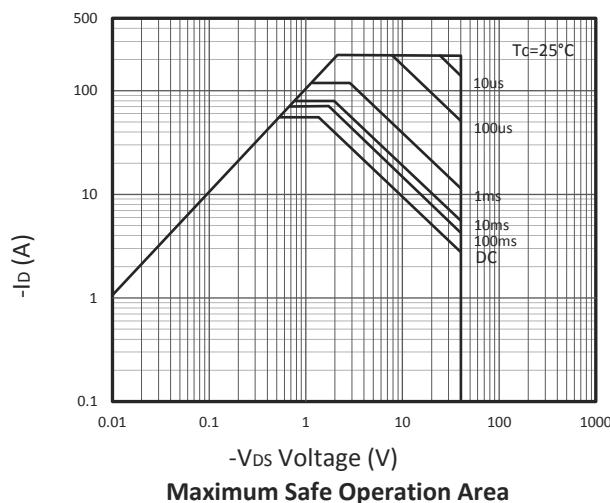
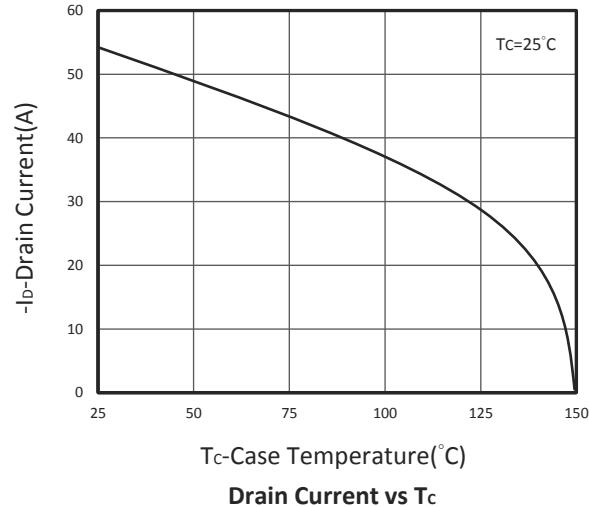
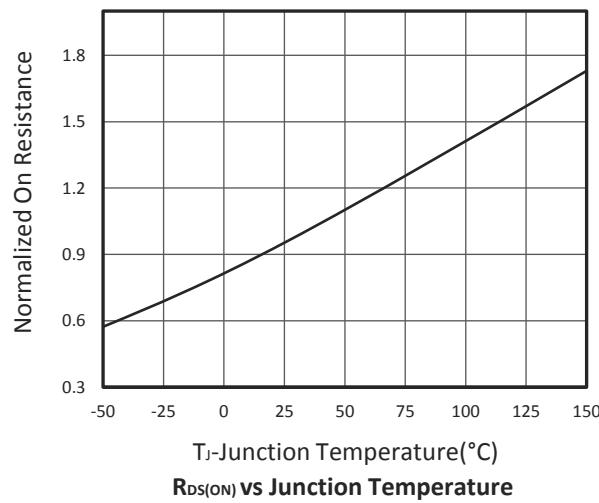
- A. Surface mounted on FR4 board using 1 in² pad size.
- B. Pulsed width limited by maximum junction temperature, $T_J(\text{MAX})=150^\circ\text{C}$.
- C. Using $\leq 10\text{s}$ junction-to-ambient thermal resistance is base on $T_J(\text{MAX})=150^\circ\text{C}$.
- D. Pulse test width $\leq 300\mu\text{s}$ and duty cycle $\leq 2\%$.
- E. Guaranteed by design, not subject to production testing.

The products and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date. We assume no responsibility for any infringement of patents, patent rights, or other rights arising from the use of any information and circuitry in this datasheet.

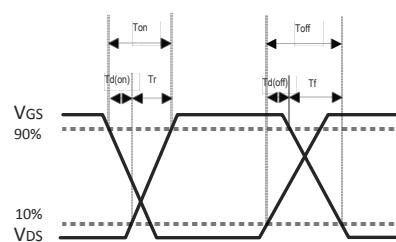
■ TYPICAL CHARACTERISTICS



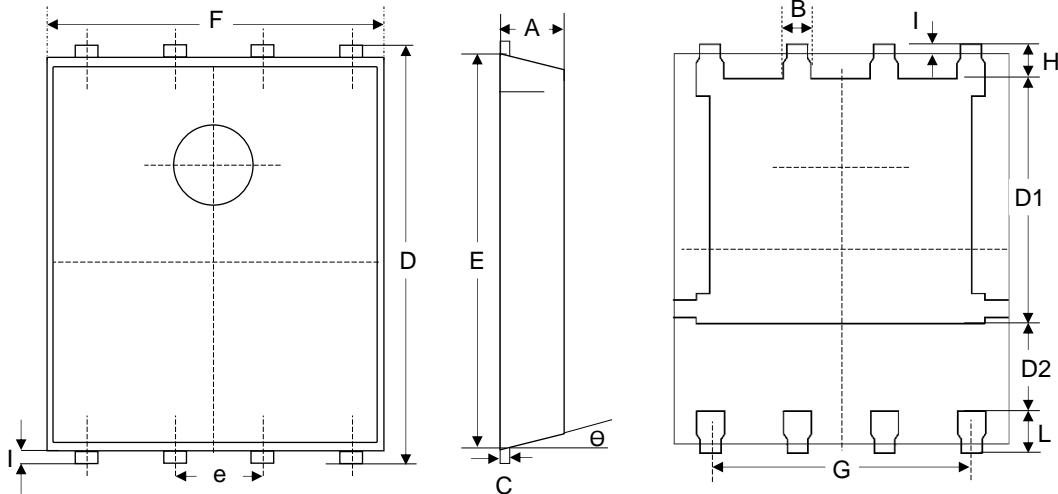
TYPICAL CHARACTERISTICS



Gate Charge Waveform



Switching Time Waveform

■ DFN5X6A PACKAGE DIMENSIONS


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043
B	0.330	0.510	0.013	0.020
C	0.200	0.300	0.008	0.012
D	5.900	6.100	0.232	0.240
D1	3.380	3.780	0.133	0.149
D2	1.100		0.043	
E	5.700	5.800	0.224	0.228
e	1.270BSC.		1.270BSC.	
F	4.800	5.000	0.189	0.197
G	0.361	0.396	0.014	0.016
H	0.410	0.610	0.016	0.024
I	0.060	0.200	0.002	0.008
L	0.510	0.710	0.020	0.028
Θ	0°	12°	0°	12°

Recommended Land Pattern

