8-Bit Micro-controller

With 64KB ISP Flash & TWSI & PWM & 1KB RAM embedded

Product List

SM5964AL25, 25MHz 64KB internal flash MCU

General Description

The SM5964A is a single-chip 8-bits micro-controller manufactured in an advanced CMOS process with on chip flash memory. It supports In-System Programming (ISP) function and is a derivative of the 8052 microcontroller family. The SM5964A has the same instructions set as the 80C51. The SM5964A contains a 64KB 3.3V on chip program flash, a volatile 1024 x 8 data RAM, four 8-bits I/O ports, one 4-bits I/O port, two 16-bits timer/event counters, and an additional 16-bits timer coupled to capture and compare latches, a two-priority-level, nested interrupt structure, two pulse-width- modulation (PWM) outputs, two serial interfaces (UART and TWSI bus). For system that requires extra capability the SM5964A can be expanded using standard LVTTL compatible memory and logic.

In addition, The SM5964A has two software selectable modes of power saving – IDLE mode and POWER-DOWN mode. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports, and interrupt system to continue functioning. The POWER-DOWN mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

The SM5964A is designed for 3.3V applications. The on chip flash memory can store data while the program is running. It also can upgrade the user program by down-load new code form PC or other devices. The chip is considered as a small integrated system.

Feature

- Working Voltage:3.0V through 3.6V
- 80C51 Central Processor Unit (CPU)
- 64K x 8 on chip flash memory with In-System-Programming(ISP) capability and it can be programmed at V_{CC} = 3.3V
- 1024 x 8 RAM, expandable externally to 64KB
- Two standard 16-bits timers/counters
- An additional 16-bits timer/counter coupled to a capture and compare register.
- Two 8-bits / 5-bits resolution Pulse-Width-Modulation (PWM) outputs
- Four 8-bits I/O ports.(For PDIP package)
- Four 8-bits I/O ports plus one 4-bits I/O port. (For PLCC or QFP package)
- TWSI-bus serial I/O port with master and slave functions
- Full-duplex UART
- 7 interrupt sources with 2 priority levels
- Temperature range (0℃ to +70℃)
- Software enable/disable ALE output pulse
- Wake-up from POWER-DOWN mode by external interrupt or H/W RESET.
- ISP service program space configurable in N*512 byte (N=0 to 8) size

Ordering Information

SM5964AihhkL

yymmv

i: process identifier {L=3.0V~3.6V}

hh: working clock in MHz {25}

k: package type postfix {as below table}

yy: year

mm: month

v: version identifier { , A, B, ...}

L: PB free identifier {no text is Non-PB free, “P” is PB free}

Taiwan
6F, No.10-2 Li- Hsin 1st Road ,
Science-based Industrial Park,
Hsinchu, Taiwan 30078

TEL: 886-3-567-1820
886-3-567-1880
FAX: 886-3-567-1891
886-3-567-1894

8-Bit Micro-controller
With 64KB ISP Flash & TWSI & PWM & 1KB RAM embedded

Package Spec.

K	Package	Pin / PAD
J	44L PLCC	Figure 1
Q	44L QFP	Figure 2
P	40L PDIP	Figure 3

Pin Configuration

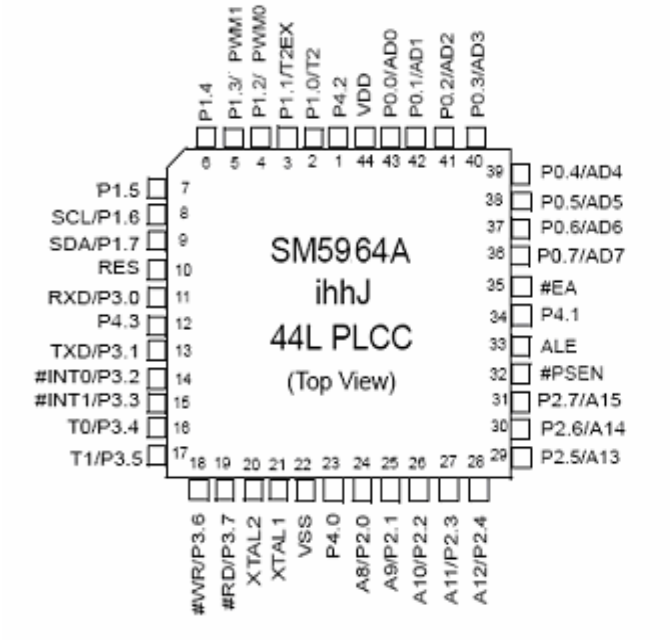


Figure 1 44L PLCC Package

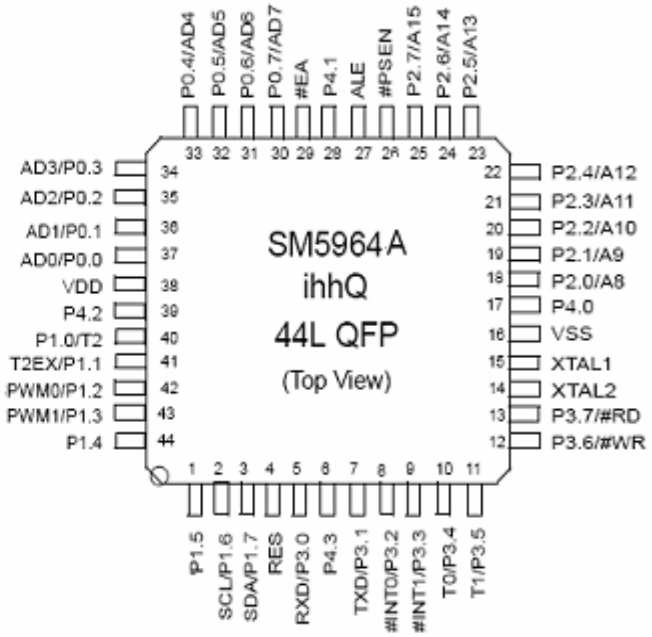


Figure 2 44L QFP Package

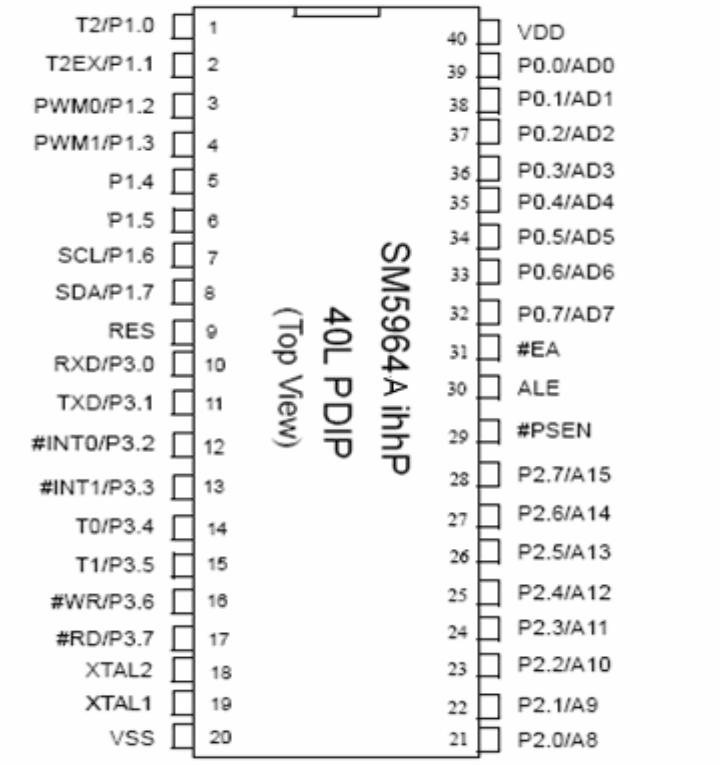
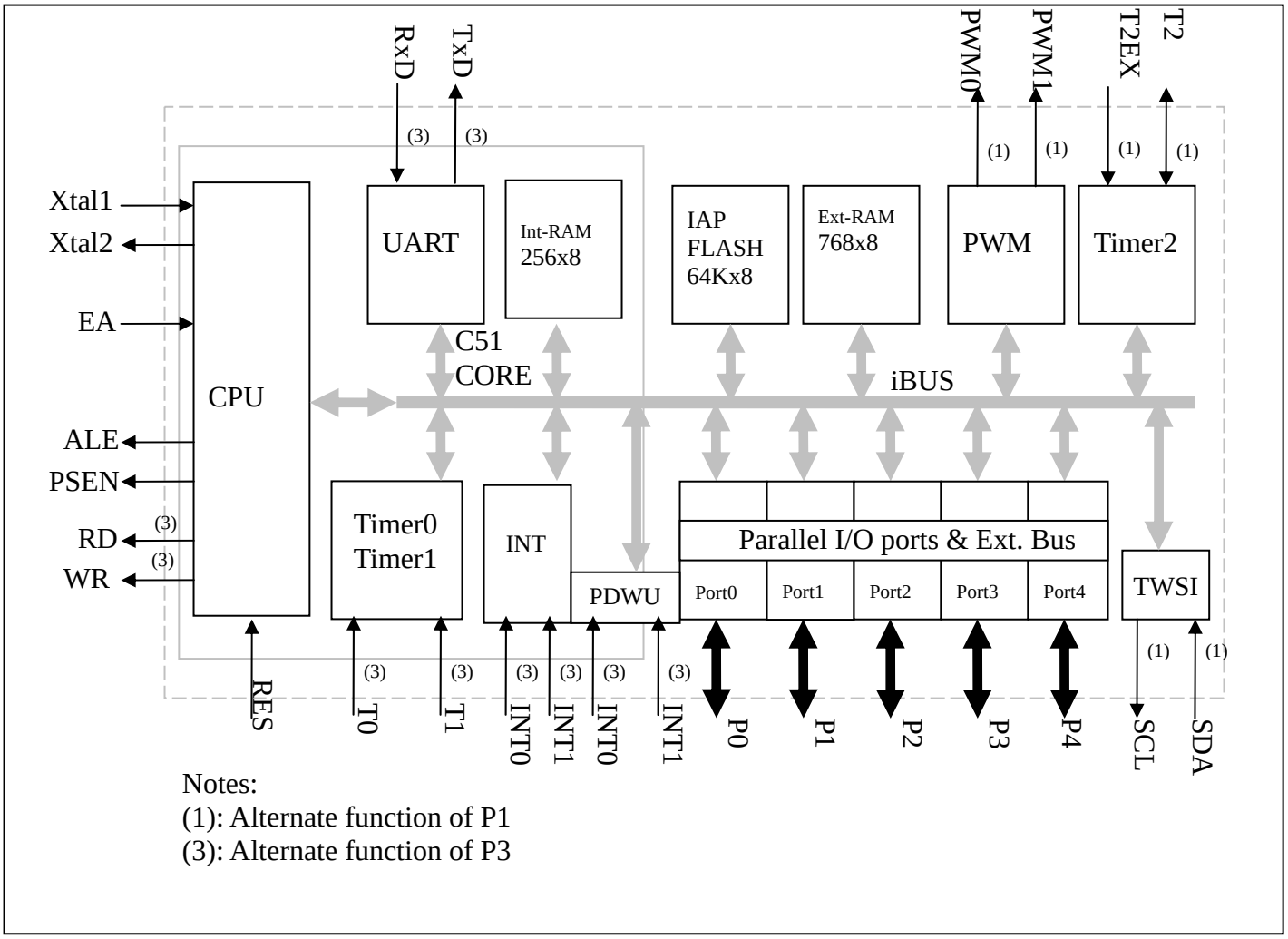


Figure 3 40L PDIP Package

Specifications subject to change without notice contact your sales representatives for the most recent information.

Block Diagram



Notes:
(1): Alternate function of P1
(3): Alternate function of P3

Pin Description

MNEMONIC	PDIP 40 pin	PQFP 44 Pin	PLCC 44 pin	Names and Functions
VDD	40	38	44	**Power supply**: +3.3V power supply pin during normal operations and power saving modes.
P0.0 – P0.7	39,38,37,36 35,34,33,32	37,36,35,34 33,32,31,30	43,42,41,40 39,38,37,36	**Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them become floating and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0 – P1.7	1,2,3,4, 5,6,7,8	40,41,42,43, 44,1,2,3	2,3,4,5, 6,7,8,9	**Port 1:** An 8-bits bidirectional I/O port with internal pull-ups on all pins. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL). Alternate function of SM5964A include： Port Pin Alternative function P1.0 T2： TIMER2 clock output P1.1 T2EX：TIMER2 reload/capture DIR. P1.2 PWM0：PWM channel 0 output P1.3 PWM1：PWM channel 1 output P1.6 SCL：TWSI bus clock P1.7 SDA：TWSI bus data
RST	9	4	10	**Reset**: A high on this pin for two machine cycles while the oscillator is running resets the device. An internal resistor to VSS permits a power-on reset using only an external capacitor to VCC.
P2.0 – P2.7	21,22,23,24, 25,26,27,28	18,19,20,21 22,23,24,25	24,25,26,27, 28,29,30,31	**Port 2:** Port 2 is an 8-bits bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: IIL). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bits addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bits addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
P3.0 – P3.7	10,11,12,13 14,15,16,17	5,7,8,9, 10,11,12,13	11, 13,14,15, 16,17,18,19	**Port 3**: Port 3 is an 8-bits bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: IIL). Port 3 also serves the special features. Port Pin Alternative function P3.0 RxD UART input P3.1 TxD UART output P3.2 #EX0 external interrupt 0 P3.3 #EX1 external interrupt 1 P3.4 T0: Timer 0 external input P3.5 T1: Timer 1 external input P3.6 #WR External data memory write strobe P3.7 #RD External data memory read strobe

MNEMONIC	PDIP 40 pin	PQFP 44 Pin	PLCC 44 pin	Names and Functions
ALE	30	27	33	**Address Latch Enable:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. Setting SFR SCONF.0 can disable ALE. With this bit set, ALE will be active only during a MOVX instruction.
#PSEN	29	26	32	**Program Store Enable:** The read strobe to external program memory. When executing code from the external program memory, #PSEN is activated twice each machine cycle, except that two #PSEN activations are skipped during each access to external data memory. #PSEN is not activated during fetches from internal program memory.
#EA	31	29	35	**External Access Enable**: #EA must be externally held low to enable the device to fetch code from external program memory locations. If #EA is held high, the device executes from internal program memory.
X1	19	15	21	**Crystal 1**: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
X2	18	14	20	**Crystal 2**: Output from the inverting oscillator amplifier.

SFR Mapping

The special function register of SM5964A fall into the following categories

- C51 CORE register: ACC, B, DPL, DPH, PSW, SP
- I/O ports: P0,P1, P2, P3, P4, P1CON
- Timer/Counter register: T2CON, T2MOD, TCON, TMOD, TH0, TH1, TH2, TL0, TL1, TL2, RCAP2L, RCAP2H
- UART I/O register: SBUF, SCON
- TWSI bus register: TWSIS, TWSIA, TWSIC1, TWSIC2, TWSITXD, TWSIRXD
- Power and system control register: PCON, SCONF
- Interrupt system register: IP, IE, IP1, IE1, IFR
- IAP Flash programming register :ISPFAH, ISPFAL, ISPFD, ISPC
- PWM output register: PWMC0, PWMC1, PWMD0, PWMD1

Table 1 SFR Map

$F8									$FF
$F0	B 0000 0000				**ISPFAH** 0000 0000	**ISPFAL** 0000 0000	**ISPFD** 0000 0000	**ISPC** 0000 0000	$F7
$E8									$EF
$E0	ACC 0000 0000								$E7
$D8	**P4** xxxx 1111								$DF
$D0	PSW 0000 0000			**PWMC0** 0000 0000	**PWMC1** 0000 0000				$D7
$C8	T2CON 0000 0000	**T2MOD** xxxx xx00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			$CF
$C0	**TWSIS** 0000 0000	**TWSIA** 1010 0000	**TWSIC1** 0000 0001	**TWSIC2** 0000 0000	**TWSITXD** 1111 1111	**TWSIRXD** 0000 0000			$C7
$B8	IP 0000 0000	**IP1** 0000 0000						**SCONF** 0000 0000	$BF
$B0	P3 1111 1111			**PWMD0** 0000 0000	**PWMD1** 0000 0000				$B7
$A8	IE 0000 0000	**IE1** 0000 0000	**IFR** 0000 0000						$AF
$A0	P2 1111 1111								$A7
$98	SCON 0000 0000	SBUF xxxx xxxx		**P1CON** 0000 0000					$9F
$90	P1 1111 1111								$97
$88	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000			$8F
$80	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000		**RCON** 0000 0000		PCON 0000 0000	$87

Table 2 : All SFR list (8051, I/O, Timer, UART, TWSI, System, Interrupt)

Symbol	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
8051 Core											
ACC	Accumulator	E0H									00H
B	B register	F0H									00H
SP	Stack Pointer	81H									07H
PSW	Process Status	D0H	CY	AC	F0	RS1	RS0	OV		P	00H
DPH	Data Pointer High	83H									00H
DPL	Data Pointer Low	82H									00H
I/O PORT											
P0	Port 0	80H	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFH
P1	Port 1	90H	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFH
P2	Port 2	A0H	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFH
P3	Port 3	B0H	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFH
P4	Port 4	D8H					P4.3	P4.2	P4.1	P4.0	XFH
P1CON	P1 Control	9BH	SDAE	SCLE			PWM1E	PWM0E	-	-	00H
TIMER / Counter											
TCON	Timer Control register	88H	TF1	TF1	TF0	TR0	IE1	IT1	IE0	IT0	00H
TMOD	Timer Mode	89H	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
TH0	Timer 0 High	8CH									00H
TL0	Timer 0 Low	8AH									00H
TH1	Timer 1 High	8DH									00H
TL1	Timer 1 Low	8BH									00H
T2CON	Timer 2 Control	C8H	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00H
T2MOD	Timer 2 Mode	C9H							T2OE	DCEN	X0H
RCAP2H	RCAP2 High	CBH									00H
RCAP2L	RCAP2 Low	CAH									00H
TH2	Timer 2 High	CDH									00H
TL2	Time 2 Low	CCH									00H
UART											
SCON	UART Control	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SBUF	UART Buffer	99H									XXH
TWSI BUS											
TWSIS	TWSI bus status	C0H	RXIF	TXIF	TFIF	NAKIF		RXAK	MASTER	TXAK	00H
TWSIA	TWSI address	C1H									A0H
TWSIC1	TWSI control 1	C2H	TWSIE				Bus Busy	TWSIFS2	TWSIFS1	TWSIFS0	01H
TWSIC2	TWSI Control 2	C3H	Match	SRW			RESTART			MRW	00H
TWSITXD	TWSI Transmit Data	C4H									FFH
TWSIRXD	TWSI Received Data	C5H									00H
Power and System											
PCON	Power Control register	87H	SMOD				GF1	GF0	PD	IDLE	00H
SCONF	System Control	BFH				PDWUE		ISPE	OME	ALEI	00H
Interrupt system											
IE	Interrupt Enable	A8H	EA		ET2	ES0	ET1	EX1	ET0	EX0	00H
IE1	Interrupt Enable 1	A9H							ETWSI		00H
IFR	Interrupt Flag 1	AAH							TWSIIF		00H
IP	Interrupt Priority	B8H			PT2	PS0	PT1	PX1	PT0	PX0	00H
IP1	Interrupt Priority 1	B9H							PTWSI		00H
Data Memory											
RCON	Internal RAM Control	85H							RAMS1	RAMS0	00H
ISP FLASH memory											
ISPFAH	ISP Address high	F4H									00H
ISPFAL	ISP Address low	F5H									00H
ISPFD	ISP Data	F6H									00H
ISPC	ISP Control	F7H	START						ISPF1	ISPF0	00H
PWM output											
PWMC0	PWM 0 Control	D3H						PBS	PFS1	PFS0	00H
PWMC1	PWM 1 Control	D4H						PBS	PFS1	PFS0	00H
PWMD0	PWM 0 Data	B3H	PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0	00H
PWMD1	PWM 1 Data	B4H	PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0	00H

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	0	25	70	℃	Ambient temperature under bias

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VCC33	Supply voltage	3.0	3.3	3.6	V	
Fosc 25	Oscillator Frequency			25	MHz	For 3.3V application

DC Characteristic

VCC = 3.3V (±10%), VSS=0V TA= 0℃ to +70℃

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	Supply Voltage		3.0	3.6	V
I_{CC}	Supply current operating	See notes 1 f_{CLK} = 12MHz V_{CC} = 3.6V		10	mA
I_{ID}	Supply current IDLE mode	See note 2 f_{CLK} = 12MHz V_{CC} = 3.6V		5	mA
I_{PD}	Supply current Power-Down mode	See note 3 2V < V_{PC} < V_{CCmax}		20	μA
INPUT					
VIL1	Input LOW voltage, Port 0,1,2,3,4,/EA		-0.5	0.8	V
VIL2	Input LOW voltage, RES, XTAL1		0	0.8	V
VIH1	Input HIGH voltage, Port 0,1,2,3,4,EA		2.0	Vcc+0.2	V
VIH2	Input HIGH voltage, RES, XTAL1		70% VCC	Vcc+0.2	V
IIL1	Input current LOW level Port 1,2,3,4 (except P1.6,P1.7)	VIN = 0.45V		-50	μA
IIL2	Input current LOW level Port 0,P1.6,P1.7	VIN = 0.45V		-650	μA
ITL	Transition current High to Low Port 1,2,3,4	VIN = 1.5 V		-650	μA
ILI	Input leakage current	0.45V < VIN < VCC		10	μA
ISK1	Sink Current Port 1, 2, 3, 4	VCC = 3.3V, VIN = 0.4 V	3	6	mA
ISK2	Sink Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 0.4 V	4	8	mA
ISR1	Source Current Port 1, 2, 3, 4	VCC = 3.3V, VIN = 2.4 V	-40	-80	uA
ISR2	Source Current Port 0,ALE, /PSEN	VCC = 3.3V, VIN = 2.4 V	-4	-8	mA
OUTPUT					
V_{OL1}	Output LOW voltage, Port 0,ALE, /PSEN	I_{OL} = 3.2mA，V_{CC}=3.3V		0.4	V
V_{OL2}	Output LOW voltage, Port 1, 2, 3, 4	I_{OL} = 1.6mA，V_{CC}=3.3V		0.4	V
V_{OH1}	Output High voltage Port0 ALE, /PSEN	I_{OH} = -300uA，V_{CC}=3.3V	2.4		V
V_{OH1}	Output High voltage Port 1,2,3,4	I_{OH} = -20μA，V_{CC}=3.3V	2.4		V
R_{RST}	Internal RESET pull-down resistor	VCC=3.6V	50	300	kΩ
C_{IO}	Pin capacitance	Test freq=1MHz, T_A=25℃		10	pF

NOTES FOR DC ELECTRICAL CHARACTERISTICS

1. The operating supply current is measured with all output disconnected;
   XTAL1 driven with $t_r = t_f$ = 5ns; V_{IL} = V_{SS}+0.5V; V_{IH}=V_{CC}-0.5V; XTAL2 not connect;/EA=RST=Port0=V_{DD};
2. The IDLE MODE supply current is measured with all output pins disconnected;
   XTAL1 driven with $t_r = t_f$ = 5ns; V_{IL} = V_{SS}+0.5V; V_{IH}=V_{CC}-0.5V; XTAL2 not connect;/EA= Port0=V_{DD};
3. The POWER-DOWN MODE supply current is measured with all output pins disconnected;
   V_{IL} = V_{SS}+0.5V; V_{IH}=V_{CC}-0.5V; XTAL2 not connect; /EA= Port0=V_{DD};
4. Port 1, 2, 3, and 4 sources a transition current when they are being externally driven from HIGH to LOW. The transition current reaches its maximum value when V_{IN} is approximately 2V.
5. Capacities loading on port 0 and 2 may cause spurious noise to be superimposed on V_{OL} of ALE and port 1, 3, and 4. The noise is due to external bus capacitance discharging into port 0 and port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacities loading > 100pF), the noise pulse on the ALE pin may exceed 0.8V. In such cases, it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt trigger STROBE input.
6. Under steady state (non-transient) conditions, IOL must be externally
   Limited as follows:
   Maximum IOL per pin (use sign pin only) : 10mA
   Maximum IOL per 8-bit port : port 0 : 26mA
   port 1,2,3 : 15mA
   Maximum total IOL for all output pins : 71mA

If IOL exceeds the condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

Specifications subject to change without notice contact your sales representatives for the most recent information.

AC Characteristic

V_{CC}=3.3V±10%, V_{SS}=0V, t_{clk} min = 1/ f_{max}(maximum operating frequency)
T_A=0℃ to +70℃
C_L=100pF for Port0, ALE and /PSEN; C_L=80pF for all other outputs unless otherwise specified.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
External Clock drive into XTAL1					
tCLK	4	Xtal1 Period	40(1)	-	ns
tCLKH	4	Xtal1 HIGH time	20	-	ns
tCLKL	4	Xtal1 LOW time	20	-	ns
tCLKR	4	XTAL1 rise time	-	10	ns
tCLKF	4	XTAL1 fall time	-	10	ns
tCYC	4	Controller cycle time = tCLK / 12	3.33	-	ns

NOTES :
1. Operating is 25MHz.

Symbol	FIGURE	PARAMETER	MIN	MAX	UNIT
Program Memory					
1/tCLK	7	System clock frequency	3.0	25	MHz
tLHLL	7	ALE pulse width	2tCLK-40		ns
tAVLL	7	Address valid to ALE low	tCLK-40		ns
tLLAX	7	Address hold after ALE low	tCLK-30		ns
tLLIV	7	ALE LOW to valid instruction in		4tCLK-100	ns
tLLPL	7	ALE LOW to /PSEN LOW	tCLK-30		ns
tPLPH	7	/PSEN pulse width	3tCLK-45		ns
tPLIV	7	/PSEN LOW to valid instruction in		3tCLK-105	ns
tPXIX	7	Input instruction hold after /PSEN	0		ns
tPXIZ	7	Input instruction float after /PSEN		tCLK -25	ns
tAVIV	7	Address to valid instruction in		5tCLK-105	ns
tPLAZ	7	/PSEN low to address float		10	ns
Data Memory					
tAVLL	8,9	Address valid to ALE LOW	tCLK-40		ns
tLLAX	8,9	Address hold after ALE LOW	tCLK-35		ns
tRLRH	8	/RD pulse width	6tCLK-100		ns
tWLWH	9	/WR pulse width	6tCLK-100		ns
tRLDV	8	/RD LOW to valid data in		5tCLK-165	ns
tRHDX	8	Data hold after /RD	0		ns
tRHDZ	8	Data float after /RD		2tCLK-70	ns
tLLDV	8	ALE LOW to valid data in		8tCLK-150	ns
tAVDV	8	Address to valid data in		9tCLK-165	ns
tLLWL	8,9	ALE LOW to /RD or /WR LOW	3tCLK-50	3tCLK+50	ns
tAVWL	8,9	Address valid to /WR or /RD LOW	4tCLK-130		ns
tQVWX	9	Data valid to /WR transition	tCLK-50		ns
tQVWH	9	Data before /WR	7tCLK-150		ns
tWHQX	9	Data hold after /WR	tCLK-50		ns
tRLAZ	8	/RD LOW to address float		0	ns
tWHLH	8,9	/RD or /WR HIGH to ALE HIGH	tCLK-40	tCLK+40	ns
UART					
tXLXL	10	Serial port clock time	12tCLK		ns
tQVXH	10	Output data setup to clock rising edge	10tCLK-133		ns
tXHQX	10	Output data hold after clock rising edge	2tCLK-117		ns
tXHDX	10	Input data hold after clock rising edge	0		ns
tXHDV	10	Clock rising edge to input data valid		10tCLK-133	ns

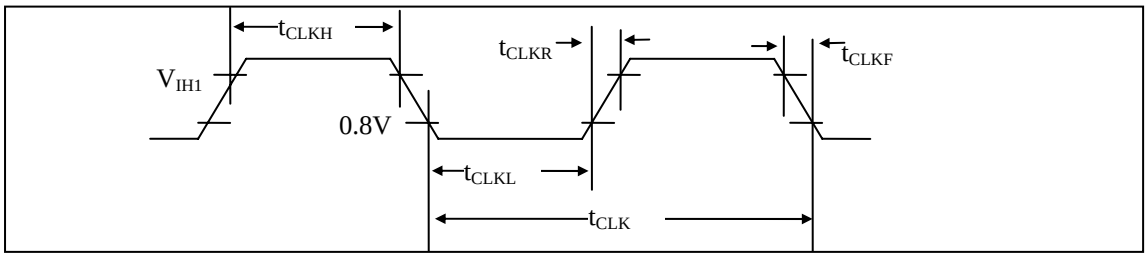


Figure 4 External Clock Drive waveform

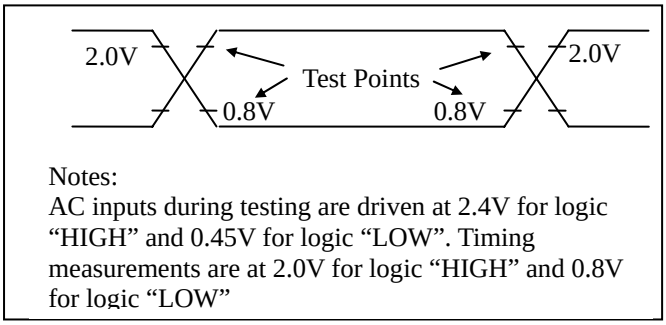


Figure 5 AC Testing Input/Output

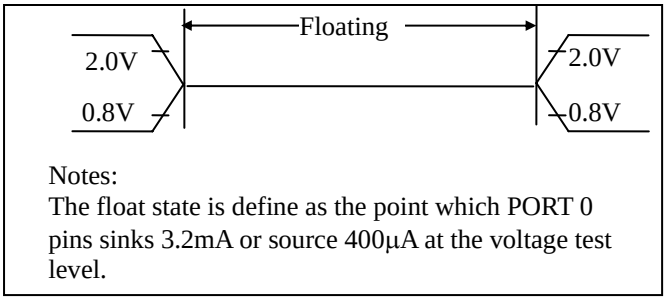


Figure 6 AC Testing, Floating Waveform

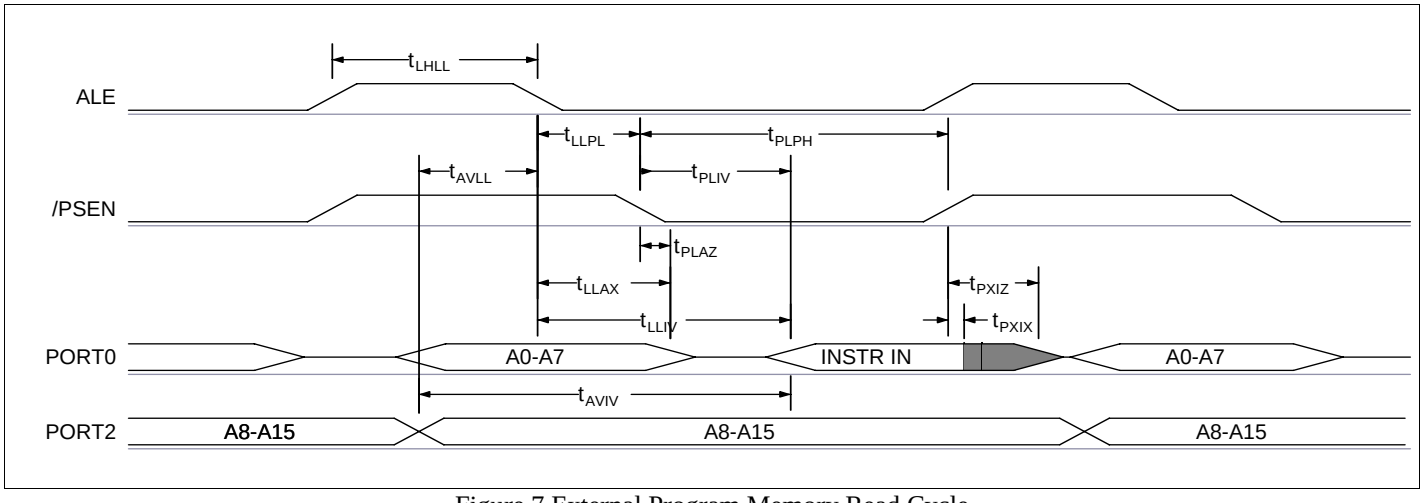


Figure 7 External Program Memory Read Cycle

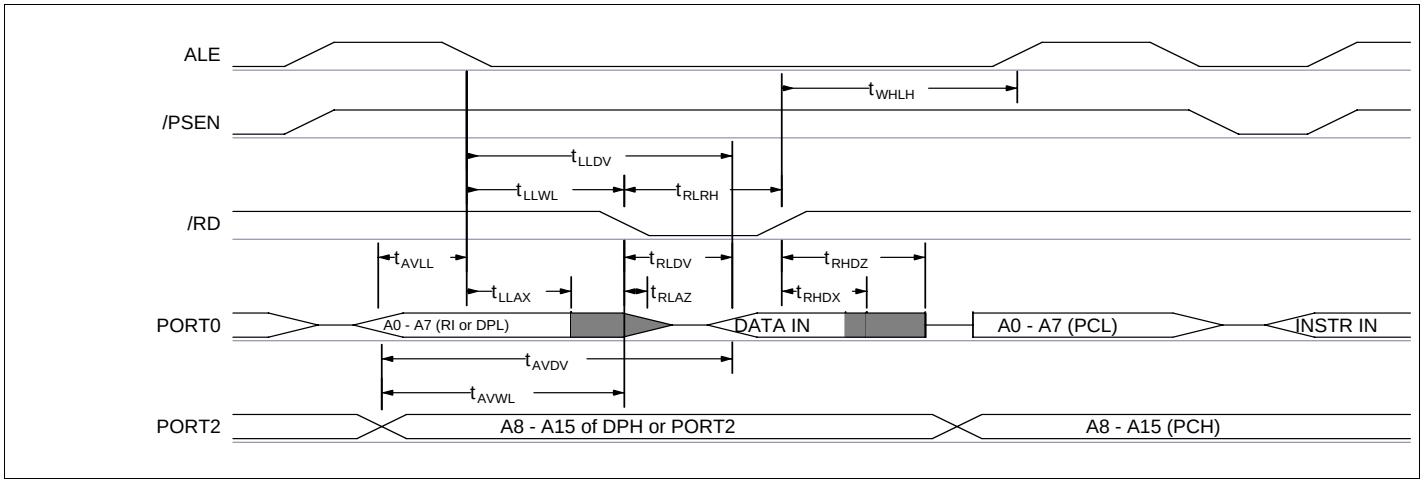


Figure 8 external memory read cycle

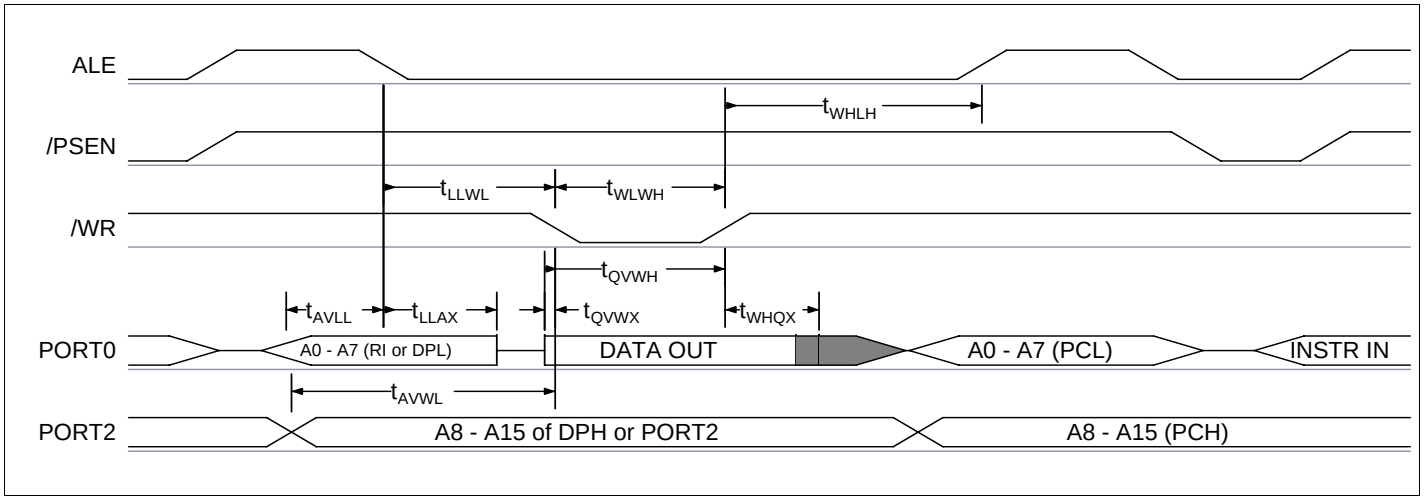


Figure 9 external memory write cycle

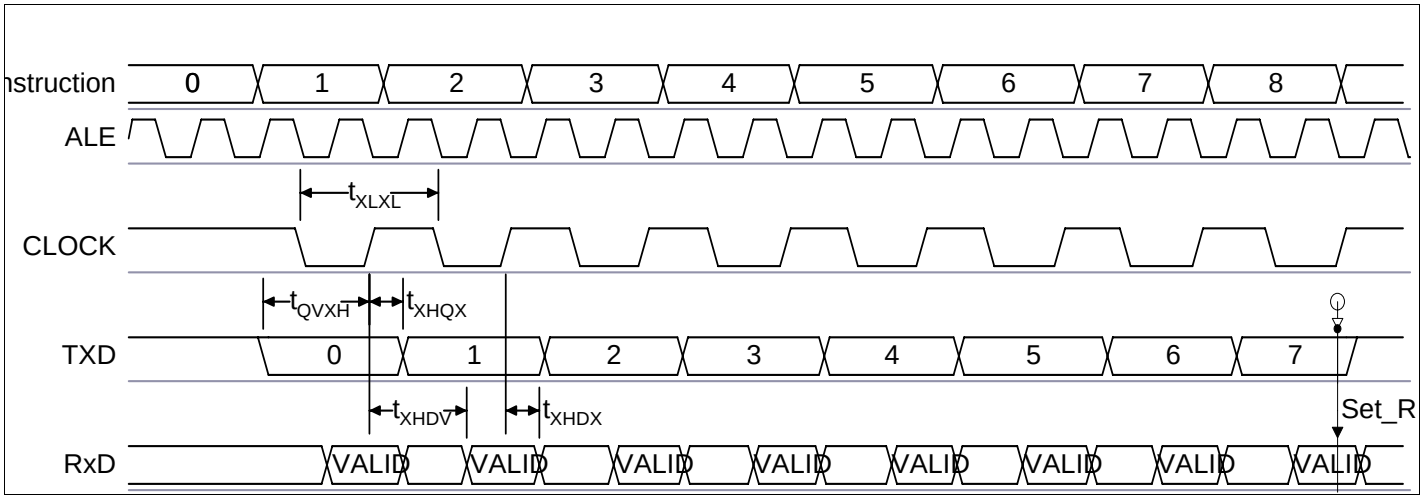


Figure 10 UART waveform in Shift Register MODE

Specifications subject to change without notice contact your sales representatives for the most recent information.

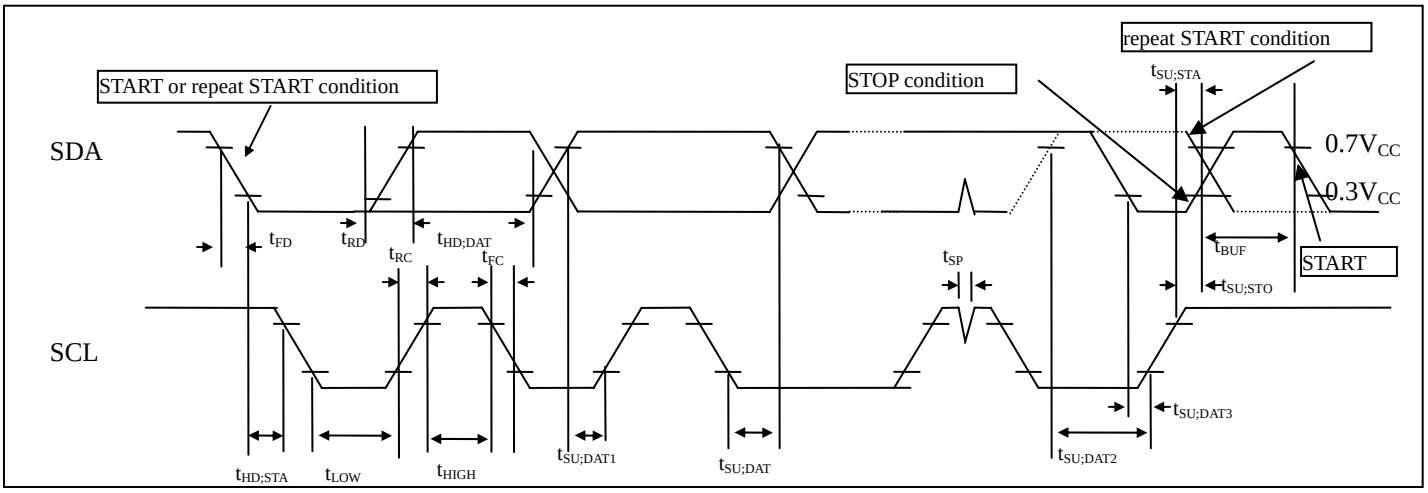


Figure 11 Timing waveform of TWSI interface

Symbol	FIGURE	PARAMETER	Standard-MODE		Fast-MODE		UNIT
			MIN	MAX	MIN	MAX	
TWSI Bus							
f_{SCL}	11	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	11	Bus free time between a stop and stop condition	4.7	-	1.3	-	µS
$t_{HD;STA}$	11	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	-	0.6	-	µS
t_{LOW}	11	Low Period of the SCL clock	4.7	-	1.3	-	µS
t_{HIGH}	11	High period of the SCL clock	4.7	-	1.3	-	µS
$t_{SU;STA}$	11	Set-up time of a repeated START condition	4.0	-	0.6	0	µS
$t_{HD;DAT}$	11	Data hold time	0	-	0	0.9	µS
$t_{SU;DAT}$	11	Data Setup-Time	250	-	100(1)	-	nS
t_{RD},t_{RC}	11	Rise time of both SDA and SCL	-	1000	20+0.1C_b(2)	300	ns
t_{FD} t_{FC}	11	Fall time of both SDA and SCL	-	300	20+0.1C_b(2)	300	ns
$t_{SU;STO}$ $t_{SU;STA}$	11	Set-up time for STOP and START condition	4.0	-	0.6	-	µS
C_b	11	Capacitive load for each bus line	-	400	-	400	pF
t_{SP}	11	Pulse width of spikes which must be suppressed by input filter	-	-	0	50	nS

NOTES:

1. A fast-mode TWSI bus device can be used in a standard-mode TWSI bus system, but the requirement $t_{SU;DAT} \geq 250ns$ must the be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to SDA line $t_{RMAX} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode TWSI bus specification) before the SCL line is released.
2. C_b = Total capacitance of one bus line in pF.

Function Description

The SM5964A is a stand-alone high-performance microcontroller designed for using in 3.3V ISP applications, such as LCD monitor, instrumentation, or high-end consumer applications.
In addition to the 80C51 standard functions, the device provides a number of dedicated hardware functions for these applications.
The SM5964A is a control-oriented CPU with on-chip program and data memory. It can be extended with external data memory up to 64K bytes. For system requiring extra capability, the SM5964A can be enhanced by using external memory and peripherals.
The SM5964A has two software selectable modes of saving power consumption：IDLE and POWER- DOWN. The IDLE mode freezes the CPU while allowing the RAM, timer, serial ports and interrupt system to continue functioning. The POWER-DOWN mode save the RAM contents but freezes the oscillator causing all other chip functions to be inoperative. The POWER-DOWN mode can be terminated by H/W reset, or by any one of the two external interrupt.

CPU

The CPU of SM5964A is compatible to standard 80C51. The structure of this CPU is shown as FIGURE 12. It contains Instruction Register (IR), Instruction Decoder, Program Counter (PC), Accumulator (ACC), B Register, and control logic. This CPU provides a 8-bits bi-direction bus to communicate with other blocks in the chip. The address and data are transferred through on the same 8-bits bus.

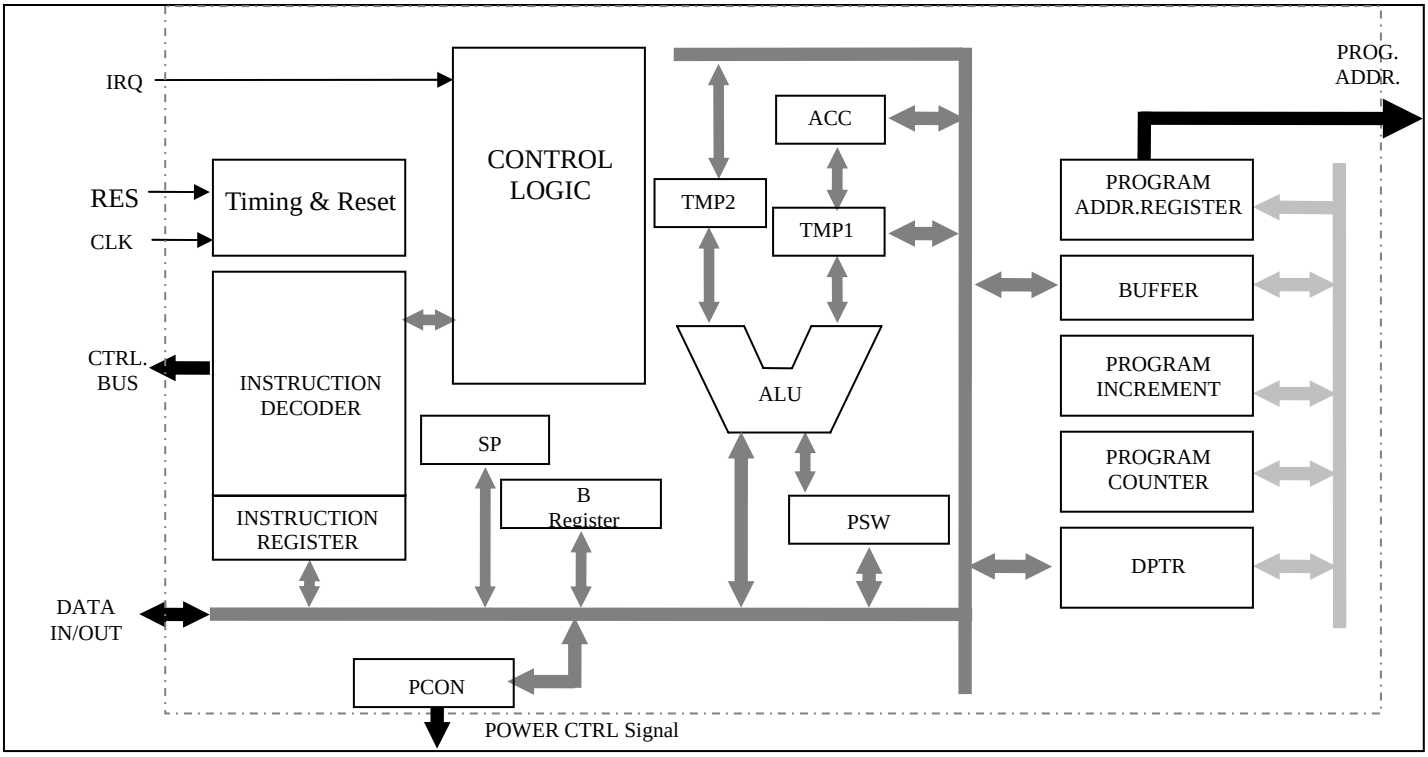


Figure 12 The CPU structure

CPU Timing

The machine cycle consists of a sequence of 6 states, numbered S1 through S6. Each state time lasts for two oscillator periods. Thus a machine cycle takes 12 oscillator periods. Each state is divided into a PHASE1 half and a PHASE2 half. FIGURE 13 shows relationships between oscillator, phase, and S1-S6.

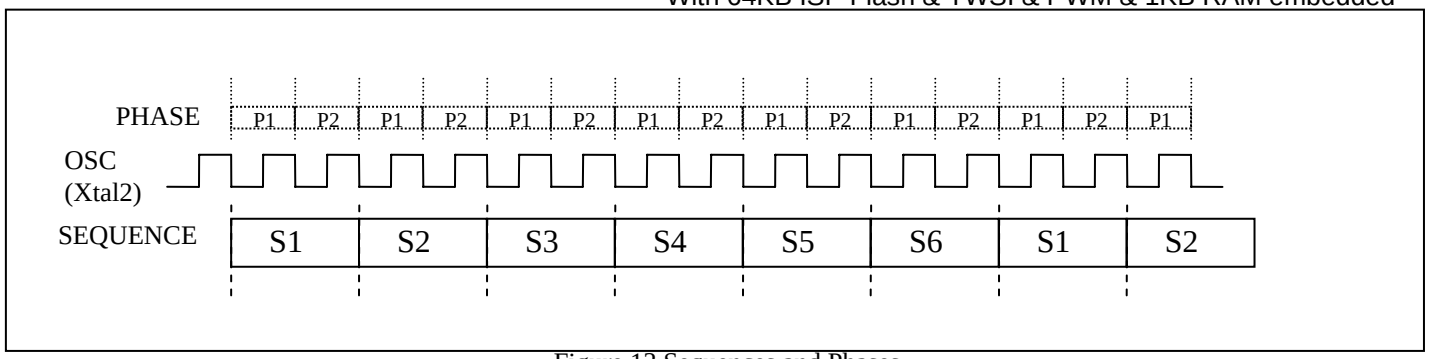


Figure 13 Sequences and Phases

FIGURE 14 shows the fetch / execute sequences in states and phases for various kinds of instructions. Normally the program fetches are generated during each machine cycle, even if the instruction being executed doesn't require it. If the instruction being executed doesn't need more code bytes, the CPU simply ignores the extra fetch, and the PROGRAM COUNTER is incremented accordingly.
Execution of a one-cycle instruction (FIGURE 14 A and B) begins during S1 of the machine cycle, when the OPCODE is latched into INSTRUCTION REGISTER. A second fetch occurs during S4 of the same machine cycle. Execution is completed at the end of S6 of this machine cycle.

The MOVX instructions take two machine cycles to execute. No program fetch is generated during the second cycle of a MOVX instruction. This is the only time program fetches are skipped. The fetch/execute sequence for MOVX instructions is shown in FIGURE 14 (D)

The fetch / execute sequences are the same whether the PROGRAM MEMORY is internal or external to the chip. Execution times do not depend on whether the PROGRAM MEMORY is internal or external.

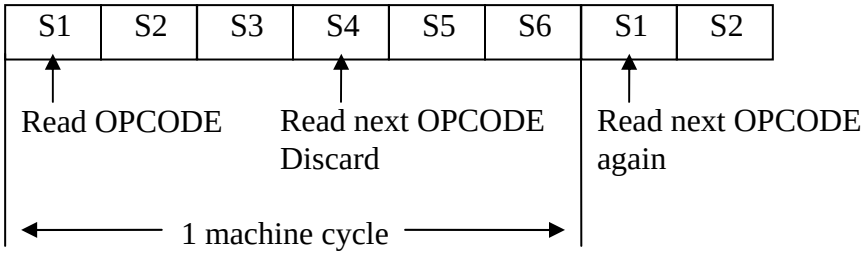
FIGURE 15 shows the signals and timing involved in program fetches when the program memory is external. If PROGRAM MEMORY is external, the PROGRAM MEMORY READ STOBE (/PSEN) is normally activated twice per machine cycle, as shown in FIGURE 15(A).

If an access external DATA MEMORY occurs, as shown in FIGURE 15(B), two (/PSEN) are SKIPPED, because the address and data bus are being used for DATA MEMORY access.

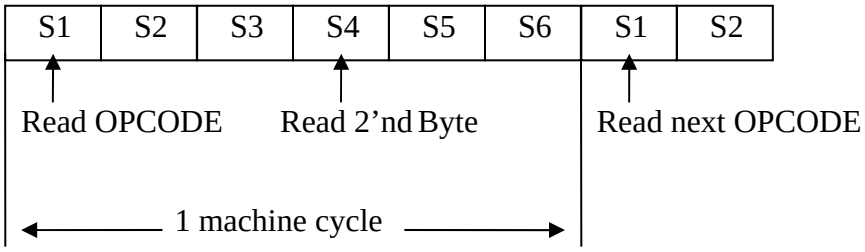
Note that a DATA MEMORY bus cycle takes twice as much time as PROGRAM MEMORY bus cycle. FIGURE 15 shows the relative time of the address begin emitted at PORT0 and PORT2, and of ALE and /PSEN. ALE is used to latch the low address byte form PORT0 into the address latch.

When CPU is executing from internal PROGRAM MEMORY, /PSEN is not activated, and program address are not emitted. However, ALE continues to be activated twice per machine cycle and so is available as clock output signal. Note, however, that ALE is skipped during the execution of the MOVX instruction.

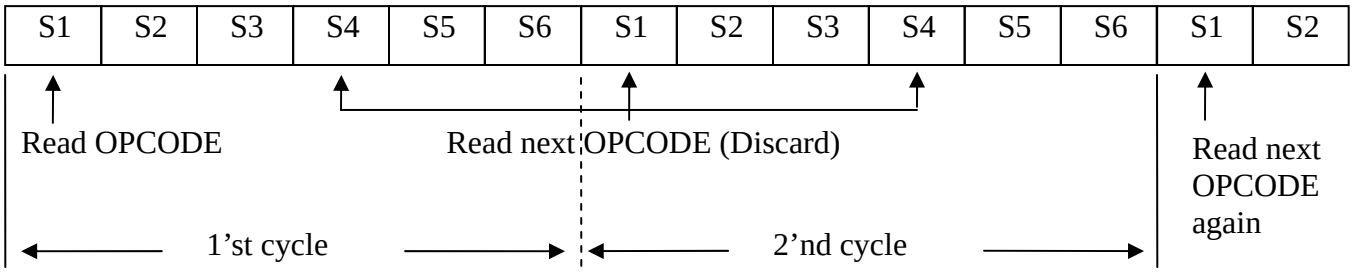
A.) 1 byte, 1 Cycle Instruction



B.) 2 byte, 1 Cycle Instruction



C.) 1 byte, 2 Cycle Instruction



D.) MOVX: 1 byte, 2 Cycle Instruction ACCESS external memory

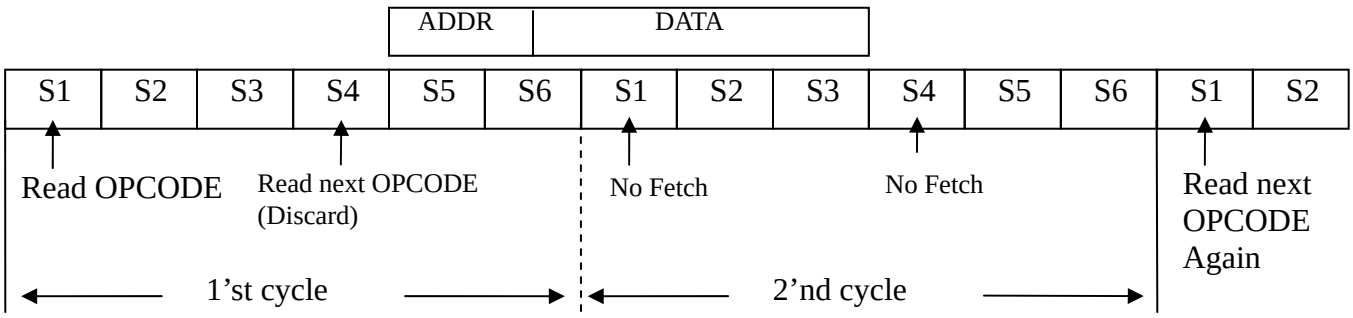


Figure 14 Timing of various instructions

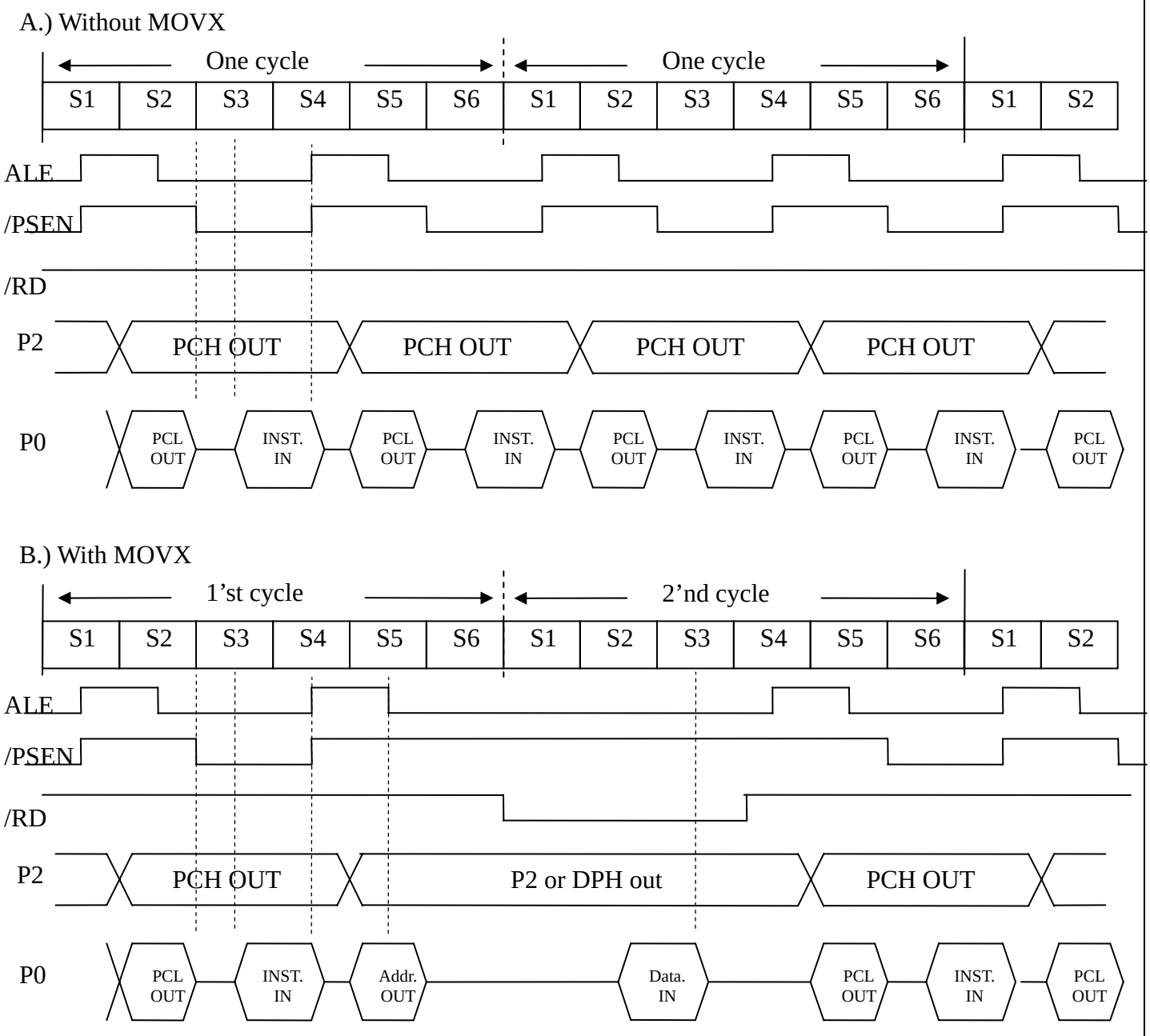


Figure15: Bus cycle in external program memory mode

Instruction Set

The SM5964A uses the powerful instruction set of 80C51. It consists of 49 single-byte, 42 two-byte, and 15 three- byte instructions. Among them 63 instructions are executed in 1 machine-cycle, 46 instructions in 2 machine-cycles, and the multiply, 2 instructions in 4 machine-cycles.
A summary of the instruction set is given in Table 4.

Addressing Mode

Notes on instruction set and address modes:

Rn		Register R7-R0 of the currently selected register bank.
direct		8-bits internal data location's address. This could be internal DATA RAM location (0-127) or a SFR [i.e., I/O port, control register, status register, etc. (128-255)]
@Ri		8-bits RAM location addressed indirectly through register R1 or R0 of the actual register bank
#data		8-bits constant included in the instruction
#data16		16-bits constant included in the instruction
addr11		11-bits destination address. Used by ACALL and AJMP. The branch can be anywhere within the same 2 K bytes page of program memory as the first byte of the following instruction.
rel		Signed (2's complement) 8-bits offset byte. Used by SJMP and all conditional jumps. Range is -128 to +127 bytes relative to first byte of the following instruction.
bit		Direct addressed bit in internal data RAM or SFR

Table 4: A Summary of the instruction set

Mnemonic		**OPERATION**	**BYTE**	**CYCLE**
Arithmetic Instructions				
ADD	A,Rn	A = A + Rn	1	1
ADD	A,direct	A = A + direct	2	1
ADD	A,@Ri	A = A + <@Ri>	1	1
ADD	A,#data	A = A + #data	2	1
ADDC	A,Rn	A = A + Rn + C	1	1
ADDC	A,direct	A = A + direct + C	2	1
ADDC	A,@Ri	A = A + @Ri + C	1	1
ADDC	A,#data	A = A + #data + C	2	1
SUBB	A,Rn	A = A — Rn — C	1	1
SUBB	A,direct	A = A — direct — C	2	1
SUBB	A,@Ri	A = A — <@Ri> — C	1	1
SUBB	A,#data	A = A—#data — C	2	1
INC	A	A = A + 1	1	1
INC	Rn	Rn = Rn + 1	1	1
INC	direct	direct = direct + 1	2	1
INC	@Ri	<@Ri> = <@Ri> + 1	1	1
DEC	A	A = A — 1	1	1
DEC	Rn	Rn = Rn — 1	1	1
DEC	direct	direct = direct — 1	2	1
DEC	@Ri	<@Ri> = <@Ri> — 1	1	1
INC	DPTR	DPTR = DPTR — 1	1	2
MUL	AB	B:A = A × B	1	4
DIV	AB	A = INT (A/B) B = MOD (A/B)	1	4
DA	A	Decimal adjust ACC	1	1
Logical Instructions				
ANL	A,Rn	A .AND. Rn	1	1
ANL	A,direct	A .AND. direct	2	1
ANL	A,@Ri	A .AND. <@Ri>	1	1
ANL	A,#data	A .AND. #data	2	1
ANL	direct,A	direct .AND. A	2	1
ANL	direct,#data	direct .AND. #data	3	2
ORL	A,Rn	A .OR. Rn	1	1
ORL	A,direct	A .OR. direct	2	1
ORL	A,@Ri	A .OR. <@Ri>	1	1
ORL	A,#data	A .OR. #data	2	1
ORL	direct,A	direct .OR. A	2	1
ORL	direct,#data	direct .OR. #data	3	2
XRL	A,Rn	A .XOR. Rn	1	1
XRL	A,direct	A .XOR. direct	2	1
XRL	A,@Ri	A .XOR. <@Ri>	1	1
XRL	A,#data	A .XOR. #data	2	1
XRL	direct,A	direct .XOR. A	2	1
XRL	direct,#data	direct .XOR. #data	3	2
CLR	A	A = 0	1	1

CPL	A	A = /A	1	1
RL	A	Rotate ACC Left 1 bit	1	1
RLC	A	Rotate Left through Carry	1	1
RR	A	Rotate ACC Right 1 bit	1	1
RRC	A	Rotate Right through Carry	1	1
SWAP	A	Swap Nibbles in A	1	1
Data Transfers Instructions				
MOV	A,Rn	A = Rn	1	1
MOV	A,direct	A = direct	2	1
MOV	A,@Ri	A = <@Ri>	1	1
MOV	A,#data	A = #data	2	1
MOV	Rn,A	Rn = A	1	1
MOV	Rn,direct	Rn = direct	2	2
MOV	Rn,#data	Rn = #data	2	1
MOV	direct,A	direct = A	2	1
MOV	direct,Rn	direct = Rn	2	2
MOV	direct,direct	direct = direct	3	2
MOV	direct,@Ri	direct = <@Ri>	2	2
MOV	direct,#data	direct = #data	2	1
MOV	@Ri,A	<@Ri> = A	1	1
MOV	@Ri,direct	<@Ri> = direct	2	2
MOV	@Ri,#data	<@Ri> = #data	2	1
MOV	DPTR,#data16	DPTR = #data16	3	2
MOVC	A,@A+DPTR	A = code memory[A+DPTR]	1	2
MOVC	A,@A+PC	A = code memory[A+PC]	1	2
MOVX	A,@Ri	A = external memory[Ri] (8-bits address)	1	2
MOVX	A,@DPTR	A = external memory[DPTR] (16-bits address)	1	2
MOVX	@Ri,A	external memory[Ri] = A (8-bits address)	1	2
MOVX	@DPTR,A	external memory[DPTR] = A (16-bits address)	1	2
PUSH	direct	INC SP: MOV “@’SP’, < direct >	2	2
POP	direct	MOV < direct >, “@SP”: DEC SP	2	2
XCH	A,Rn	ACC and < Rn > exchange data	1	1
XCH	A,direct	ACC and < direct > exchange data	2	1
XCH	A,@Ri	ACC and < Ri > exchange data	1	1
XCHD	A,@Ri	ACC and @Ri exchange low nibbles	1	1
Boolean Instructions				
CLR	C	C = 0	1	1
CLR	bit	bit = 0	2	1
SETB	C	C = 1	1	1
SETB	bit	bit = 1	2	1
CPL	C	C = /C	1	1
CPL	bit	bit = /bit	2	1
ANL	C,bit	C = C .AND. bit	2	2
ANL	C,/bit	C = C .AND. /bit	2	2
ORL	C,bit	C = C .OR. bit	2	2
ORL	C,/bit	C = C .OR. /bit	2	2
MOV	C,bit	C = bit	2	1
MOV	bit,C	bit = C	2	2
JC	rel	Jump if C= 1	2	2
JNC	rel	Jump if C= 0	2	2
JB	bit,rel	Jump if bit = 1	3	2
JNB	bit,rel	Jump if bit = 0	3	2
JBC	bit,rel	Jump if C = 1	3	2
Jump Instructions				
ACALL	addr11	Call Subroutine only at 2k bytes Address	2	2
LCALL	addr16	Call Subroutine in max 64K bytes Address	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr11	Jump only at 2k bytes Address	2	2
LJMP	addr16	Jump to max 64K bytes Address	3	2
SJMP	rel	Jump on at 256 bytes	2	2
JMP	@A+DPTR	Jump to A+ DPTR	1	2
JZ	rel	Jump if A = 0	2	2
JNZ	rel	Jump if A ≠ 0	2	2
CJNE	A, direct,rel	Jump if A ≠ < direct >	3	2

CJNZ	A, #data,rel	Jump if A ≠ < #data >	3	2
CJNZ	Rn, #data,rel	Jump if Rn ≠ < #data >	3	2
CJNZ	@Ri, #data,rel	Jump if @Ri ≠ < #data >	3	2
DJNZ	Rn,rel	Decrement and jump if Rn not zero	2	2
DJNZ	direct,rel	Decrement and jump if direct not zero	3	2
NOP		No Operation	1	1

Memory organization

The central processing unit (CPU) manipulates operands in three memory spaces; there are 1024 bytes internal data memory (consisting of 256 bytes standard RAM and 768 bytes AUX-RAM) and 64K bytes internal/external program memory (see FIGURE 16)

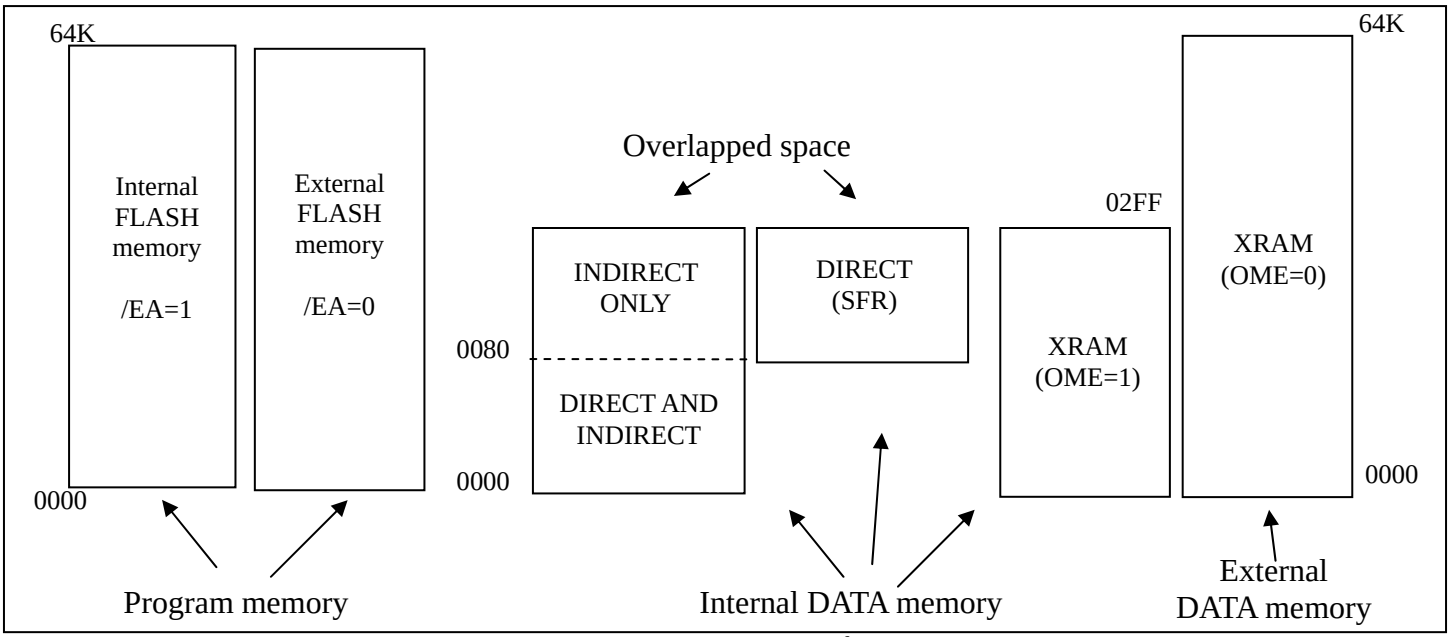


Figure 16 Memory organization of SM5964A

Program memory

The program memory of SM5964A consists of 64K bytes FLASH memory on chip. If during RESET, the /EA pin was held HIGH, the SM5964A does not execute out of the internal program memory. If the /EA pin was held LOW during RESET the SM5964A fetch all instructions from the external program memory. The FLASH memory of SM5964A can be programmed during the program is running by using ISP. Normally, a Writer is used for programming. The feature of FLASH memory is shown as following:

- **READ:** byte-wise
- **WRITE:** byte-wise within 30us (previously erased by a chip erase).
- **ERASE:**
  Full Erase (64K bytes) within 2 sec.
  Erased bytes contain FFH
- **Endurance :** 10K erase and write cycles each byte at TA=25℃
- **Retention :** 10 years

Program Code Security

MOVC instruction executed from external program memory space will not be able to fetch internal codes from on chip program memory after the chip is protected on the Writer.

Internal Data memory

The Data memory of SM5964A consists of 1024 bytes internal data memory (256 bytes standard RAM and 768 bytes AUX-RAM). The AUX-RAM is enable by SCONF.1 ($BF.1), and read/write by MOVX

Internal RAM Control Register (RCON, $85)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						RAMS1	RAMS0

SM5964A has 768 byte on-chip RAM which can be accessed by external memory addressing method only. (By instruction MOVX). The address space of instruction MOVX @Rn is determined by bit 1 and bit 0 (RAMS1, RAMS0) of RCON. The default setting of RAMS1, RAMS0 bits is 00 (page0).

Pulse Width Modulation (PWM)

The PWM output pins are P1.2 and P1.3.
The PWM clock is {FOSC/ (2xDivider)}, the PWM output frequency is {(PWM clock)/32} at 5 bits resolution and {(PWM clock)/256} at 8 bits resolution.
The PWM SFR has shown as below:

PWMC [0:1] ($D3H and $D4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					PBS	PFS1	PFS0

PBS: when set, the PWM is 5 bits resolution.
PFS [1:0]: The PWM clock divider select.

PFS1	PFS0	PWM clock divider select
0	0	2
0	1	4
1	0	8
1	1	16

PWMD [0:1] ($B3H and $B4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWMD.7	PWMD.6	PWMD.5	PWMD.4	PWMD.3	PWMD.2	PWMD.1	PWMD.0

Two-Wire Series Interface (TWSI)

The TWSI module uses the SCL (clock) and the SDA (data) line to communicate with external TWSI interface between other TWSI parts. The speed can up to 400K bps (max.) by software setting the TWSIFS [2:0].
The TWSI module used SFR shown as below
TWSI Status Register:

TWSIS ($C0H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RXIF	TXIF	TFIF	NAKIF		RXAK	MASTER	TXAK

RXIF: The data Receive Interrupt Flag (RXIF) is set after the TWSIRxD (TWSI Receive Data Buffer) is loaded with a newly receive data.
TXIF: The data Transmit Interrupt Flag (TXIF) is set when the data of the TWSITxD (TWSI Transmit Data Buffer) is downloaded to the shift register or the TWSIA is downloaded to the shift register at Master Transmit mode.
TFIF: The Transmit Fail Interrupt Flag is set when the data transmit fail.

NAKIF: The Non-acknowledge Interrupt Flag is only set in the master mode when there is no acknowledge bit detected after one byte data or calling address is transferred.
RXAK: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data transmit on the bus.
MASTER: This bit define this module is working at master mode.
TXAK: The Acknowledge status transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and transmit to master to indicate the receive status.

TWSIA ($C1H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TWSIA.7	TWSIA.6	TWSIA.5	TWSIA.4	TWSIA.3	TWSIA.2	TWSIA.1	EXTADDR

TWSIA [7:1]: TWSI Address registers 7 bits.
EXTADDR: Its only compare 4 bits MSB when set this bit.

TWSIC1 ($C2H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TWSIE				BusBusy	TWSIFS2	TWSIFS1	TWSIFS0

TWSIE: enable TWSI module.
BusBusy: When start condition is detected, this bit will set. When stop condition is detected, this bit will clear.
TWSIFS [2:0]: The TWSI SCL speed divider select.

TWSIFS [2:0]	Speed
000	Xtal/32
001	Xtal/64(default)
010	Xtal/128
011	Xtal/256
100	Xtal/512
101	Xtal/1024
110	Xtal/2048
111	Xtal/4096

TWSIC2 ($C3H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MATCH	SRW			RESTART			MRW

MATCH: When the first received data (following the START signal) in TWSIRxD register is matches with the address that address register (TWSIA) set, this bit will set.
SRW: The slave mode read (received) or wrote (transmit) on the TWSI bus. When this bit is clear, the slave module received data on the TWSI bus (SDA).
RESTART: This bit only set by master mode. The master will send a start signal then send TWSIA after the ACK signal when this bit setting. If TFIF was set (the NonACK signal was received), the master mode will release, and this bit will clear.
MRW: This bit is determined the data transmit direction. And this bit will transmit to bus as bit0 at Address (Address is collection TWSIA [7:1] and MRW as 8 bits data). When clear this bit the master is in transmits mode and clear is in receive mode.

TWSITXD ($C4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TWSITxD.7	TWSITxD.6	TWSITxD.5	TWSITxD.4	TWSITxD.3	TWSITxD.2	TWSITxD.1	TWSITxD.0

The data written into this register will be automatically downloaded to the shift register when the module detects a calling address is matched and the bit 0 of the received data is one (Slave transmit mode) or when the data in the shift register has been transmitted with received acknowledge bit (RXAK) =0 in transmit

mode.

TWSIRXD ($C5)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TWSIRxD.7	TWSIRxD.6	TWSIRxD.5	TWSIRxD.4	TWSIRxD.3	TWSIRxD.2	TWSIRxD.1	TWSIRxD.0

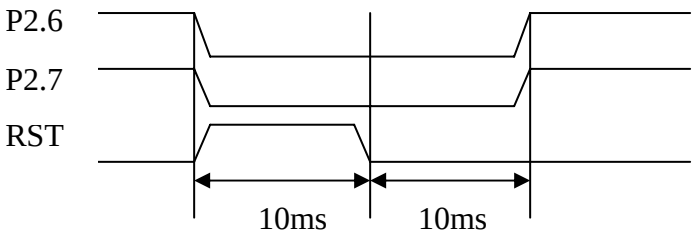
The TWSI Receive Data Buffer (TWSIRxD) contains the last received data when the MATCH flag is one or the calling address from master when the MATCH flag is zero. The TWSIRxD register will be updated after a data byte is received and the previous received data had been read out, otherwise the TWSI module will pull down to SCL line to inhabit the next data transfer. It is a read-only register. The read operation of this register will clear the RXIF flag. After the RXIF flag is cleared, the register can load the received data again and set the RXIF flag to generate interrupt request for reading the newly received data.

In-System Programming (ISP)

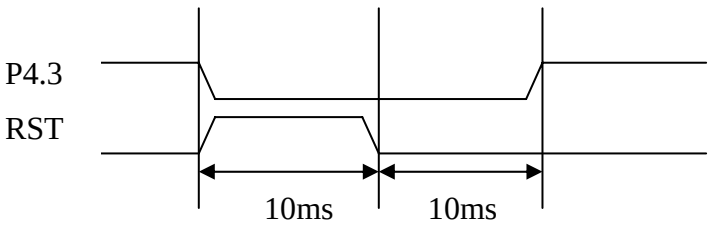
The SM5964A can generator flash control signal by internal hardware circuit. That only need to put the ISP service code into ISP code area (4 Kbytes and divided by 8 zones)
The area is set by lock-bit (N), the lock-bit number and ISP code area relation ship shown as below:

Lock-bit number	ISP code area
1	512 bytes (from $FE00h to $FFFF)
2	1K bytes (from $FC00H to $FFFF)
3	1.5 K bytes (from $FA00H to $FFFF)
4	2 K bytes (from $F800H to $FFFF)
5	2.5 K bytes (from $F600H to $FFFF)
6	3 K bytes (from $F400H to $FFFF)
7	3.5 K bytes (from $F200H to $FFFF)
8	4 K bytes (from $F000H to $FFFF)

There are three ways to into ISP code area:
1. Blank reset: Hardware reset with first flash address blank ($0000H = #FFH).
2. Execute the “LJMP” instruction.
3. By hardware setting:



Or



The ISP register:

ISPFAH ($F4H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8

FA15 ~ FA8: flash address-high for ISP function

ISPFAL ($F5H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0

FA7 ~ FA0: flash address-low for ISP function

The ISPFAH & ISPFAL provide the 16-bits flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

ISPFD ($F6H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

FD7 ~ FD0: flash data for ISP function

The ISPFD provide the 8-bits data for ISP function.

ISPC ($F7H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
START						ISPF1	ISPF0

ISPF[1: 0]: ISP function select bit

START: ISP function start bit

= 1: start ISP function which indicated by bit 1, bit 0 (ISPF1, ISPF0)

= 0: no operation

The START bit is read-only by default, software must write three specific values 55H, AAH and 55H sequentially to the ISPFD register to enable the START bit write attribute. That is:

```
Ex：Open ISP function:    MOV ISPFD, #55H
                          MOV ISPFD, #0AAH
                          MOV ISPFD, #55H
```

Any attempt to set START bit will not be allowed without the procedure above.

After START bit set to 1 then the SM5964A hardware circuit will latch address and data bus and hold the program counter until the START bit reset to 0 when ISP function finished. User does not need to check START bit status by software method

ISPF [1:0]	ISP function
00	Byte Program
01	Chip Protect
10	Page erase (512 Bytes)
11	Chip Erase

ISPF[1:0]: ISP function select bits

One page of flash memory is 512 bytes.

To perform byte program / page erase ISP function, user need to specify flash address at first. When performing page erase function, SM5964A will erase entire page which flash address indicated by ISPFAH registers located within the page.

To perform chip erase ISP function, SM5964A will erase all the flash program memory and data flash memory except the

ISP service program space if lock bit N been configured. Also, SM5964A will un-protect the flash memory automatically. To perform chip protect ISP function, all the flash memory will be read all zero.

e.g. ISP service program to do the byte program - to program data of #22H to the address of the $1005H

```
MOV ISPFD, #55H
MOV ISPFD, #0AAH
MOV ISPFD, #55H          ; open ISP function
MOV SCONF, #04H          ; enable SM5964A ISP function
MOV ISPFAH, #10H         ; set flash address-high, 10H
MOV ISPFAL, #05H         ; set flash address-low, 05H
MOV ISPFD, #22H          ; set flash data to be programmed, data = 22H
MOV ISPFC, #80H          ; start to program data of 22H to the flash address of the $1005H
                         ; after byte program finished, START bit of ISPC will reset to 0 automatically
                         ; program counter then point to the next instruction
```

The Power Down Wake Up (PDWU) function

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity is completely stopped and the power consumption is reduced to the lowest possible value. In this state the ALE and PSEN pins are pulled low. The port pins output the values held by their respective SFRs.

PCON ($87H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SMOD				GF1	GF0	PD	IDLE

SMOD: This bit set to ‘1’ to make the UART baud-rate double.
GF1: General-purpose flag bit.
GF0: General-purpose flag bit.
PD: When set to ‘1’ , the MCU will into Power Down mode
IDLE: When set to ‘1’ , the MCU will into IDLE mode

SCONF ($BFH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			PDWUE		ISPE	OME	ALEI

PDWUE: When set to ‘1’, enable the PDWU function.
ISPE: When set to ‘1’, enable the ISP function.

IE ($A8H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EA		ET2	ES0	ET1	EX1	ET0	EX0

EA: When set to ‘1’, enable interrupt global.
ET2: When set to ‘1’, enable Timer2 interrupt.
ES0: When set to ‘1’, enable UART interrupt.
ET1: When set to ‘1’, enable Timer1 interrupt.
EX1: When set to ‘1’, enable external interrupt 1.
ET0: When set to ‘1’, enable Timer0 interrupt.
EX0: When set to ‘1’, enable external interrupt 0.

IE1 ($A9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						ETWSI	

ETWSI: When set to '1', enable the TWSI interrupt.

IFR ($AAH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						TWSIIF	

TWSIIF: When set to '1', enable the TWSI interrupt flag.

TCON ($88H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TF1: Timer 1 overflow flag.
TR1: Timer 1 run control bit.
TF0: Timer 0 overflow flag.
TR0: Timer 0 run control bit.
IE1: External Interrupt 1 edge flag.
IT1: Interrupt 1 type control bit.
IE0: External Interrupt 0 edge flag.
IT0: Interrupt 0 type control bit.

TMOD ($89H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GATE	C/T	M1	M0	GATE	C/T	M1	M0

Note: High 4 bits are Timer1, Low 4 bits are Timer0.

GATE: Gating control when set. Timer/Counter "x" is enabled only while "INTx" pin is high and "TRx" control pin is set. when cleared Timer "x" is enabled whenever "TRx" control bit is set.
C/T: Timer or Counter Selector cleared for Timer operation (input from in=ternal system clock.) Set for Counter operation (input from "Tx" input pin).

M1	M0	Mode	OPERATING
0	0	0	13-bit Timer Mode. 8-bit Timer/Counter THz with TLx as 5-bit prescaler.
0	1	1	16-bit Timer Mode. 16-bit Timer/Counters THx and TLx are cascaded; there is no prescaler.
1	0	2	8-bit Auto Reload. 8-bit auto-reload Timer/Counter THx holds a value which is to be reloaded into TLx each time it overflows.
1	1	3	Split Timer Mode (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits. TH0 is an 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/Counter 1 stopped.

IP ($B8H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		PT2	PS0	PT1	PX1	PT0	PX0

PT2: Timer2 interrupt priority.
PS0: UART interrupts priority.
PT1: Timer1 interrupt priority.
PX1: external interrupt 1 priority.
PT0: Timer0 interrupt priority.

PX0: external interrupt 0 priority.

IP1($B9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						PTWSI	

PTWSI: When set to '1', enable the TWSI interrupt priority.

The Priority structure and vector locations of interrupts:

Source	Flag	Priority level	Vector Address
External interrupt 0	IE0	1(highest)	03H
Timer 0 overflow	TF0	2	0BH
External interrupt 1	IE1	3	13H
Timer 1 overflow	TF1	4	1BH
UART interrupt	RI+TI	5	23H
Timer 2 overflow	TF2+EXF2	6	2BH
TWSI	RXIF+ TXIF+ TFIF+ NAKIF	7	3BH

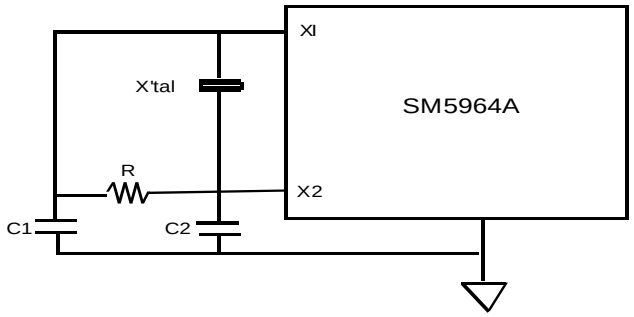
T2MOD ($C9H)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
						T2OE	DCEN

T2OE: Timer2 clock Output Enable bit. If set to 1, the Timer2 clock will output to P1.0.
DCEN: Down Count Enable. When set this bit then allows Timer2 to be configured as an up/down counter.

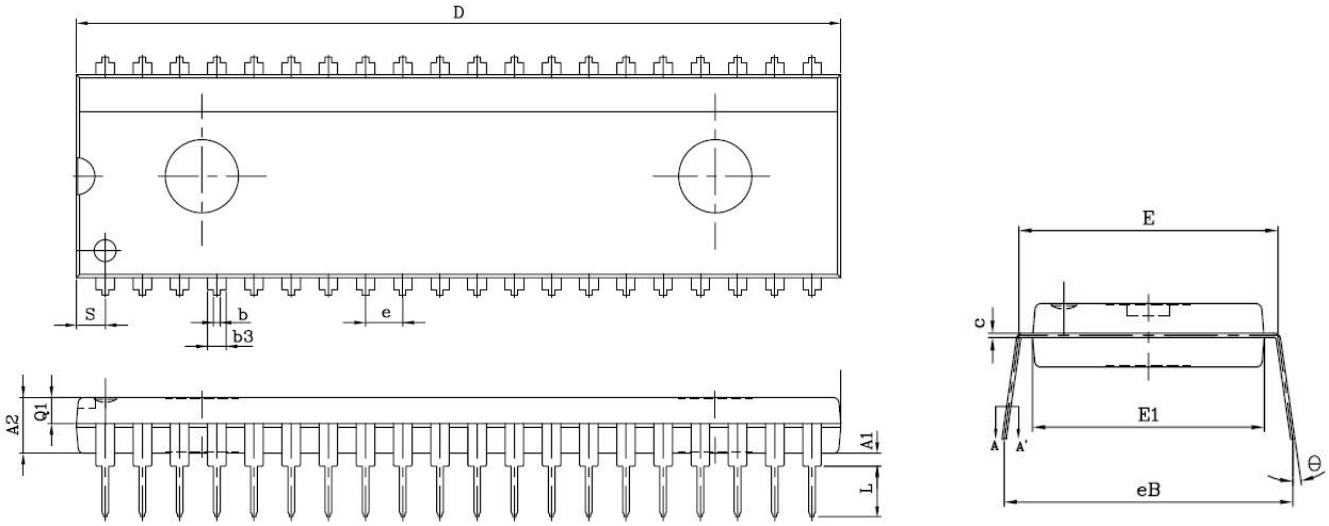
Application Reference

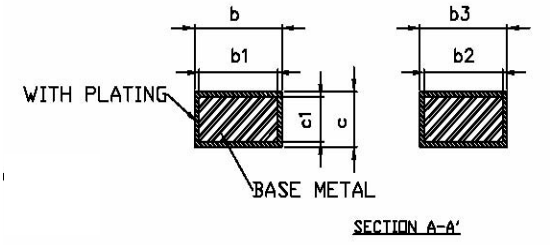
Valid for SM5964A				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	22 pF
C2	30 pF	30 pF	30 pF	22 pF
R	open	open	open	open
X'tal	16MHz	25MHz		
C1	30 pF	15 pF		
C2	30 pF	15 pF		
R	open	open		



Note:
Oscillation circuit may differs with different crystal or ceramic resonator in higher oscillation frequency which was due to each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

PDIP 40L (600mil) Package Information：

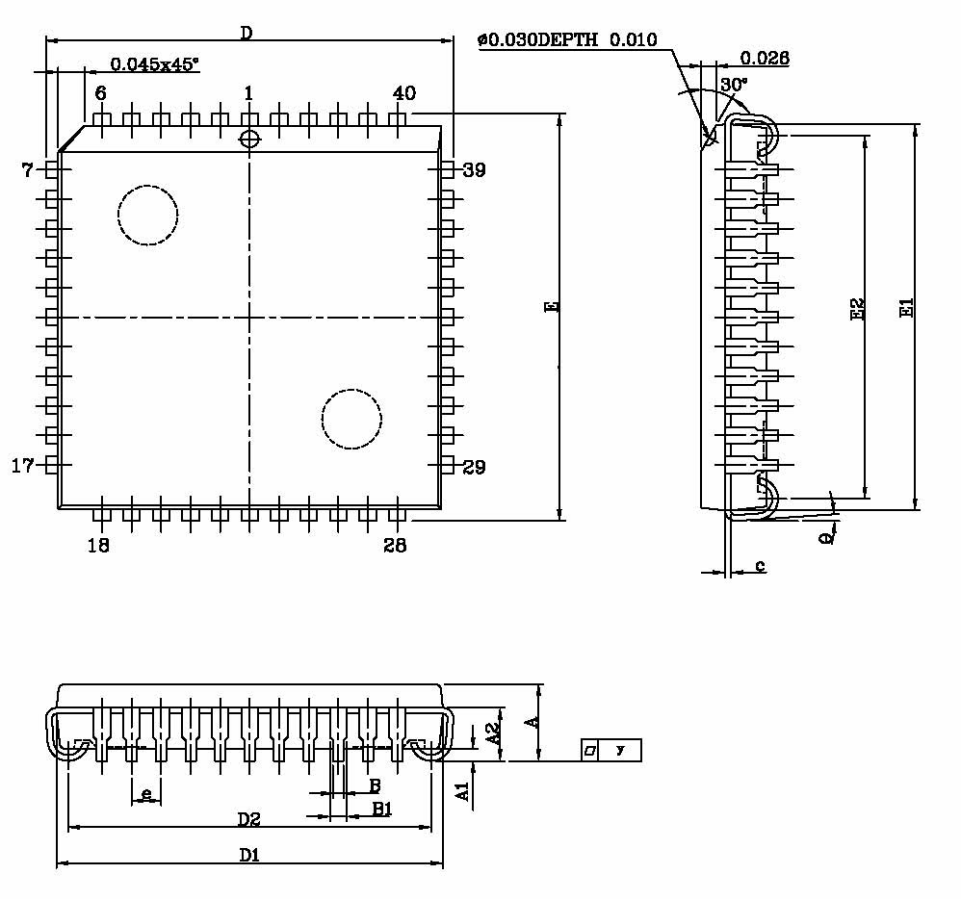


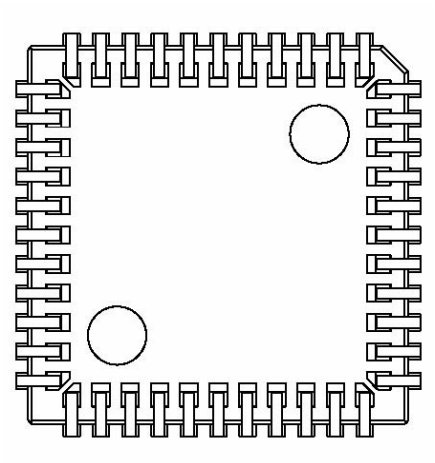


Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A1	0.254	—	—	10	—	—
A2	3.683	3.810	3.937	145	150	155
b	0.356	0.500	0.660	14	20	26
b1	0.356	0.457	0.508	14	18	22
b2	1.016	1.270	1.524	40	50	60
b3	1.016	1.321	1.626	40	52	64
c	0.203	0.254	0.432	8	10	17
c1	0.203	0.254	0.356	8	10	14
D	52.07	52.2	52.32	2050	2055	2060
E	14.99	15.24	15.49	590	600	610
E1	13.69	13.87	13.94	539	546	549
e	—	2.540	—	—	100	—
eB	15.75	16.26	16.76	620	640	660
L	2.921	3.302	3.683	115	130	145
S	1.727	1.981	2.235	68	78	88
Q1	1.651	1.778	1.905	65	70	75
θ	0°	—	10°	0°	—	10°

Note:
1. Refer to JEDEC STD.MS-011(AC).
2. Dimension D and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D and E1 are maximum plastic body size dimension include mold mismatch.
3. Dimension b3 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.2mm.

PLCC 44L Package Information：

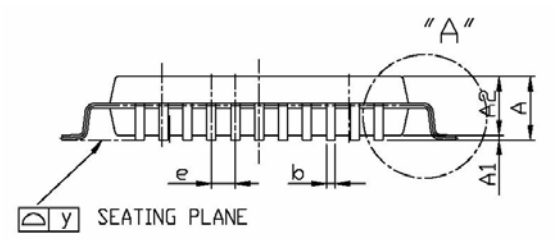


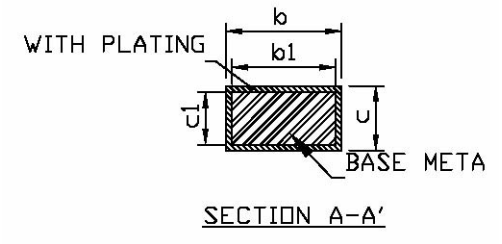


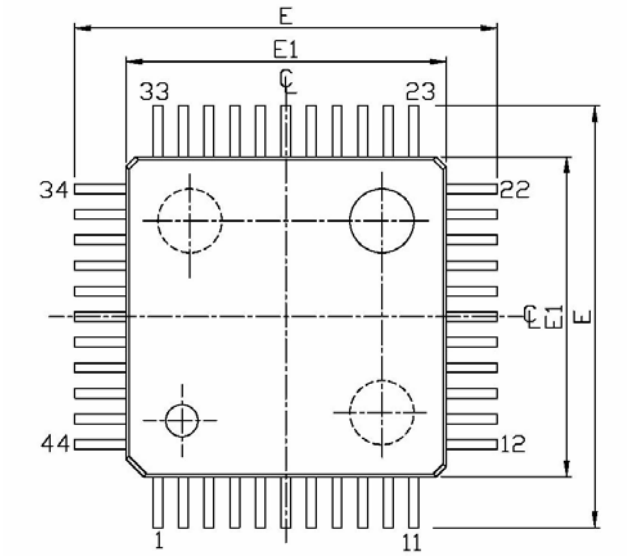
UNIT / SYMBOL	INCH(REF)	MM(BASE)
A	0.180(MAX)	4.572(MAX)
A1	0.024 ±0.005	0.52 ±0.14
A2	0.105 ±0.005	2.667 ±0.127
B	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
B1	0.028 + 0.004 - 0.002	0.711 + 0.102 - 0.051
c	0.010(TYP)	0.254(TYP)
D	0.690 ±0.010	17.526 ±0.254
D1	0.653 ±0.003	16.586 ±0.076
D2	0.610 ±0.020	15.494 ±0.508
E	0.690 ±0.010	17.526 ±0.254
E1	0.653 ±0.003	16.586 ±0.076
E2	0.610 ±0.010	15.494 ±0.254
e	0.050(TYP)	1.270(TYP)
y	0.003(MAX)	0.076(MAX)
θ	0~5°	0~5°

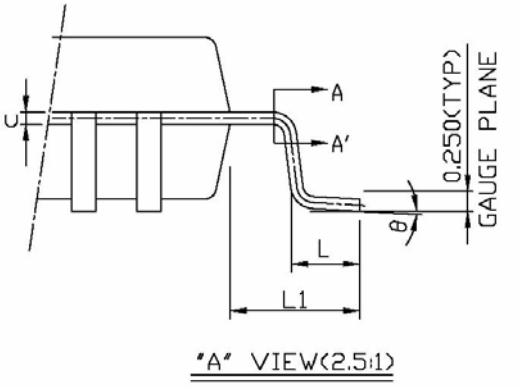
Specifications subject to change without notice contact your sales representatives for the most recent information.

QFP 44L(10x10x2.0mm) Package Information：









Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
A	—	—	2.45	—	—	964
A1	0.05	0.15	0.25	2.1	6.0	9.6
A2	1.90	2.00	2.10	74.8	78.7	82.7
b	0.29	0.32	0.45	11.4	12.6	17.7
b1	0.29	0.30	0.41	11.4	11.8	16.1
c	0.11	0.17	0.23	4.3	6.7	9.1
c1	0.11	0.15	0.19	4.3	5.9	7.5
E	13.00	13.20	13.40	512	520	528
E1	9.90	10.00	10.10	390	394	398
【e】	—	0.800	—	—	31.5	—
L	0.73	0.88	1.03	28.7	34.6	40.6
L1	1.50	1.60	1.70	59.1	63.0	66.9
y	—	—	0.076	—	—	3
θ	0°	—	7°	0°	—	7°

Note:
1. Refer to JEDC STD.MS-022(AB).
2. Dimension E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.E1 are maximum plastic body size dimension include mold mismatch .
3. Dimension b does not include dambar protrusion .Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.1 mm.

Specifications subject to change without notice contact your sales representatives for the most recent information.

e MCU writer list		
Company	Contact info	Programmer Model Number
Advantech 7F, No.98, Ming-Chung Rd., Shin-Tien City, Taipei, Taiwan, ROC Web site: http://www.aec.com.tw	Tel:02-22182325 Fax:02-22182435 E-mail: aecwebmaster@advantech.com.tw	Lab Tool - 48XP (1 * 1) Lab Tool - 848 (1*8)
Hi-Lo 4F, No. 20, 22, LN, 76, Rui Guang Rd., Nei Hu, Taipei, Taiwan, ROC. Web site: http://www.hilosystems.com.tw	Tel:02-87923301 Fax:02-87923285 E-mail: support@hilosystems.com.tw	All - 11 (1*1) Gang - 08 (1*8)
Leap 6th F1-4, Lane 609, Chunghsin Rd., Sec. 5, Sanchung, Taipei Hsien, Taiwan, ROC Web site: http://www.leap.com.tw	Tel:02-29991860 Fax:02-29990015 E-mail: service@leap.com.tw	Leap-48 (1*1) SU - 2000 (1*8)
Xeltek Electronic Co., Ltd 338 Hongwu Road, Nanjing, China 210002 Web site: http://www.xeltek-cn.com	Tel:+86-25-84408399, 84543153-206 E-mail: xelclw@jlonline.com, xelgbw@jlonline.com	Superpro/2000 (1*1) Superpro/280U (1*1) Superpro/L+(1*1)