NIPPON PRECISION CIRCUITS INC.

SM5879AV

3rd-order ΣΔ, 2-channel D/A Converter

OVERVIEW

The SM5879AV is a 3rd-order ∑Δ, two-channel D/A convertor LSI for digital audio reproduction equipment. This device incorporate NPC's molybdenum-gate CMOS technology and incorporates an 8-times oversampling digital filter and analog 3rd-order ∑Δ post-converter low-pass filters.

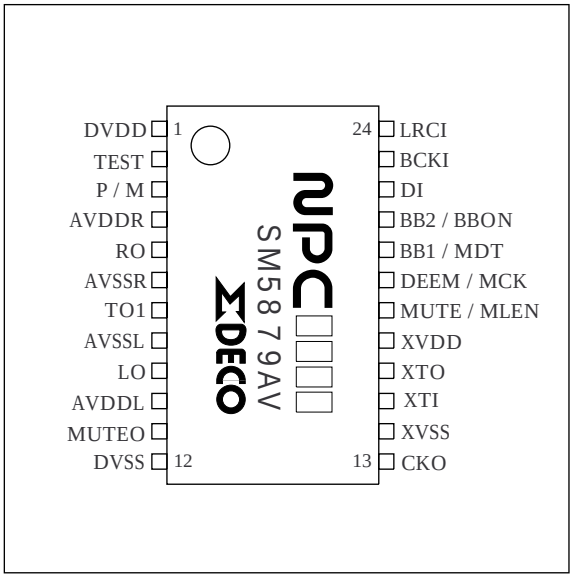
The SM5879AV also incorporates built-in digital bass boost and deemphasis filters, an attenuator, and soft mute function. Low-voltage operation is also supported.

This device features a compact 24-pin VSOP package and a D/A converter that provides both compact size and low power consumption.

FEATURES

- 2.7 to 3.3 V operating supply voltage
- 44.1 kHz sampling frequency
- 16.9344 MHz (384fs) system clock
- Built-in crystal oscillator circuit
- 16-bit, MSB first, rear-packed serial data input format (≤ 64 fs bit clock)
- 8-times oversampling digital filter
  - 32 dB stopband attenuation
  - +0.05 to -0.05 dB passband ripple
- Deemphasis filter operation
  - 36 dB stopband attenuation
  - -0.09 to +0.23 dB deviation from ideal deemphasis filter characteristics
- Attenuator
  - 7-bit attenuator (128 steps) set by microcontroller
- Soft mute function set by parallel setting
  - (approximately 1024/fs total muting time)
- Mono setting
  - Left or right channel mono selectable by microcontroller
- Built-in infinity-zero detection circuit
- ∑Δ, two-channel D/A converter
  - 3rd-order noise shaper
  - 32fs oversampling
- Built-in 3rd-order post-converter low-pass filters
- 24-pin VSOP package
- Molybdenum-gate CMOS process

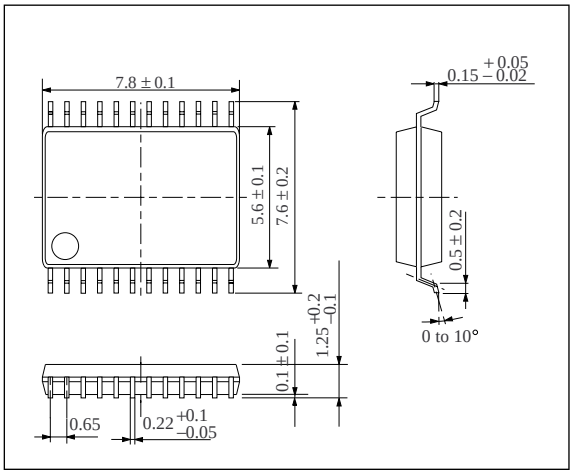
PINOUT (TOP VIEW)



PACKAGE DIMENSIONS

Unit: mm

24-pin VSOP



ORDERING INFOMATION

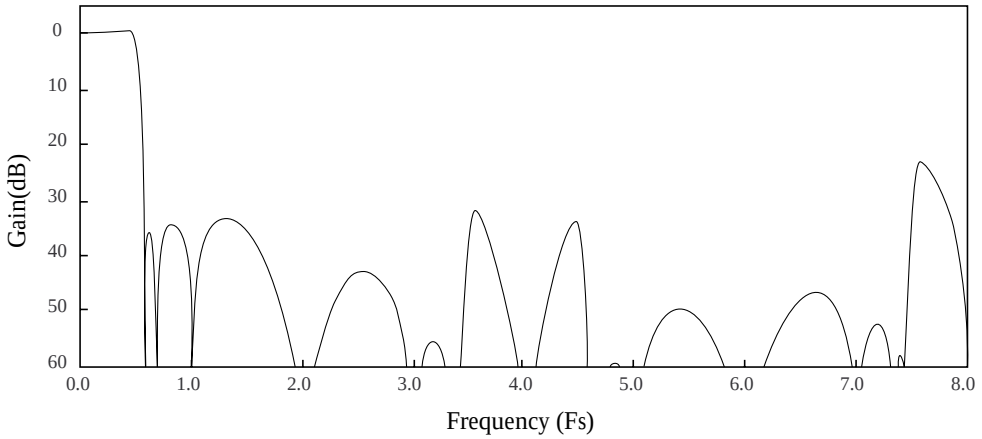
Device	Package
SM5879AV	24pin VSOP

Theoretical Filter Characteristics

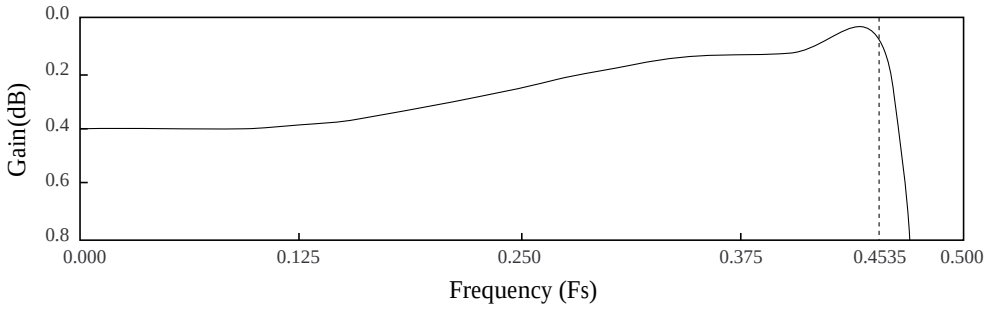
Deemphasis OFF overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Passband ripple	0 to 0.4535fs	0 to 20.0 kHz	–0.05	–	+0.05
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	32	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Overall frequency characteristic (deemphasis OFF)



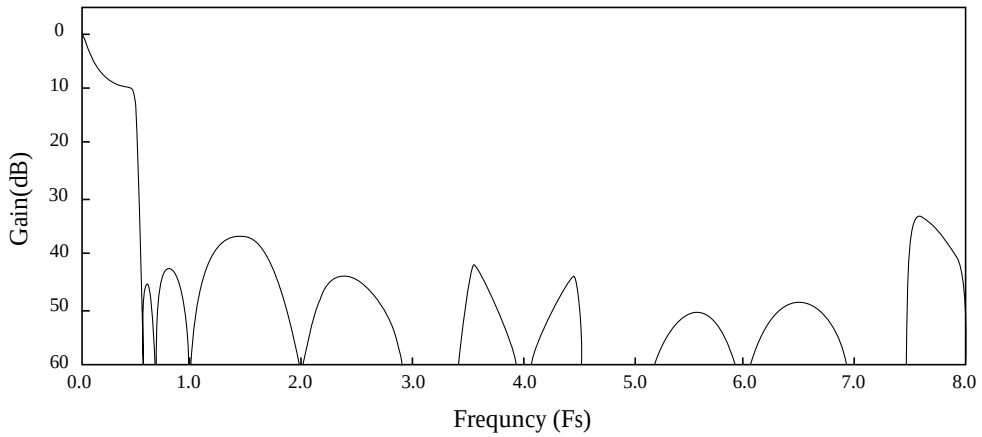
Passband characteristic (deemphasis OFF)



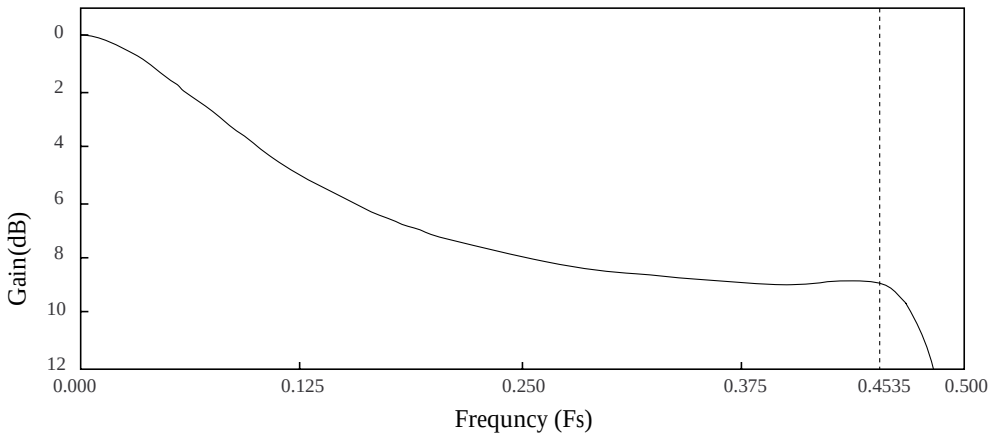
Deemphasis ON overall characteristics

Parameter	Frequency band		Attenuation (dB)		
	f	@ fs = 44.1 kHz	min	typ	max
Deviation from ideal deemphasis filter characteristics	0 to 0.4535fs	0 to 20.0 kHz	–0.09	–	+0.23
Stopband attenuation	0.5465fs to 7.4535fs	24.1 to 328.7 kHz	36	–	–
Built-in analog LPF compensation	0.4535fs	20.0 kHz	–	–0.34	–

Overall frequency characteristic (deemphasis ON)



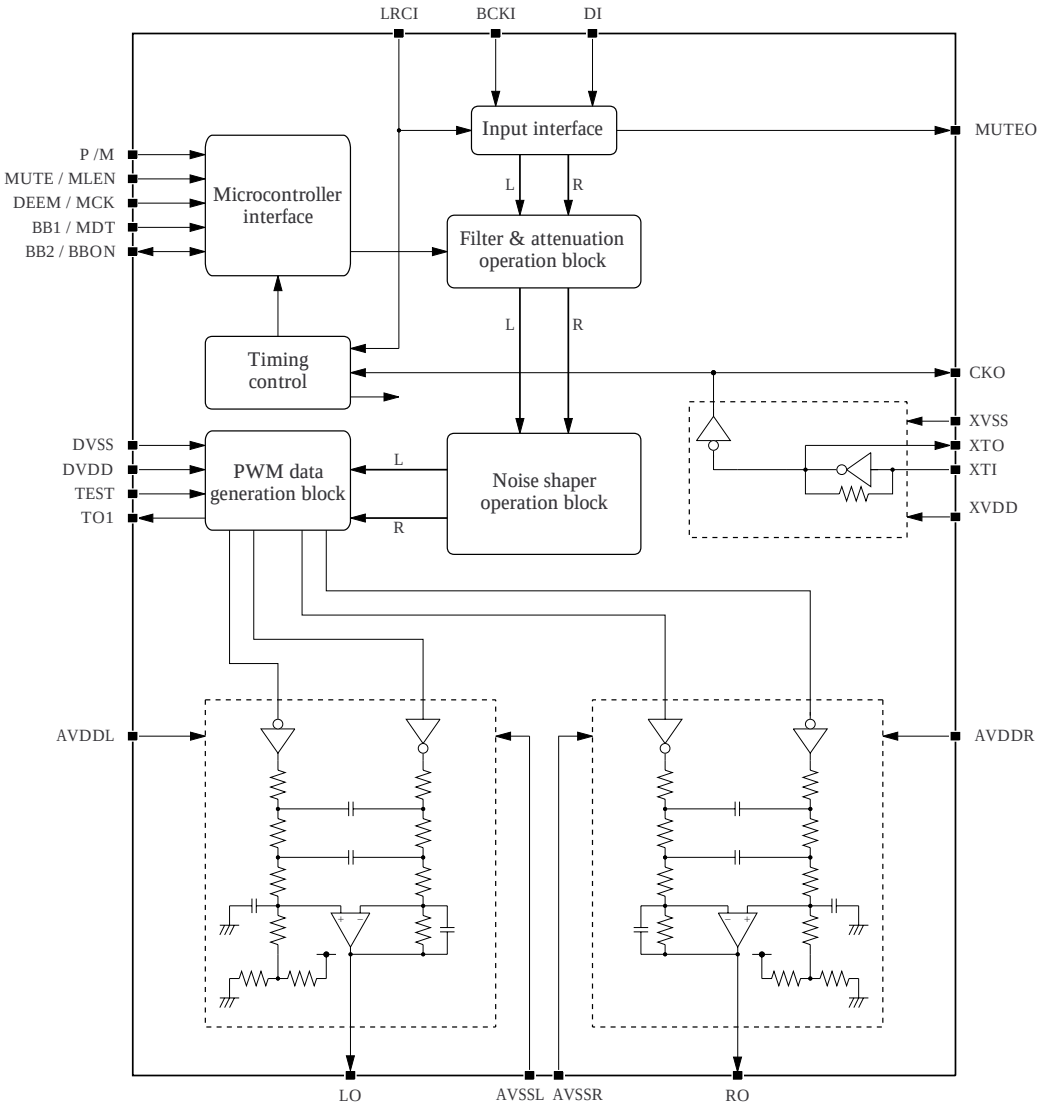
Passband characteristic (deemphasis ON)



PIN DESCRIPTION

Number	Name	I/O	Description
1	DVDD	I-	Digital supply pin.
2	TEST	I	Input for testing LSI. Test mode when HIGH.
3	P/M	I	Parallel/microcontroller setting selection pin. Parallel setting when HIGH.
4	AVDDR	-	Right-channel analog supply pin.
5	RO	O	Right channel analog output pin.
6	AVSSR	-	Right-channel analog ground pin.
7	TO1	O	Test mode output. Normally LOW.
8	AVSSL	-	Left-channel analog ground pin.
9	LO	O	Left-channel analog output pin.
10	AVDDL	O	Left-channel analog supply pin.
11	MUTEO	O	Infinity-zero detection output
12	DVSS	-	Digital ground pin
13	CKO	O	Oscillator clock output. 16.9344 MHz.
14	XVSS	-	Crystal oscillator ground pin
15	XTI	I	Crystal oscillator or 16.9344-MHz external clock input pin
16	XTO	O	Crystal oscillator output pin
17	XVDD	-	Crystal oscillator supply pin
18	MUTE/ MLEN	I	P/M=H; soft mute control pin. Mute is active when HIGH. P/M=L; microcontroller interface clock
19	DEEM/ MCK	I	P/M=H; deemphasis control pin. Deemphasis is ON when HIGH. P/M=L; microcontroller interface clock
20	BB1/ MDT	I	P/M=H; bass boost setting switch pin 1 P/M=L; microcontroller interface serial data
21	BB2/ BBON	IO	P/M=H; bass boost setting switch pin 2 P/M=L; bass boost detection output
22	DI	I	Serial data input pin
23	BCKI	I	Bit clock input pin
24	LRCI	I	Sample rate clock (fs) input pin. Left channel when HIGH, and right channel when LOW.

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

$DV_{SS} = AV_{SSL} = AV_{SSR} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	–0.3 to 7.0	V
Input voltage range[1]	V_{IN1}	DV_{SS} – 0.3 to DV_{DD} + 0.3	V
XTI input voltage range	V_{IN}	XV_{SS} – 0.3 to XV_{DD} + 0.3	V
Storage temperature range	T_{stg}	–55 to 125	°C
Power dissipation	P_D	250	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

1. Pins TEST, P/ M, MUTE/ MLEN, DEEM/ MCK, BB1/ MDT, BB2/ BBON, DI, BCKI, LRCI
Also applicable during supply switching.

Recommended Operating Conditions

$DV_{SS} = AV_{SSL} = AV_{SSR} = XV_{SS} = 0$ V, $AV_{DD} = AV_{DDL} = AV_{DDR}$

Parameter	Symbol	Rating	Unit
Supply voltage range	DV_{DD}, AV_{DD}, XV_{DD}	2.7 to 3.3	V
Supply voltage variation	$DV_{DD} – XV_{DD}$, $DV_{DD} – AV_{DD}$, $XV_{DD} – AV_{DD}$, $DV_{SS} – XV_{SS}$, $DV_{SS} – AV_{SS}$, $XV_{SS} – AV_{SS}$	±0.1	V
Operating temperature range	T_{opr}	–20 to 70	°C

note) Since DVDD, XVDD, AVDDL, and AVDDR are connected via the LSI base board, current may flow if potential difference occurs among them.

DC Electrical Characteristics

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DVDD digital supply current[1]	I_{DDD}		–	3.70	7.40	mA
XVDD system clock supply current[1]	I_{DDX}		–	0.55	1.10	mA
AVDD analog supply current[1]	I_{DDA}[2]		–	0.68	1.36	mA
XTI HIGH-level input voltage	V_{IH1}	Clock input	$0.7XV_{DD}$	–	–	V
XTI LOW-level input voltage	V_{IL1}	Clock input	–	–	$0.3XV_{DD}$	V
XTI AC-coupled input voltage	V_{INAC}		$0.3XV_{DD}$	–	–	V_{p-p}
HIGH-level input voltage[3]	V_{IH2}		$0.7DV_{DD}$	–	–	V
LOW-level input voltage[3]	V_{IL2}		–	–	$0.3DV_{DD}$	V
HIGH-level output voltage[4]	V_{OH}	I_{OH} = –0.5mA	DV_{DD} – 0.4	–	–	V
LOW-level output voltage[4]	V_{OL}	I_{OL} = 0.5mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH1}	$V_{IN} = XV_{DD}$	–	4	10	µA
XTI LOW-level input current	I_{IL1}	V_{IN} = 0 V	–	4	10	µA
Input leakage current[3]	I_{ILH}	$V_{IN} = DV_{DD}$	-1.0	–	1.0	µA
	I_{LL}	V_{IN} = 0V	-1.0	–	1.0	µA

1. $DV_{DD} = AV_{DD} = XV_{DD}$ = 2.7V, XTI clock input frequency f_{XTI} = 16.9344 MHz, no output load.
2. I_{DDA} is the total current.
3. Pins TEST, P/ M, MUTE/ MLEN, DEEM/ MCK, BB1/ MDT, BB2/ BBON, DI, BCKI, LRCI
4. Pins MUTEO, CKO, BB2/ BBON, TO1

AC Electrical Characteristics

System clock (XTI)

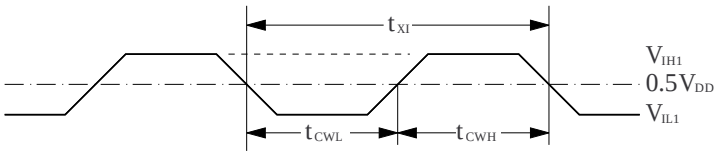
Crystal Oscillator

Parameter	Symbol	Rating			Unit
		min	typ	max	
Oscillator frequency	f_{OSC}	10.0	16.9344	18.5	MHz

External clock input

Parameter	Symbol	Rating			Unit
		min	typ	max	
HIGH-level clock pulsewidth	t_{CWH}	20.0	29.5	50	ns
LOW-level clock pulsewidth	t_{CWL}	20.0	29.5	50	ns
Clock pulse cycle	t_{XI}	54.0	59.0	100	ns

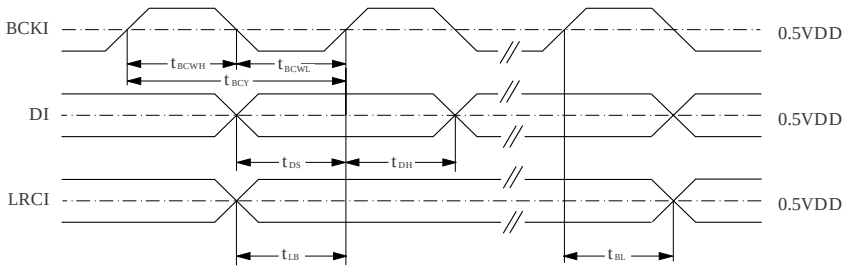
XTI input clock



Serial input (BCKI, DI, LRCI)

Parameter	Symbol	Rating			Unit
		min	typ	max	
BCKI HIGH-level pulsewidth	t_{BCWH}	50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}	50	–	–	ns
BCKI pulse cycle	t_{BCY}	$6t_{XI}$	–	–	ns
DI setup time	t_{DS}	50	–	–	ns
DI hold time	t_{DH}	50	–	–	ns
Last BCKI rising edge to LRCI edge	t_{BL}	50	–	–	ns
LRCI edge to first BCKI rising edge	t_{LB}	50	–	–	ns

Serial input timing



Control input

P/M=H

Parameter	Symbol	Rating			Unit
		min	typ	max	
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	50	ns

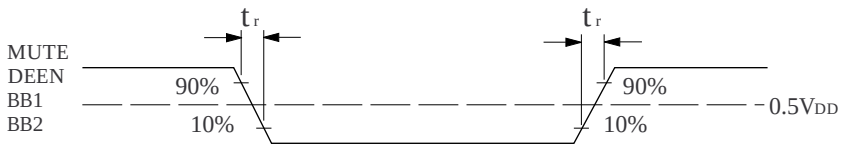
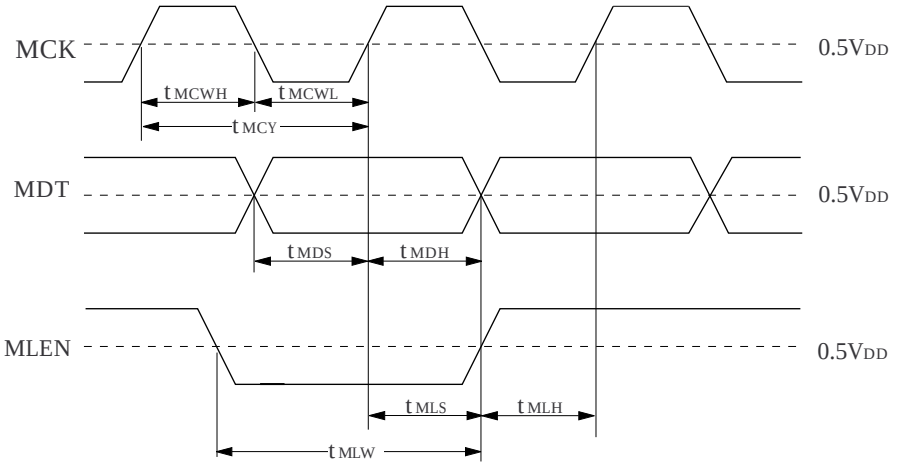


Figure 1.

P/M=L

Parameter	Symbol	Rating			Unit
		min	typ	max	
MCK LOW-level pulsewidth	t_{MCWL}	200	–	–	ns
MCK HIGH-level pulsewidth	t_{MCWH}	200	–	–	ns
MCK pulse width	t_{Mcy}	400	–	–	ns
MDT setup time	t_{MDS}	100	–	–	ns
MDT hold time	t_{MDH}	100	–	–	ns
MLEN setup time	t_{MLH}	100	–	–	ns
MLEN hold time	t_{MLW}	200	–	–	ns
Rise time	t_r	–	–	50	ns
Fall time	t_f	–	–	50	ns



AC Analog Characteristics

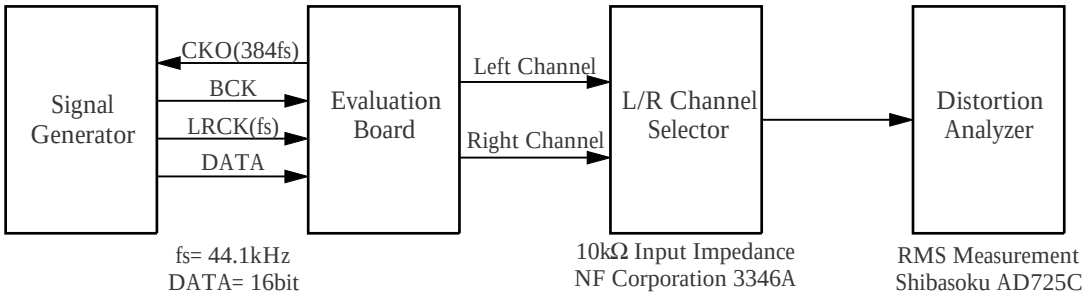
DV_{SS} = AV_{SSL}= AV_{SSR} = XV_{SS} = 0 V, DV_{DD} = AV_{DDL} = AV_{DDR} = XV_{DD} = 2.7V, P/M=2.7V, MUTE=0V, DEEM=0V, BB1=2.7V, BB2=2.7V, crystal oscillator frequency f_{OSC} = 16.9344 MHz, T_a = 25 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Total harmonic distortion	THD + N	1 kHz, 0 dB	–	0.0075	0.015	%
LSI output level	V_{out1}	1 kHz, 0 dB	0.65	0.70	0.75	V_{rms}
Evaluation board output level	V_{out2}	1 kHz, 0 dB	–	0.70	–	V_{rms}
Dynamic range	D.R	1 kHz, –60 dB	86.0	91.0	–	dB
Signal-to-noise ratio[1]	S/N	1 kHz, 0/–∞ dB	86.0	91.5	–	dB
Channel separation	Ch. Sep	1 kHz, –∞/0 dB	80.0	87.0	–	dB

1. Signal-to-noise is measured following a device reset, with DATA = 0 (DI = LOW). Under these conditions, the signal-to-noise ratio includes noise-shaper noise.

AC Measurement Circuit and Conditions

Measurement circuit block diagram

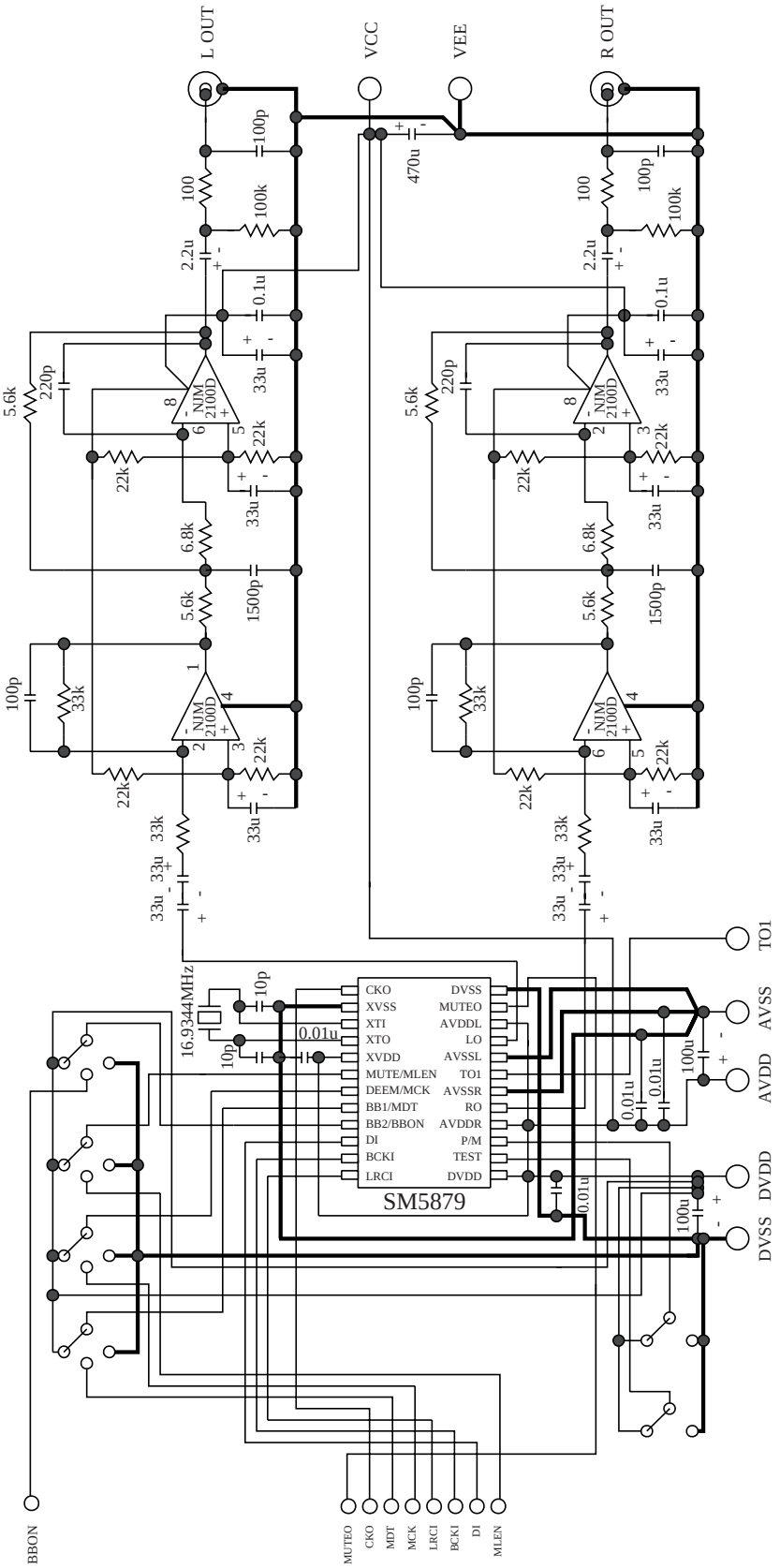


Measurement conditions

Parameter[1]	Symbol	3346A left/right-channel selector switch	AD725C distortion analyzer with built-in filter
Total harmonic distortion	THD + N	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF
Output level	V_{out}		
Dynamic range	DR	D-RANGE	
Signal-to-noise ratio	S/N	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF JIS A filter ON
Channel separation	Ch. Sep	THRU	20 kHz lowpass filter ON 400 Hz highpass filter OFF

1. Pins LO and RO should have an output load of 10 kΩ (min).

Measurement circuit



FUNCTIONAL DESCRIPTION

System Clock

Note that the input clock accuracy and jitter greatly influence the AC analog characteristics.

The system clock can be controlled by a crystal oscillator consisting of a crystal connected between XTI and XTO and a built-in CMOS invertor or, alternatively, an external system clock. Since the built-in CMOS invertor has a feedback resistor, the external system clock can be AC coupled to XTI. The system clock is output from CKO.

System Reset (RSTN)

System reset for SM5879AV is performed by a built-in power ON reset circuit.

At system reset, the internal arithmetic operation and output timing counter are synchronized with the next LCRI rising edge and thereby reset again for synchronization with external elements.

Analog output is muted by this resetting, and muting is cleared by the ninth LCRI rise (See Figure 1).

However, noise is generated due to the change in PWM output during a timing reset. An external mute circuit is necessary to prevent this noise.

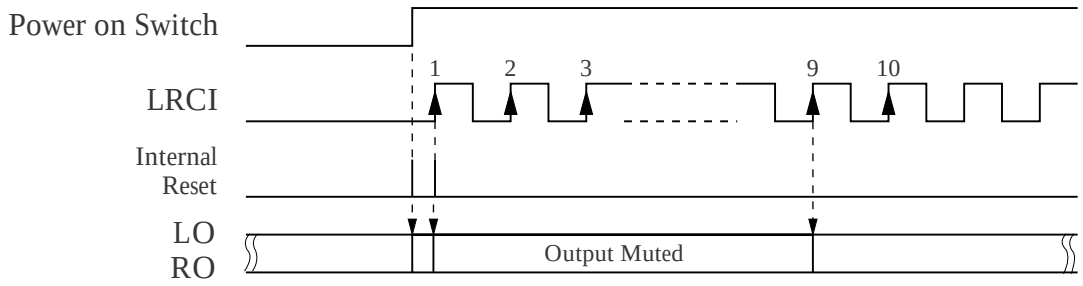


Figure 2. System reset timing

Audio Data Input (DI, BCKI, LRCI)

The digital audio data is input on DI in MSB-first, 2s-complement, 16-bit serial format.

Serial data bits are read into the SIPO register (serial-to-parallel converter register) on the rising edge of the bit clock BCKI.

The bit clock frequency on BCKI should be between 32fs and 64fs.

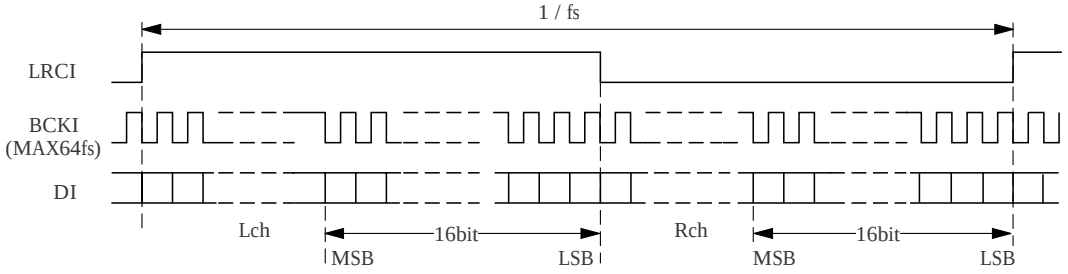


Figure 3.

Selection and Setting of Functions

SM5879AV offers a variety of functions. Fundamentally, there are two methods available for selecting and setting these functions.

One method is using an external input pin; this is called parallel setting. The other method is by using the microcontroller interface, which is called microcontroller setting.

Microcontroller interface refers here to serial data transfer from the microcontroller using the three pins MDT, MCK, and MLEN.

These two methods of setting and selection are set by the P/M pin.

When P/M is HIGH, parallel setting is used.

When P/M is LOW, microcontroller setting is used.

Table 1. Selection and Setting of Functions

Function	**Function Setting Methods**		**Notes**
	Parallel setting Related external pin name (When P/M is HIGH)	**Microcontroller setting** Related flag (When P/M is LOW)	
Bass boost	BB1, BB2	FBB1, FBB2	Bass boost
Bass boost detection output	None	Output to BBON	Bass boost detection output
Deemphasis filter	DEEM	FDEM	Deemphasis filter
Soft mute	MUTE	None (Enabled by attenuator)	Soft mute
Attenuator setting	None	7 bits (A6 - A0)	Attenuation
Monaural setting	None	MONO, CSEL	Stereo/mono output setting

Microcontroller Interface

For microcontroller setting (when P/M is HIGH), the microcontroller interface consisting of MDT (data), MCK (clock) and MLEN (latch enable) can be used.

Data from the microcontroller is input to the input-stage shift registers at the rise of MCK. Changes in MDT should be performed at the rise of MCK.

Serial data in the shift registers is latched in parallel to the flag registers at the rise of MLEN.

Two flag registers are available, divided into the attenuation factor and mode flag by the D7 data.

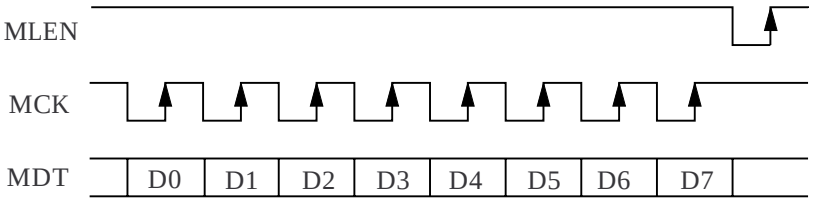


Figure 4. Format of microcontroller interface input

Table 2. microcontroller setting flags

Microcontroller serial data	Flag	
D7	0	1
D6	A6	-
D5	A5	FDEM
D4	A4	FBB1
D3	A3	FBB2
D2	A2	MONO
D1	A1	CSEL
D0	A0	-

A0 to A6: Attenuation factor (A6: MSB)
FDEM: Deemphasis ON/OFF (ON when 1)
FBB1: Bass boost setting switch flag 1
FBB2: Bass boost setting switch flag 2
MONO: Stereo/mono setting (Mono when 1)
CSEL: Mono output channel selection
(Right channel when 1)

Bass Boost

Two types of bass boost and gain modification can be set by either parallel or microcontroller.

Table 3.

Parallel setting pin name	BB1	BB2	Mode
Microcontroller setting flag	FBB1	FBB2	
	H	H	Flat 1
	H	L	Bass boost MIN
	L	H	Bass boost MAX
	L	L	Flat2

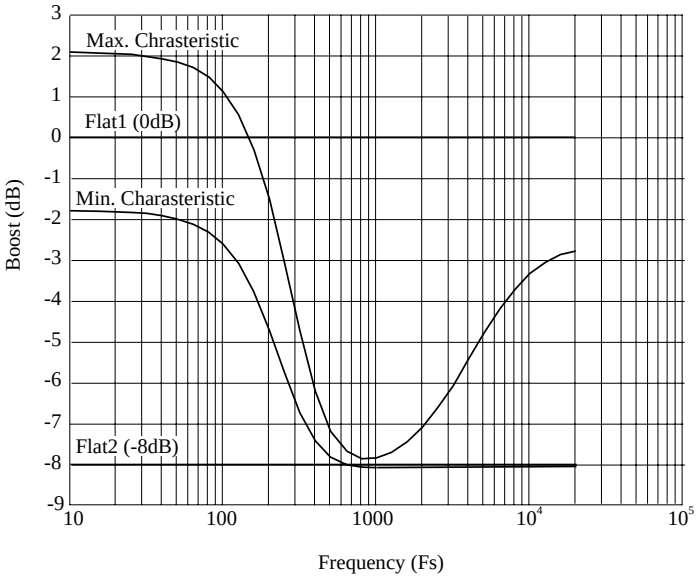


Figure 5. Bass boost mode frequency response

Bass boost detection output

With microcontroller setting (when P/M is LOW), the 21st pin is the BBON output pin and functions as output that detects the bass boost mode.

BBON output is LOW when the bass boost mode is set to Flat 1 and HIGH in all other cases.

Table 4.

Microcontroller setting flag	BB1	BB2	Mode	BBON pin
	H	H	Flat 1	L
	H	L	Bass boost MIN	H
	L	H	Bass boost MAX	H
	L	L	Flat 2	H

Deemphasis filter

The built-in deemphasis filter in the SM5879AV operates at fs = 44.1 kHz.

Table 5.

Parallel setting pin name	DEEM	Deemphasis mode
Microcontroller setting flag	FDEM	
	H	ON
	L	OFF

Soft Mute

With parallel setting (when P/M is HIGH), soft mute can be activated by the MUTE pin level setting using the built-in attenuation counter. When muting is activated, MUTE is HIGH.

When soft mute is activated, the attenuation counter operates and lowers gain in 128 steps.

The time until mute is activated is approximately 1024/fs ≈ 23.2 msec. The time required to release muting is the same.

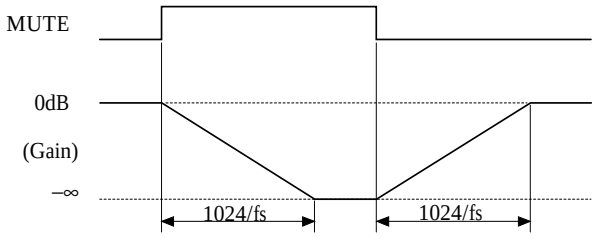


Figure 6. Example of soft mute operation

Attenuation

The SM5879AV loads the attenuation factor with serial data by means of the microcontroller interface, thus enabling attenuation operation.

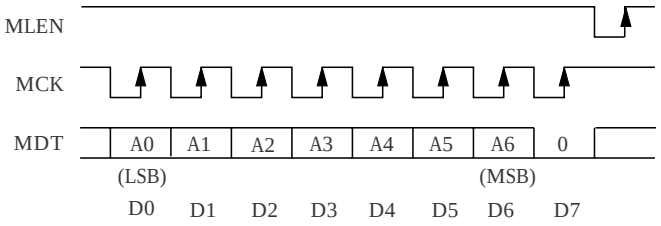


Figure 7. Method of setting the attenuation factor

The attenuation computation is performed by multiplying the output of the internal 7-bit UP/DOWN counter output data by the signal data. When the contents of the counter are DATT, gain can be expressed by the following equations.

L channel

$$Gain = 20 \times \log\left(\frac{DATT}{127}\right)[dB]$$

R channel

$$Gain = 20 \times \log\left(\frac{DATT}{127}\right)[dB]$$

When DATT = 0, this becomes -∞.

When the attenuation factor is changed, it is smoothly changed from the previous setting until it reaches the value of the new setting as expressed by the above equations. The time required to change gain is approximately 1024 fs ≈ 23.2 msec when the time required to change one step of the attenuation factor is approximately 8 / fs ≈ 181.4 µsec over the range 0 dB to -∞.

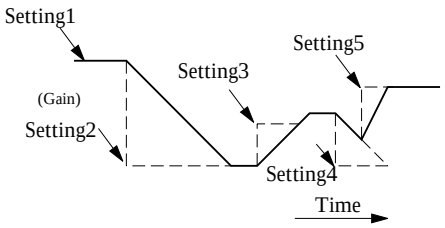


Figure 8. Example of attenuation gain

Stereo/Mono Output Setting

Mono output can be set via the microcontroller (when P/M is HIGH).

Table 6.

Microcontroller setting flag	MONO	CSEL	Output
	H	H	R channel
	H	L	L channel
	L	H	Stereo
	L	L	

Infinity-Zero Detection Output

HIGH level is output from the infinity-zero detection output pin in the following cases with the SM5879AV.

(1) From the time that power ON is reset until the first data comes in.

(2) When the LOW level space of the DI pin has continued for $2^{14} \times (1/fs) \approx 0.37$ [sec] or more.

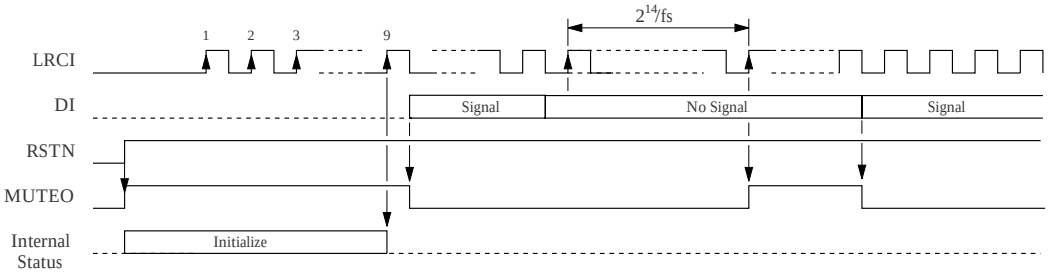
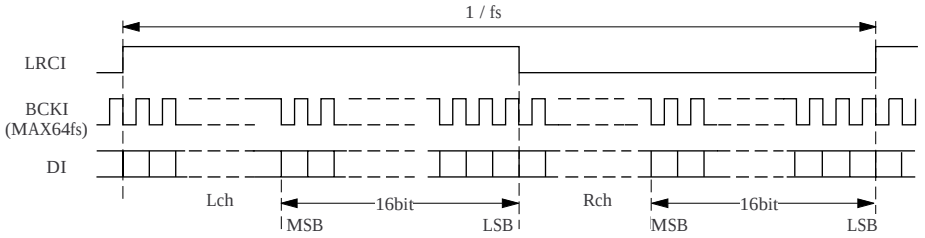


Figure 9.

TIMING DIAGRAMS

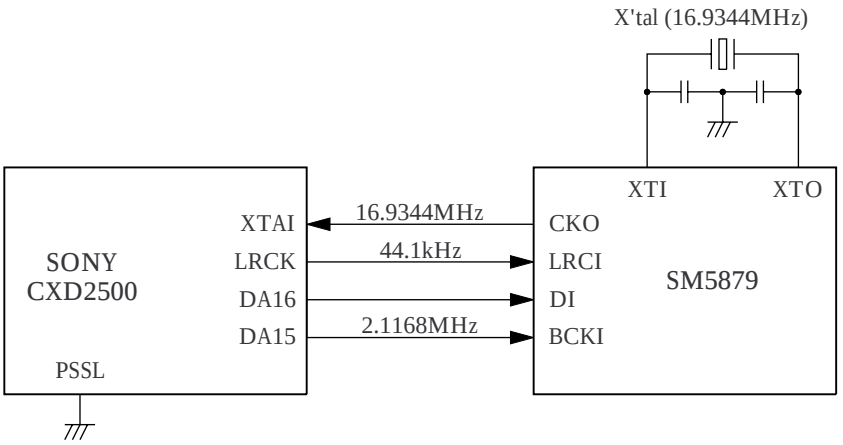
Input Timing (DI, BCKI, LRCI)



TYPICAL APPLICATIONS

Input Interface Circuits

Normal Speed



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