NIPPON PRECISION CIRCUITS INC.

SM5847AF

High-fidelity Digital Audio, Multi-function Digital Filter

OVERVIEW

The SM5847AF is a 4/8-times oversampling (interpolation), 2-channel, linear-phase FIR, multi-function digital filter for digital audio reproduction equipment. It features independent left and right-channel digital deemphasis filters and soft muting function.

The input/output interface supports input data in 16/18/20/24-bit words, and output data in 18/20/22/24-bit words in either 4-times or 8-times oversampling selectable output mode.

The internal system clock operates at either 192fs or 256fs selectable speed (where fs is the audio sampling frequency). Plus, the divide-by 1, 2, or 4 counter settings means that external clocks of 768fs/384fs/192fs (192fs input) and 1024fs/512fs/256fs (256fs input) are supported.

The SM5847AF operates from a single 3 to 5 V supply, and is available in 44-pin QFP packages.

FEATURES

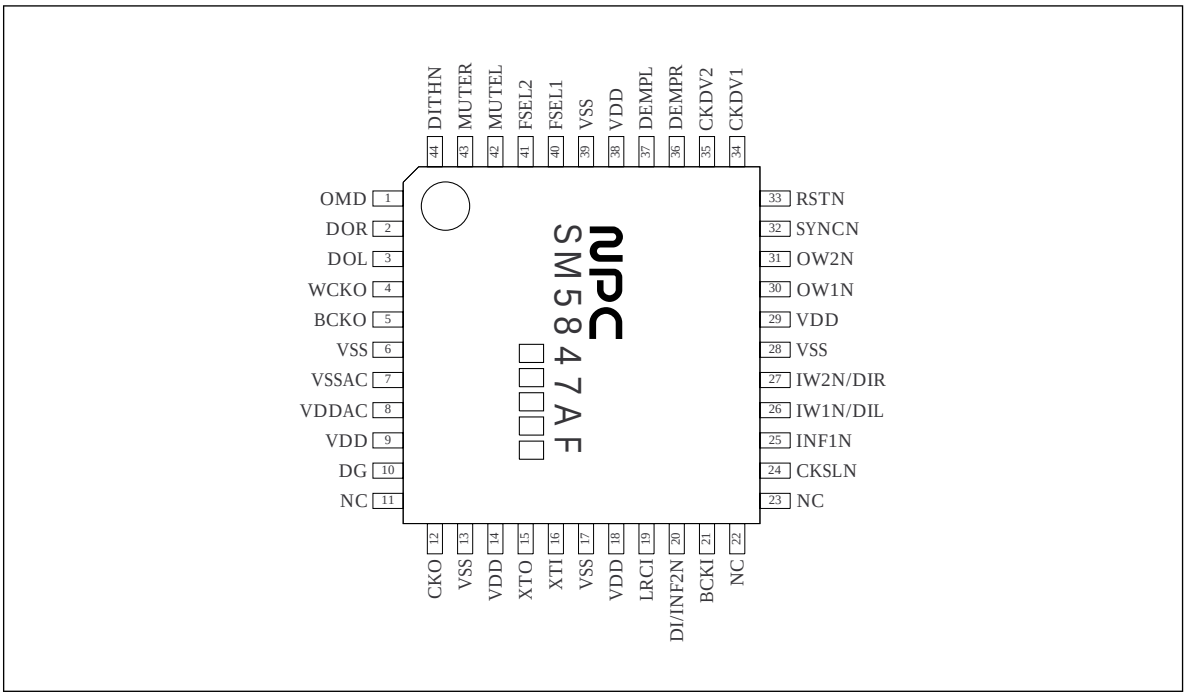
- Left/right-channel (2-channel processing)
- 4-times/8-times oversampling (interpolation)
  - 8-times interpolation filter
    - 3-stage linear-phase FIR configuration
      1st stage (fs to 2fs): 169-tap
      2nd stage (2fs to 4fs): 29-tap
      3rd stage (4fs to 8fs): 17-tap
    - ≤ ±0.00002 dB passband ripple (0 to 0.4535fs)
    - ≥ 117 dB stopband attenuation (0.5465fs to 7.4535fs)
  - 4-times interpolation filter
    - 2-stage linear-phase FIR configuration
      1st stage (fs to 2fs): 169-tap
      2nd stage (2fs to 4fs): 29-tap
    - ≤ ±0.00002 dB passband ripple (0 to 0.4535fs)
    - ≥ 116 dB stopband attenuation (0.5465fs to 3.4535fs)
- Digital deemphasis
  - IIR filter configuration
  - fs = 32kHz, 44.1kHz, 48kHz
  - 2-channel independent ON/OFF control
- 26 × 24-bit parallel multiplier/32-bit accumulator
- Overflow limiter
- Soft muting
  - 2-channel independent ON/OFF control
- Input data format
  - 2s complement, MSB first
  - 3 selectable formats
    - LR alternating, 16/18/20/24-bit serial, right-justified data
    - LR alternating, 24-bit serial, left-justified data
    - LR simultaneous, 24-bit serial, left-justified data
- Output data format
  - 2s complement, MSB first, LR simultaneous
  - 18/20/22/24-bit serial
  - BCKO burst (NPC format)
- Dither round-off processing
  - Dither round-off ON/OFF selectable
- 25-bit internal data word length
- Internal system clock
  - 192fs/256fs selectable
  - Maximum operating frequency
    192fs mode: 37 MHz max (5 V)
    20.7 MHz max (3 V)
    256fs mode: 27.6 MHz max (5 V)
    25 MHz max (3 V)
- Jitter-free function
  - Jitter-free/Sync mode selectable
- Crystal oscillator circuit built-in
- 3 to 5 V supply
- 44-pin plastic QFP
- CMOS process

ORDERING INFORMATION

Device	Package
SM5847AF	44-pin QFP

PINOUT

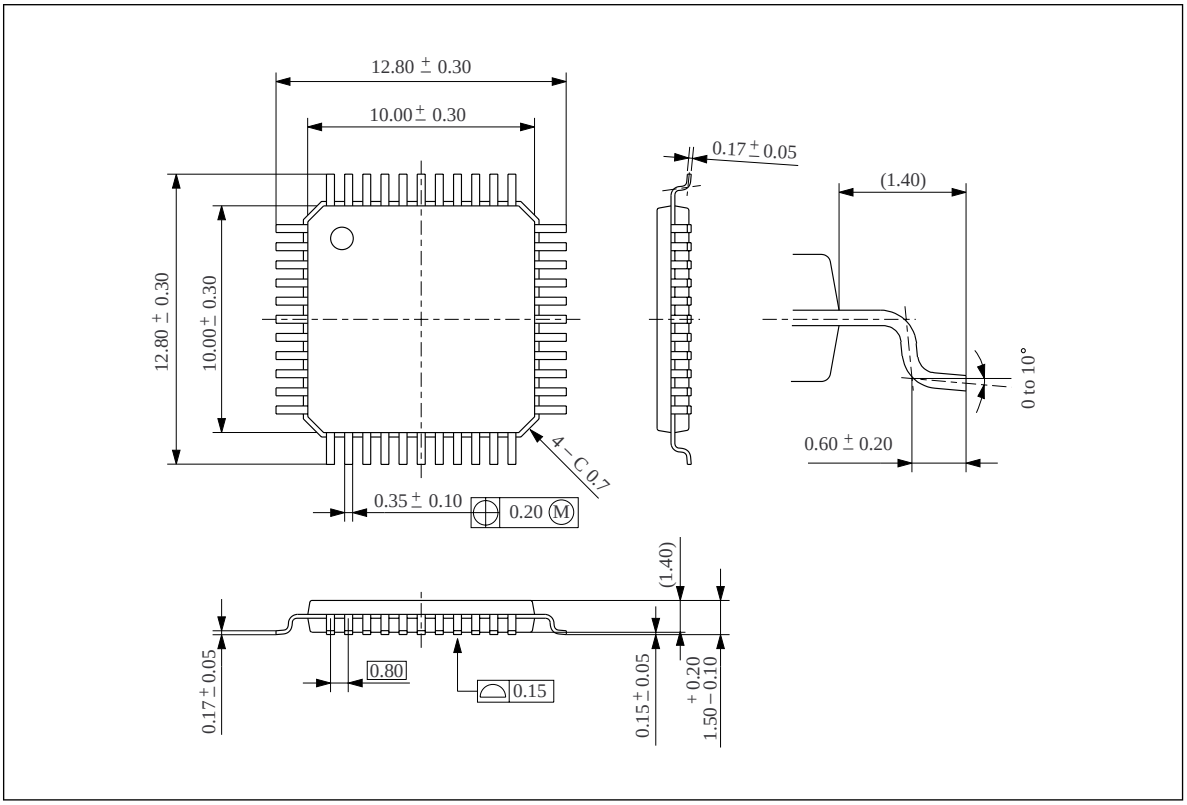
(Top View)



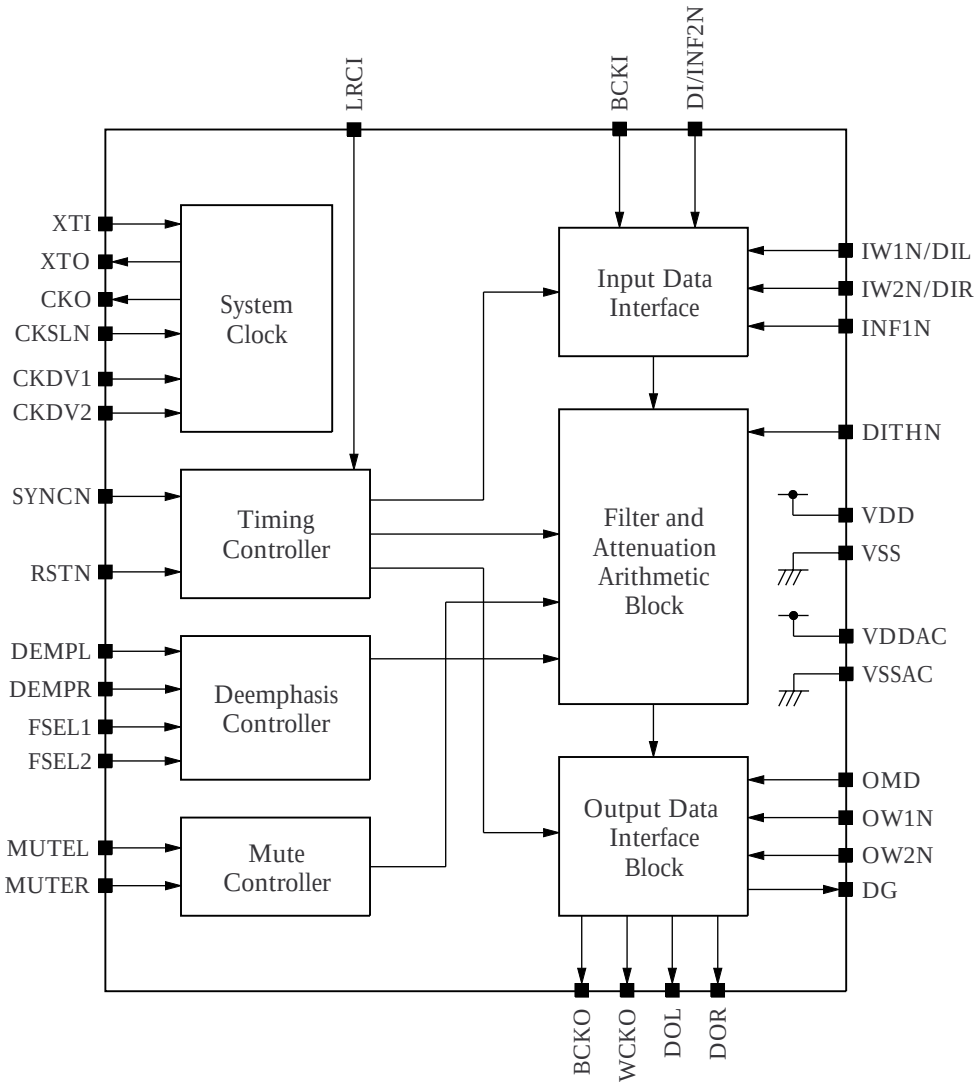
PACKAGE DIMENSIONS

(Unit: mm)

44-pin plastic QFP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	OMD	Ip[1]	Output data rate (4fs/8fs) select pin
2	DOR	O[2]	Right-channel data output
3	DOL	O[2]	Left-channel data output
4	WCKO	O[2]	Word clock output
5	BCKO	O[2]	Bit clock output
6	VSS	–	Ground
7	VSSAC	–	Ground
8	VDDAC	–	Supply voltage
9	VDD	–	Supply voltage
10	DG	O[2]	Deglitched signal output
11	NC	–	No internal connection (must be open)
12	CKO	O[2]	Master clock output
13	VSS	–	Ground
14	VDD	–	Supply voltage
15	XTO	O	Oscillator output
16	XTI	I	Oscillator input/master clock input
17	VSS	–	Ground
18	VDD	–	Supply voltage
19	LRCI	I[1]	Input data sample rate (fs) clock input
20	DI/INF2N	I[1]	Data input/input format select pin 2
21	BCKI	I[1]	Bit clock input
22	NC	–	No internal connection (must be open)
23	NC	–	No internal connection (must be open)
24	CKSLN	Ip[2]	Master clock frequency (192fs/256fs) select pin
25	INF1N	Ip[2]	Input format select pin 1
26	IW1N/DIL	Ip[1]	Input data word length select pin 1/left-channel data input
27	IW2N/DIR	Ip[1]	Input data word length select pin 2/right-channel data input
28	VSS	–	Ground
29	VDD	–	Supply voltage
30	OW1N	Ip[2]	Output data word length select pin 1
31	OW2N	Ip[2]	Output data word length select pin 2
32	SYNCN	Ip[2]	Sync mode select pin
33	RSTN	Ip[1]	Reset input
34	CKDV1	Ip[1]	Internal system clock frequency divider set pin 1
35	CKDV2	Ip[1]	Internal system clock frequency divider set pin 2
36	DEMPR	Ip[1]	Right-channel deemphasis ON/OFF pin
37	DEMPL	Ip[1]	Left-channel deemphasis ON/OFF pin
38	VDD	–	Supply voltage
39	VSS	–	Ground
40	FSEL1	Ip[1]	Deemphasis filter sample rate (fs) select pin 1
41	FSEL2	Ip[1]	Deemphasis filter sample rate (fs) select pin 2
42	MUTEL	Ip[1]	Left-channel mute ON/OFF pin
43	MUTER	Ip[1]	Right-channel mute ON/OFF pin
44	DITHN	Ip[1]	Output data dither ON/OFF pin

1. Schmitt input, TTL level
2. TTL level

Ip = Pull-up input

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = V_{SSAC} = 0$ V, $V_{DD} = V_{DDAC}$

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range[1]	V_{DD}, V_{DDAC}		–0.3 to 6.5	V
Input voltage range	V_I		V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}		–55 to 125	°C
Power dissipation	P_D	≤ 70 °C	900	mW
		≤ 85 °C	700	

1. Supply lines for VDD and VDDAC, and ground lines for VSS and VSSAC, should be connected on the printed circuit board to prevent device breakdown due to potential difference when the power is applied.

Recommended Operating Conditions

$V_{SS} = V_{SSAC} = 0$ V, $V_{DD} = V_{DDAC}$

Parameter	Symbol	Rating	Unit
Supply voltage range[1]	V_{DD}, V_{DDAC}	3.00 to 5.25	V
Operating temperature range	T_a	–40 to 85	°C

1. The minimum required operating voltage and consequent operating temperature vary with the maximum operating frequency and sampling mode selected, as shown in the following table.

$V_{SS} = V_{SSAC} = 0$ V, $V_{DD} = V_{DDAC}$

Sampling frequency fs (kHz)	Internal system clock		Minimum supply voltage V_{DD}, V_{DDAC} (V)	Operating temperature T_a (°C)
	Mode[1]	Maximum operating frequency (MHz)		
192	192fs	37	4.75 (5.0 – 5%)	–40 to 70
	256fs	Not guaranteed	Not guaranteed	Not guaranteed
108[2]	192fs	20.7	3.00 (3.3 – 10%)	–40 to 85
	256fs	27.6	4.50 (5.0 – 10%)	
96	192fs	18.5	3.00 (3.3 – 10%)	
	256fs	25	3.00 (3.3 – 10%)	
55.2[3]	192fs	10.6	3.00 (3.3 – 10%)	
	256fs	14.2	3.00 (3.3 – 10%)	

1. Mode with internal frequency divider ratio set to 1 (CKDV1 = CKDV2 = LOW).
2. 96 kHz + 12.5% variable pitch
3. 48 kHz + 15% variable pitch

DC Electrical Characteristics

$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
HIGH-level input voltage[1]	V_{IH1}		$0.7V_{DD}$	–	–	V
HIGH-level input voltage[2,4]	V_{IH2}		2.0	–	–	V
HIGH-level input voltage[3]	V_{IH3}	$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V	2.4	–	–	V
		$V_{DD} = V_{DDAC}$ = 3.00 to 4.75 V	2.0	–	–	
LOW-level input voltage[1]	V_{IL1}	$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V	–	–	$0.3V_{DD}$	V
		$V_{DD} = V_{DDAC}$ = 3.00 to 4.75 V	–	–	$0.2V_{DD}$	
LOW-level input voltage[2,4]	V_{IL2}	$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V	–	–	0.8	V
		$V_{DD} = V_{DDAC}$ = 3.00 to 4.75 V	–	–	$0.2V_{DD}$	
LOW-level input voltage[3]	V_{IL3}	$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V	–	–	0.8	V
		$V_{DD} = V_{DDAC}$ = 3.00 to 4.75 V	–	–	$0.2V_{DD}$	
Input leakage current[1,2]	I_{IL1}	V_{IN} = 0 to 5.25 V	–10	–	10	µA
Input current[3,4]	I_{IL2}	V_{IN} = 0 V	–10	–50	–120	µA
HIGH-level output voltage[5]	V_{OH}	I_{OH} = –4 mA	2.4	–	–	V
LOW-level output voltage[5]	V_{OL}	I_{OL} = 4 mA	–	–	0.4	V

1. Pin XTI
2. Pins LRCI, DI/INF2N, BCKI
3. Pins IW1N/DIL, IW2N/DIR
4. Pins OMD, CKSLN, INF1N, OW1N, OW2N, SYNCN, RSTN, CKDV1, CKDV2, DEMPR, DEMPL, FSEL1, FSEL2, MUTEL, MUTER, DITHN
5. Pins DOR, DOL, WCKO, BCKO, DG, CKO

$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C, XTI = external input, no output load

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD1}	192fs, XTI = 27 ns (37 MHz), fs = 192 kHz, T_a = –40 to 70 °C	–	–	166	mA
	I_{DD2}	256fs, XTI = 40 ns (25 MHz), fs = 96 kHz	–	–	115	mA
	I_{DD3}	384fs, XTI = 27 ns (37 MHz), fs = 96 kHz, estimated value	–	–	105	mA
	I_{DD4}	192fs, XTI = 54 ns (18.5 MHz), fs = 96 kHz, estimated value	–	–	95	mA
	I_{DD5}	384fs, XTI = 54 ns (18.5 MHz), fs = 48 kHz, estimated value	–	–	65	mA

$V_{DD} = V_{DDAC}$ = 3.00 to 3.60 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C, XTI = external input, no output load

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD6}	256fs, XTI = 81 ns (12.3 MHz), fs = 48 kHz, estimated value	–	–	27	mA
	I_{DD7}	384fs, XTI = 54 ns (18.5 MHz), fs = 48 kHz, estimated value	–	–	28	mA

AC Electrical Characteristics

Crystal oscillator (XTI, XTO)

$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator frequency[1]	f_{OSC}		–	–	50	MHz

1. External circuit components should be matched for the crystal oscillator element used.

External clock input (XTI)

$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Master clock frequency	f_{XTI}		–	–	60	MHz
Master clock duty		$1/2V_{DD}$ thresholds	40	–	60	%

Internal system clock

The crystal oscillator frequency or external clock input master clock frequency ratings are described in the preceding tables, but it is the internal system clock frequency rating, set by the internal frequency divider (CKDV1, CKDV2), that must be satisfied. The master clock frequency is a multiple of the sampling frequency fs.

CKDV1 = CKDV2 = LOW (internal system clock frequency = XTI input frequency),
$V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C

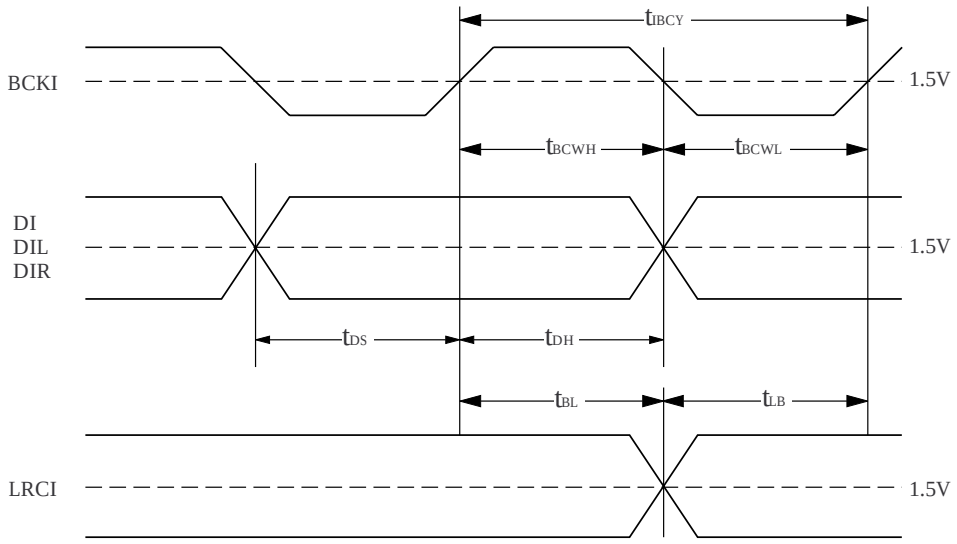
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
256fs (CKSLN = LOW, CKDV1 = LOW, CKDV2 = LOW)						
System clock frequency	f_{SYS1}	$V_{DD} = V_{DDAC}$ = 4.50 to 5.25 V	0.256	–	27.6	MHz
		$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V	0.256	–	25	
192fs (CKSLN = HIGH, CKDV1 = LOW, CKDV2 = LOW)						
System clock frequency	f_{SYS2}	$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V, T_a = –40 to 70 °C	0.384	–	37	MHz
		$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V	0.384	–	20.7	

Serial input timing (BCKI, LRCI, DI/INF2N, IW1N/DIL, IW2N/DIR)

$V_{SS} = V_{SSAC} = 0$ V, $T_a = -40$ to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKI pulse cycle	t_{IBCY}	Note 1	55	–	–	ns
		Note 2	80	–	–	
		Note 3	100	–	–	
BCKI HIGH-level pulsewidth	t_{BCWH}	Note 1	25	–	–	ns
		Note 2	35	–	–	
		Note 3	45	–	–	
BCKI LOW-level pulsewidth	t_{BCWL}	Note 1	25	–	–	ns
		Note 2	35	–	–	
		Note 3	45	–	–	
DI, DIL, DIR setup time	t_{DS}	Note 1	10	–	–	ns
		Note 2	20	–	–	
		Note 3	30	–	–	
DI, DIL, DIR hold time	t_{DH}	Note 1	10	–	–	ns
		Note 2	20	–	–	
		Note 3	30	–	–	
Last BCKI rising edge to LRCI edge	t_{BL}	Note 1	10	–	–	ns
		Note 2	20	–	–	
		Note 3	30	–	–	
LRCI edge to first BCKI rising edge	t_{LB}	Note 1	10	–	–	ns
		Note 2	20	–	–	
		Note 3	30	–	–	

1. CKSLN = HIGH (192fs), $V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V, T_a = –40 to 70 °C
2. CKSLN = LOW (256fs), $V_{DD} = V_{DDAC}$ = 4.50 to 5.25 V
   CKSLN = HIGH (192fs), $V_{DD} = V_{DDAC}$ = 3.00 to 4.75 V
3. CKSLN = LOW (256fs), $V_{DD} = V_{DDAC}$ = 3.00 to 4.50 V

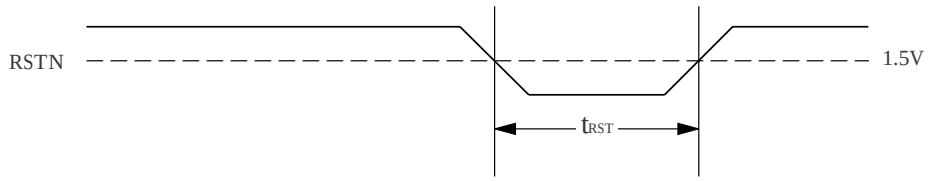


Reset timing (RSTN)

$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C

Parameter	Symbol	Condition	Rating			Unit
			min[1]	typ	max	
RSTN LOW-level reset pulsewidth	t_{RST}		$2t_{MCK}$	–	–	ns

1. t_{MCK} is equal to $1/f_{XTI}$ or $1/f_{OSC}$. For example, t_{RST} = 54 ns when f_{XTI} = 37 MHz.



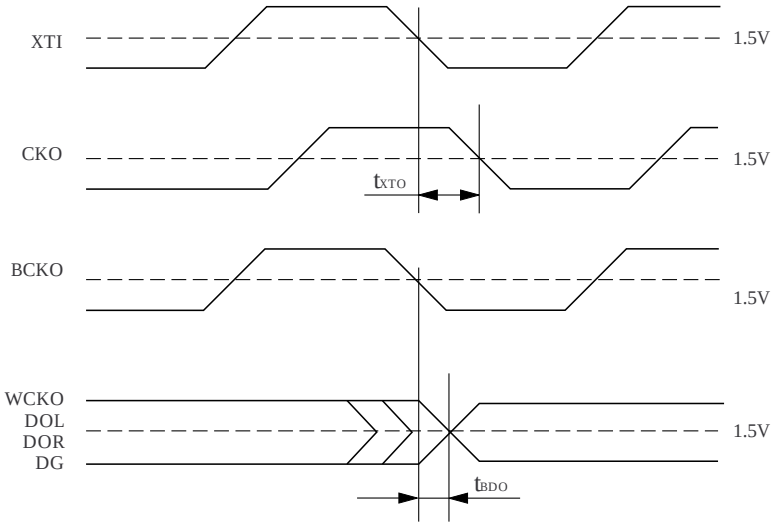
Output timing (CKO, BCKO, WCKO, DOL, DOR, DG)

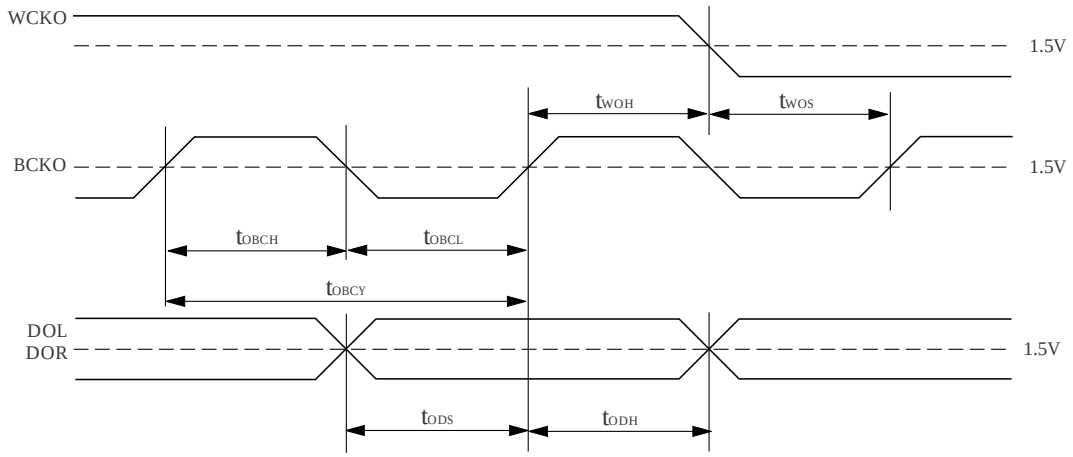
$V_{DD} = V_{DDAC}$ = 4.75 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 70 °C, C_L = 50 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI falling edge to CKO falling edge delay	t_{XTO}		4	–	9	ns
		$V_{DD} = V_{DDAC}$ = 3.00 to 5.25 V, T_a = –40 to 85 °C	4	–	11	ns
BCKO falling edge to WCKO, DOL, DOR, DG delay	t_{BDO}		–4	–	2	ns
BCKO rising edge to WCKO falling edge	t_{WOH}	Output mode: 8fs OMD = HIGH (fs = 192 kHz) External clock input: XTI = 27 ns (37 MHz), CKSLN = HIGH (192fs) Divider ratio: 1 CKDV1 = CKDV2 = LOW Output data length: 24 bits OW1N = OW2N = LOW	8	–	–	ns
WCKO falling edge to BCKO rising edge	t_{WOS}		8	–	–	ns
BCKO period	t_{OBCY}		27	–	–	ns
BCKO HIGH-level pulsewidth	t_{OBCH}		7	–	–	ns
BCKO LOW-level pulsewidth	t_{OBCL}		7	–	–	ns
DOL, DOR setup time	t_{ODS}		7	–	–	ns
DOL, DOR hold time	t_{ODH}		7	–	–	ns
BCKO rising edge to WCKO falling edge	t_{WOH}	Output mode: 4fs OMD = LOW (fs = 192 kHz) External clock input: XTI = 27 ns (37 MHz), CKSLN = HIGH (192fs) Divider ratio: 1 CKDV1 = CKDV2 = LOW Output data length: 24 bits OW1N = OW2N = LOW	17	–	–	ns
WCKO falling edge to BCKO rising edge	t_{WOS}		17	–	–	ns
BCKO period	t_{OBCY}		54	–	–	ns
BCKO HIGH-level pulsewidth	t_{OBCH}		18	–	–	ns
BCKO LOW-level pulsewidth	t_{OBCL}		18	–	–	ns
DOL, DOR setup time	t_{ODS}		18	–	–	ns
DOL, DOR hold time	t_{ODH}		18	–	–	ns

$V_{DD} = V_{DDAC}$ = 4.50 to 5.25 V, $V_{SS} = V_{SSAC}$ = 0 V, T_a = –40 to 85 °C, C_L = 50 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKO HIGH-level pulsewidth	t_{OBCH}	External clock input: XTI = 36 ns (27.6 MHz), CKSLN = LOW (256fs), fs = 108 kHz Divider ratio: 1 CKDV1 = CKDV2 = LOW Output mode: 8fs, OMD = HIGH	10	–	–	ns
BCKO LOW-level pulsewidth	t_{OBCL}		10	–	–	ns
DOL, DOR setup time	t_{ODS}		11	–	–	ns
DOL, DOR hold time	t_{ODH}		11	–	–	ns
BCKO HIGH-level pulsewidth	t_{OBCH}	External clock input: XTI = 36 ns (27.6 MHz), CKSLN = LOW (256fs), fs = 108 kHz Divider ratio: 1 CKDV1 = CKDV2 = LOW Output mode: 4fs, OMD = LOW	26	–	–	ns
BCKO LOW-level pulsewidth	t_{OBCL}		26	–	–	ns
DOL, DOR setup time	t_{ODS}		27	–	–	ns
DOL, DOR hold time	t_{ODH}		27	–	–	ns



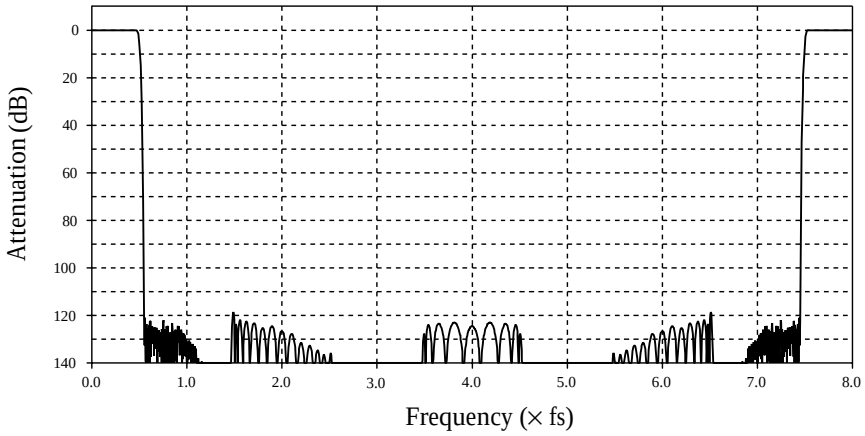


Filter Characteristics

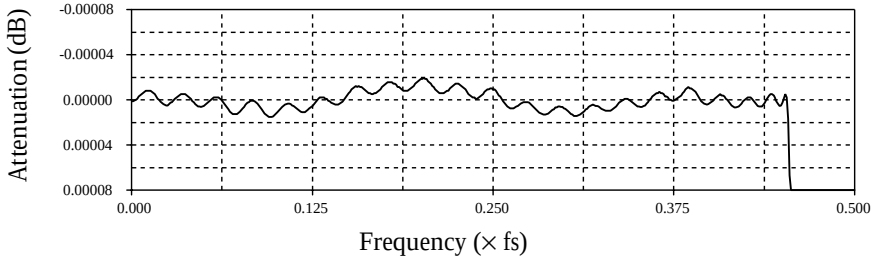
8-times interpolation filter

Parameter	Rating
Passband	0 to 0.4535fs
Stopband	0.5465fs to 7.4535fs
Passband ripple	≤ ±0.00002 dB
Stopband attenuation	≥ 117 dB
Group delay	Constant

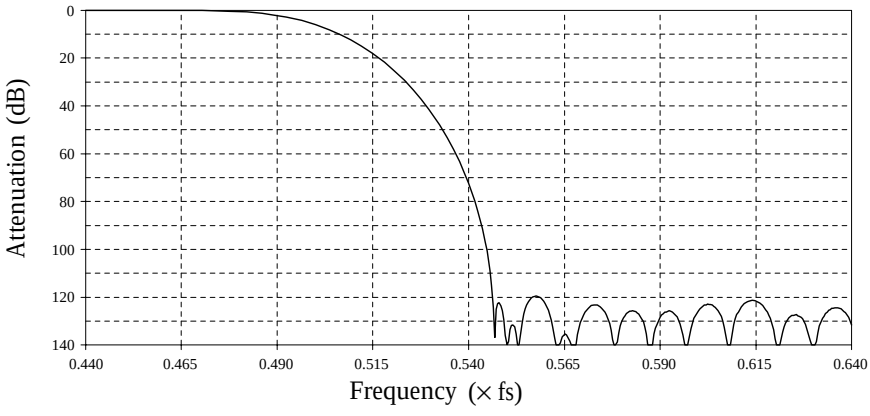
8fs filter response with deemphasis OFF



8fs filter band transition response with deemphasis OFF



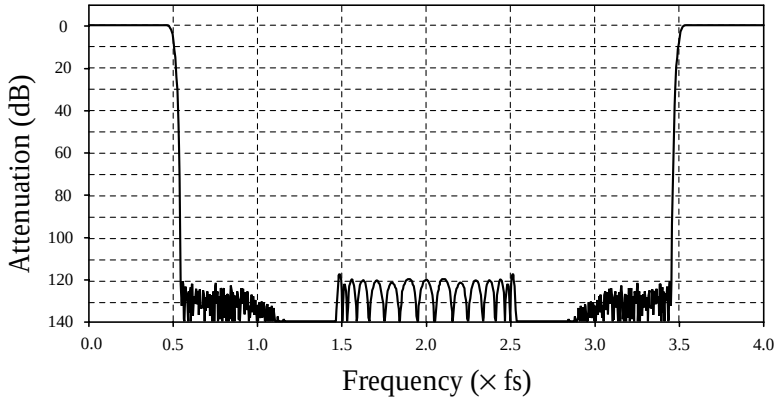
8fs filter passband response with deemphasis OFF



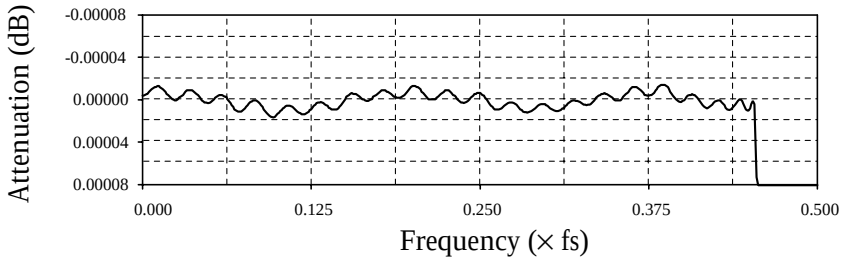
4-times interpolation filter

Parameter	Rating
Passband	0 to 0.4535fs
Stopband	0.5465fs to 3.4535fs
Passband ripple	≤ ±0.00002 dB
Stopband attenuation	≥ 116 dB
Group delay	Constant

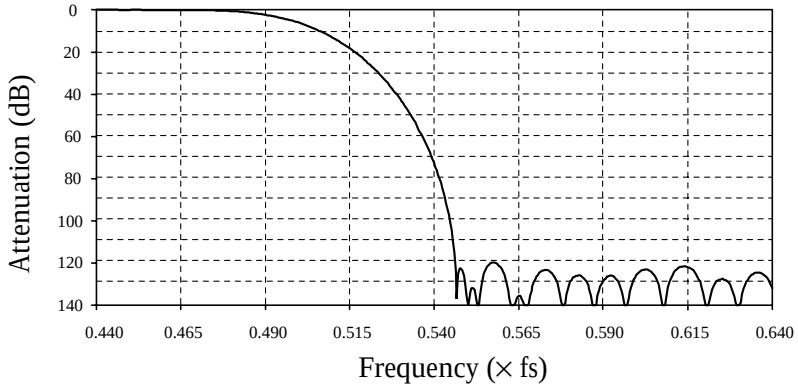
4fs filter response with deemphasis OFF



4fs filter band transition response with deemphasis OFF



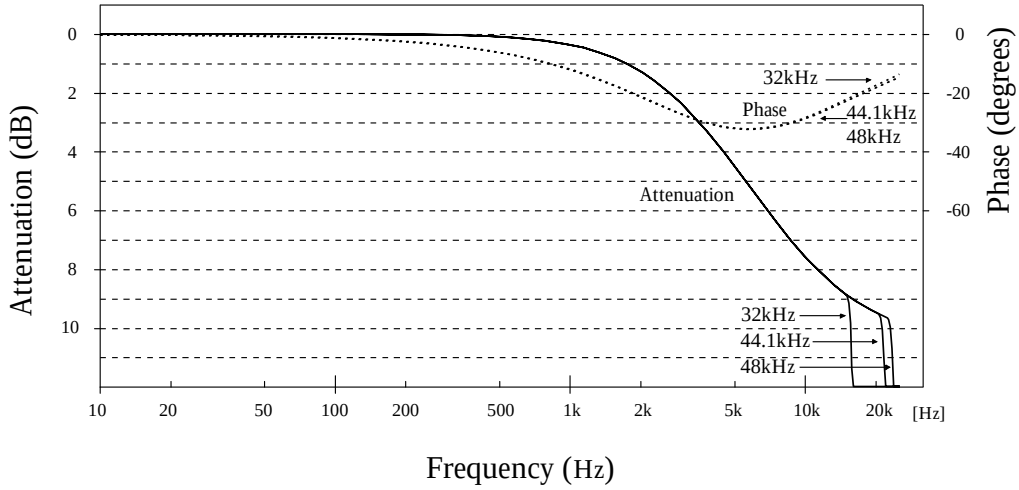
4fs filter passband response with deemphasis OFF



Deemphasis filter

Parameter		Sampling frequency (fs)		
		32 kHz	44.1 kHz	48 kHz
Passband bandwidth (kHz)		0 to 14.5	0 to 20.0	0 to 21.7
Deviation from ideal characteristic	Attenuation	≤ ±0.01 dB		
	Phase, θ	0 to 1.5°		

Passband response with deemphasis ON



FUNCTIONAL DESCRIPTION

Oversampling (Interpolation)

The interpolation arithmetic block is comprised of 3 cascaded, 2-times FIR interpolation filters, as shown in figure 1. The input signal is sampled at rate fs, and then either 4-times or 8-times oversampling data is output. Sampling noise in the 0.5465fs to 3.4535fs (4fs output) or 0.5465fs to 7.4535fs (8fs output) region is removed.

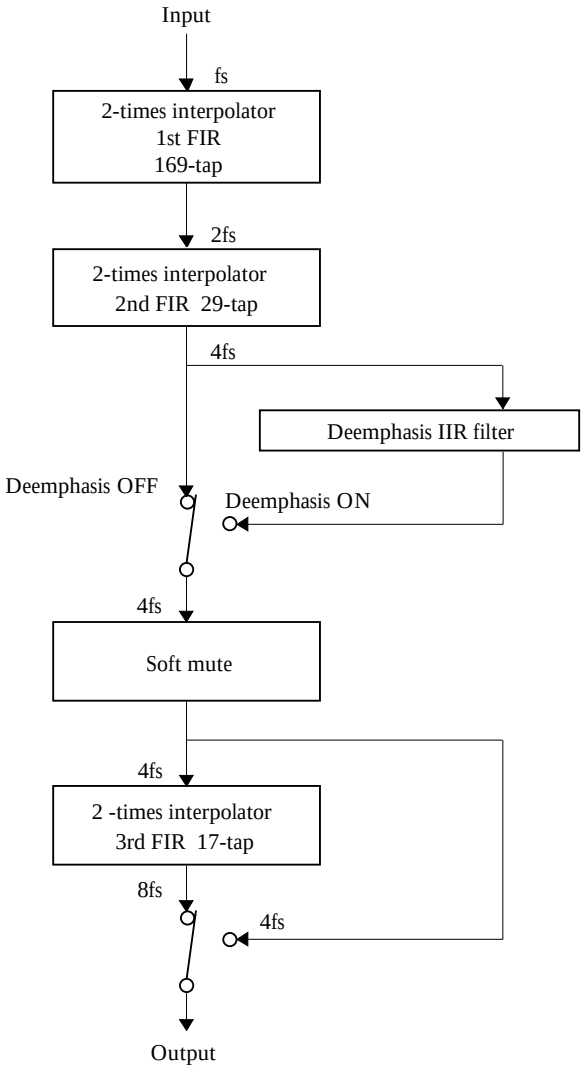


Figure 1. Arithmetic operating block

Digital Deemphasis (DEMPL, DEMPR, FSEL1, FSEL2)

Most deemphasis filters are constructed using analog circuit techniques. Here, an IIR filter is employed to faithfully reproduce the gain and phase characteristics of standard analog deemphasis filters, corresponding to analog 50µs/15µs frequency characteristics. Three sets of filter coefficients for the three fs = 32/44.1/48 kHz sampling frequencies are supported. Deemphasis for other values of fs are not supported.

Deemphasis ON/OFF (DEMPL, DEMPR)

Deemphasis for the left and right-channel can be controlled independently.

Table 1. Deemphasis control

DEMPL	DEMPR	Deemphasis
LOW	×	Left-channel OFF
HIGH	×	Left-channel ON
×	LOW	Right-channel OFF
×	HIGH	Right-channel ON

Filter coefficient select (FSEL1, FSEL2)

Table 2. Deemphasis filter coefficient select

FSEL1	FSEL2	Sampling frequency (fs)
LOW	LOW	44.1 kHz
LOW	HIGH	48 kHz
HIGH	LOW	Prohibited mode
HIGH	HIGH	32 kHz

Soft Muting (MUTEL, MUTER)

The muting function controls the muting of left and right-channel independently. Input data continues to be accepted even when mute is operating.

Mute ON/OFF

When MUTEL (MUTER) goes HIGH, the attenuation changes smoothly from 0 to –∞ dB. Similarly, when MUTEL (MUTER) goes LOW, muting is released and the attenuation changes smoothly from –∞ to 0 dB. This operation is termed soft muting.

Soft muting takes an interval of approximately 512/fs, or about 11.6 ms when fs = 44.1 kHz.

Table 3. Mute control

MUTEL	MUTER	Soft muting
LOW	×	Left-channel OFF
HIGH	×	Left-channel ON
×	LOW	Right-channel OFF
×	HIGH	Right-channel ON

Mute operation at reset

When RSTN goes LOW, the DOL and DOR outputs are immediately muted to –∞ dB. When RSTN goes HIGH, reset is released and the outputs are immediately set to 0 dB attenuation.

Note that even when either MUTEL or MUTER or both are HIGH, the reset operation takes precedence.

Analog Output Click Noise

Under the following conditions, a click noise may be output from the DAC (digital-to-analog converter) connected to the SM5847AF.

- When a system reset on RSTN occurs
- When the internal system clock mode, set by CKSLN, CKDV1, and CKDV2, is switched
- When the deemphasis mode, set by DEMPL, DEMPR, FSEL1, and FSEL2, is switched
- When the audio data input mode, set by INF1N, DI/INF2N, IW1N/DIL, and IW2N/DIR, is switched
- When the SYNCN jitter-free mode switch timing exceeds the internal timing delay limit

An external muting circuit connected to the analog output may be required to eliminate this noise.

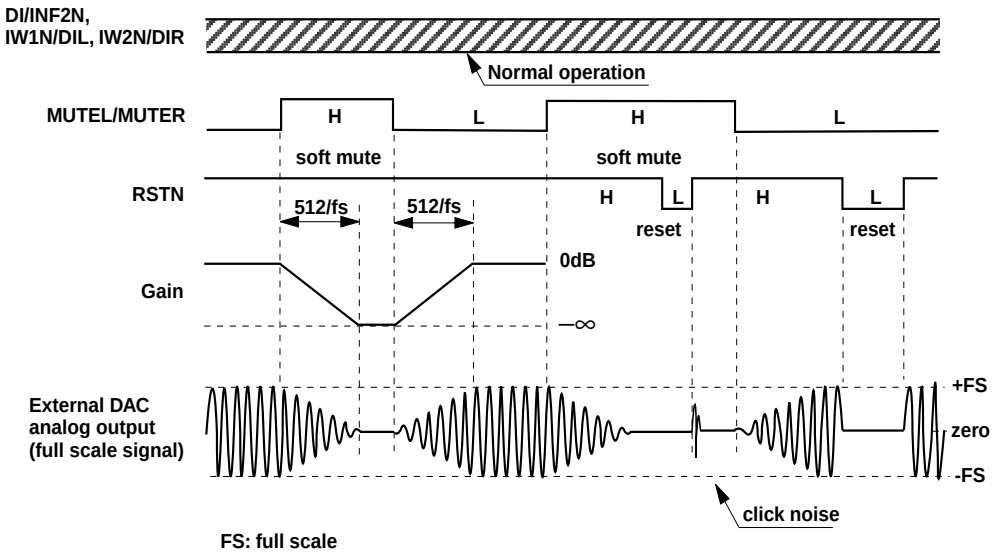


Figure 2. Soft muting/reset operation

Internal System Clock (XTI, XTO, CKO, CKSLN, CKDV1, CKDV2)

The SM5847AF supports two system clock frequencies selected by CKSLN, 192fs and 256fs, where fs is the sampling frequency.

The master clock can be provided either by a crystal oscillator connected between XTI and XTO, or by an external master clock input on XTI. Note that the feedback resistor required by the oscillator option is not built-in. External components should be selected to match the crystal oscillator element. Note also that XTO must be left open (floating) for the external master clock input option.

Note that even though it is necessary that the master clock and LRCI clock (sampling frequency fs) be in sync, it is not necessary that they be exactly in-phase (see jitter-free mode description).

The SM5847AF features independent divide-by 1, 2, or 4counter, selected by CKDV1 and CKDV2. This provides the 192fs or 256fs system clock with the necessary divider ratios to support master clocks with frequencies of 768fs, 384fs, 192fs, 1024fs, 512fs or 256fs.

Normal sampling frequencies 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz and 192 kHz are supported. However, some combinations of sampling frequency and master clock frequency are not supported, as follows.

- 768fs and 1024fs at 88.2 and 96 kHz
- 768fs, 384fs, 1024fs, 512fs, and 256fs at 176.4 kHz
- 768fs, 384fs, 1024fs, 512fs and 256fs at 192 kHz

Note also that the internal crystal oscillator circuit cannot operate at frequencies ≥ 50 MHz. The master clock input on XTI is output on CKO.

Master clock stop operation

The master clock is input after power is applied.

But if, after the XTI and LRCI clocks are input and power-ON reset occurs with all-zero input audio data, the master clock input on XTI is held either HIGH or LOW level, operation effectively stops. Note also that a reset signal is not accepted when the master clock and LRCI clock stop.

Table 4. Internal system clock select

CKSLN	System clock
LOW	256fs
HIGH	192fs

Table 5. System clock frequency divider ratio select

CKDV1	CKDV2	Divider ratio	Master clock
LOW	LOW	1	192fs, 256fs
LOW	HIGH	–	Prohibited mode
HIGH	LOW	4	768fs, 1024fs
HIGH	HIGH	2	384fs,512fs

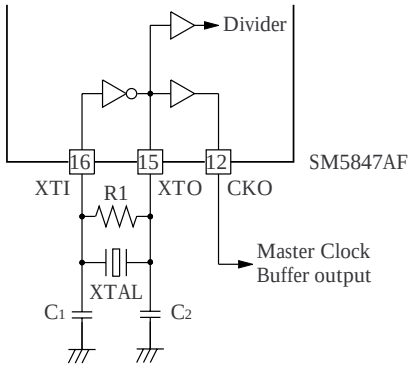


Figure 3. Crystal oscillator connection

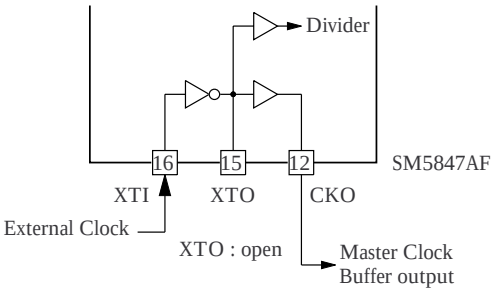


Figure 4. External clock connection

Table 6. Master clock frequency example

Sampling frequency fs (kHz)	XTI system clock frequency (MHz)											
	CKSLN = HIGH (192fs)						CKSLN = LOW (256fs)					
	CKDV1	CKDV2	CKDV1	CKDV2	CKDV1	CKDV2	CKDV1	CKDV2	CKDV1	CKDV2	CKDV1	CKDV2
	LOW	LOW	HIGH	HIGH	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH	LOW
	192fs		384fs		768fs		256fs		512fs		1024fs	
32	6.144		12.288		24.576		8.192		16.384		32.768	
44.1	8.4627		16.9344		33.8688		11.2896		22.5792		45.1584	
48	9.216		18.432		36.864		12.288		24.576		49.152	
88.2	16.9344		33.8688		Not guaranteed[1]		22.5792		45.1584		Not guaranteed	
96	18.432		36.864		Not guaranteed		24.576		49.152		Not guaranteed	
176.4	33.8688		Not guaranteed		Not guaranteed		Not guaranteed		Not guaranteed		Not guaranteed	
192	36.864		Not guaranteed		Not guaranteed[1]		Not guaranteed		Not guaranteed		Not guaranteed	

1. Refer to the AC characteristics system clock ratings.

System Reset (RSTN)

During normal device operation, reset signals are not required. However, the SM5847AF must be reset under the following conditions.

- At power-ON
- When the LRCI clock and internal operation timing need to be resynchronized in jitter-free mode.
- After the LRCI or XTI clocks, or both, stop and are subsequently started.

The system is reset by applying a LOW-level pulse on RSTN.

When RSTN is LOW, the DOL and DOR outputs are tied LOW, muting the output signal to an attenuation level of −∞.

After system reset, when RSTN goes HIGH, the arithmetic and output timing counters are reset on the first LRCI start edge, assuming that the XTI and LRCI input clocks have already stabilized. The LRCI start edge is determined by the state of INF1N and INF2N. When INF1N is LOW or when both INF1N and INF2N are HIGH, the start edge is the rising edge. When INF1N is HIGH and INF2N is LOW, the start edge is the falling edge.

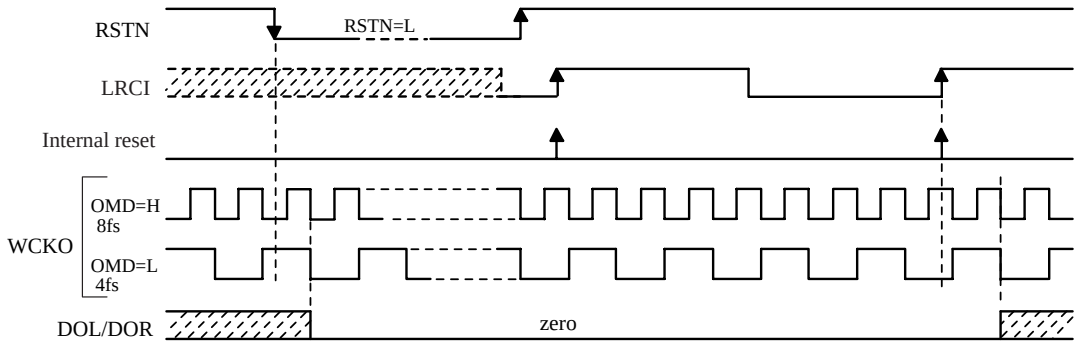


Figure 5. System reset timing and output muting (INF1N = LOW or INF1N = INF2N = HIGH)

Audio Data Input (INF1N, DI/INF2N, IW1N/DIL, IW2N/DIR, BCKI, LRCI)

The input data format and input pin functions are selected by the state of INF1N and INF2N. When INF1N is LOW, the inputs are left and right-channel data inputs, and when INF1N is HIGH, the DI/INF2N input is an input format select pin, and DIL and DIR are the audio data inputs.

Input data format select

Table 7. Input settings and functions

INF1N	DI/INF2N	Input format	Pin function selection		
			DI/INF2N	IW1N/DIL	IW2N/DIR
LOW	–	LR alternating[1], right-justified data	DI	IW1N	IW2N
LOW	–				
HIGH	LOW	LR alternating, left-justified data	INF2N	DIL	DIR
HIGH	HIGH	LR simultaneous[2], left-justified data			

1. Alternating left-channel and right-channel data input on a single input DI.
2. Simultaneous left-channel and right-channel data input on two inputs, DIL and DIR, respectively.

Input data word length

The input data word length is selected by the state of IW1N and IW2N when INF1N is LOW. 20-bit is selected when INF1N is HIGH.

Table 8. Input data word length select

INF1N	IW1N/DIL	IW2N/DIR	Input word length
LOW	LOW	LOW	24 bits
	HIGH	LOW	20 bits
	LOW	HIGH	18 bits
	HIGH	HIGH	16 bits
HIGH	–	–	24 bits

Jitter-free Function (SYNCN)

The arithmetic circuit and output control timing is derived from the system clock, and is therefore independent of the input LRCI and BCKI clocks. Accordingly, any jitter in the data input clock (LRCI and BCKI) does not cause jitter in the output.

Generally, the internal timing is synchronized to the LRCI input timing after a system reset release, when RSTN goes from LOW to HIGH, on the first LRCI clock start edge. If the input timing and LRCI start edge timing subsequently drift, the input timing is automatically resynchronized when the timing error exceeds a certain value. There are 2 timing error values at which resynchronization occurs, selected by the state of SYNCN.

Jitter-free mode (SYNCN = HIGH)

When SYNCN is HIGH, the timing error value is ±3/8 × (LRCI clock period). When the difference between the input timing and LRCI start edge position do not exceed this value, internal timing is not resynchronized and all functions continue to operate normally.

Sync mode (SYNCN = LOW)

When SYNCN is LOW, the timing error value is ±1 × (XTI master clock period), which is a much smaller timing error tolerance than in jitter-free mode. In this mode, the internal timing is guaranteed to follow the LRCI clock timing within this tolerance, making this mode useful for systems constructed from a multiple number of SM5847AF devices.

Audio Data Output (DOL, DOR, BCKO, WCKO, DG, OW1N, OW2N, OMD, DITHN)

Output data format

The output data is in serial, simultaneous left and right-channel, 2s complement, MSB first, BCKO burst (NPC format) format. Left-channel data is output on DOL, and right-channel data is output on DOR.

Output data word length

The output data word length is selected by the state of OW1N and OW2N.

Table 9. Output data word length select

OW1N	OW2N	Output word length
LOW	LOW	24 bits
HIGH	LOW	22 bits
LOW	HIGH	20 bits
HIGH	HIGH	18 bits

Output timing

The output timing is dependent on the CKSLN level and output data word length.

When CKSLN is LOW, the output timing does not change with the output data word length. However, when CKSLN is HIGH, the DOL and DOR output timing for 24-bit output data length (OW1N = OW2N = LOW) start 1 clock cycle earlier than for 18, 20, or 22-bit output data length.

Table 10. Output timing

Parameter	Symbol	CKSLN	OMD = HIGH	OMD = LOW
Bit clock rate	T_B	HIGH	1/192fs	1/96fs
		LOW	1/256fs	1/128fs
Data word length	T_{DW}	HIGH	$24t_{SYS}$	$48t_{SYS}$
		LOW	$32t_{SYS}$	$64t_{SYS}$

Output mode

The output mode, either 4fs oversampling or 8fs oversampling, is selected by the level on OMD, where fs is the input sampling rate.

Table 11. Output mode select

OMD	Output mode
LOW	4fs
HIGH	8fs

Output dither processing

The output data word length is set by OW1N and OW2N, whereas the SM5847AF performs all internal calculations in 25-bit words. As a consequence, dither processing is provided to round-off errors. The SM5847AF uses triangular dither processing (triangular probability density function or TPDF) and can be turned ON or OFF. Simple round-off processing occurs when dither is OFF (DITHN = HIGH).

Table 12. Dither select

DITHN	Dither
LOW	ON
HIGH	OFF

Group Delay

The data input to data output group delay is the delay which occurs due to the digital filter calculations. It is the time between the serial input data is completely read in (at rate fs) until the serial data is output (at rate 8fs or 4fs, depending on the mode selected).

t_{INPUT} represents the LRCI clock rising edge after the serial input data has been read in at rate fs.

t_{OUTPUT} represents the WCKO clock falling edge at the start of serial data output at rate 8fs or 4fs.

Table 13. Group delay

Mode			Group delay	Unit
CKSLN	SYNCN		$t_{OUTPUT} - t_{INPUT}$	
LOW (256fs)	LOW	After reset, or sync mode	48.625/fs	sec
	HIGH	Jitter-free mode	48.25/fs – 49.0/fs	
HIGH (192fs)	LOW	After reset, or sync mode	48.75/fs	
	HIGH	Jitter-free mode	48.375/fs – 49.125/fs	

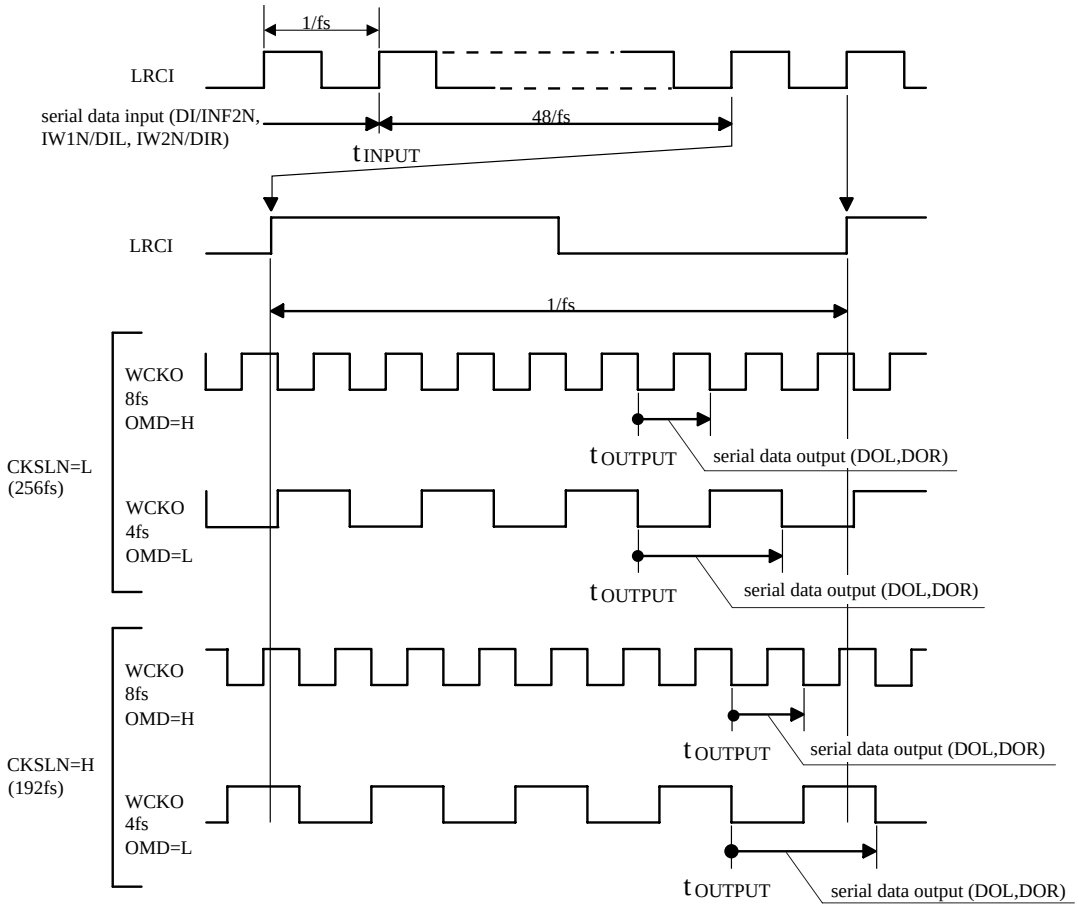
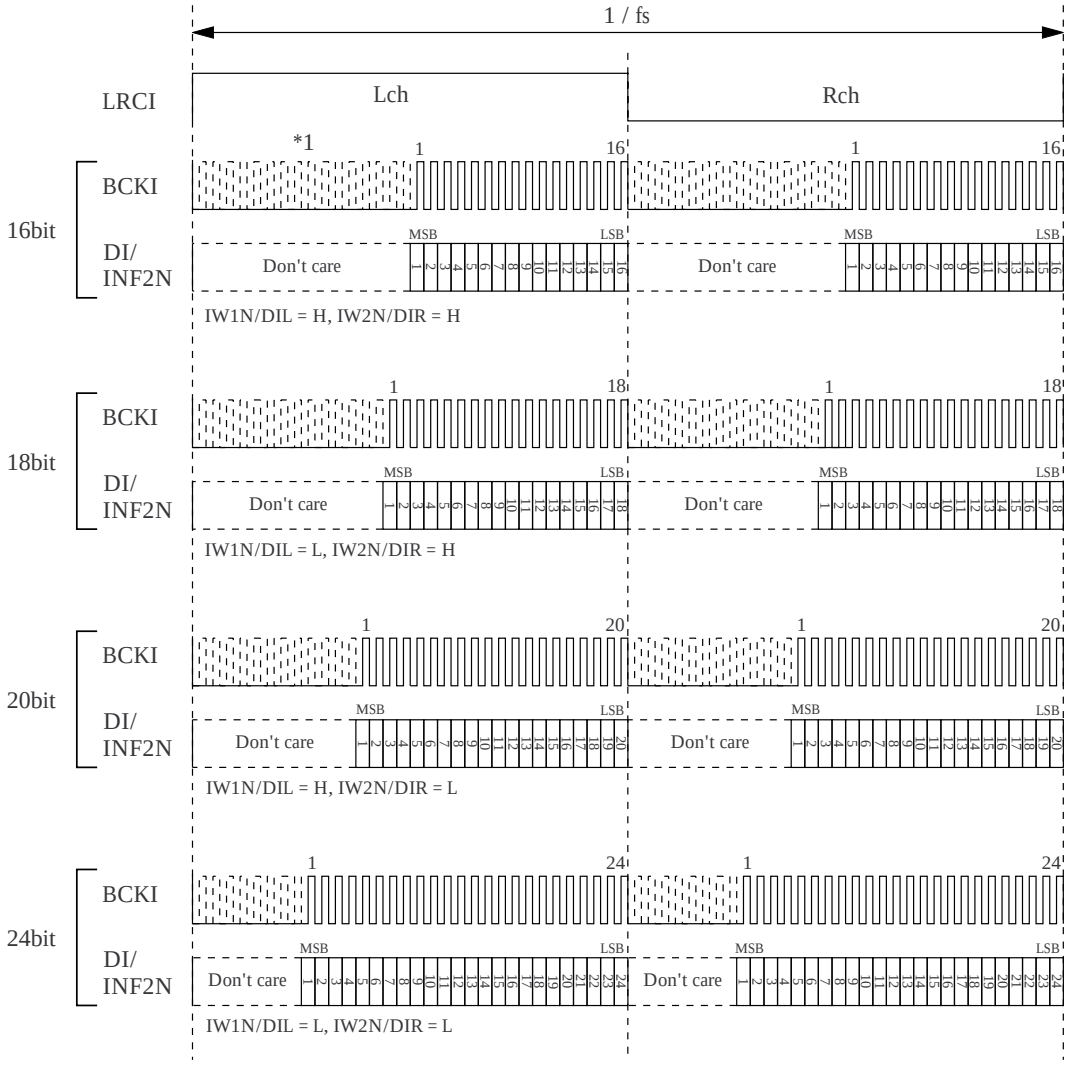


Figure 6. Group delay timing (SYNCN = LOW)

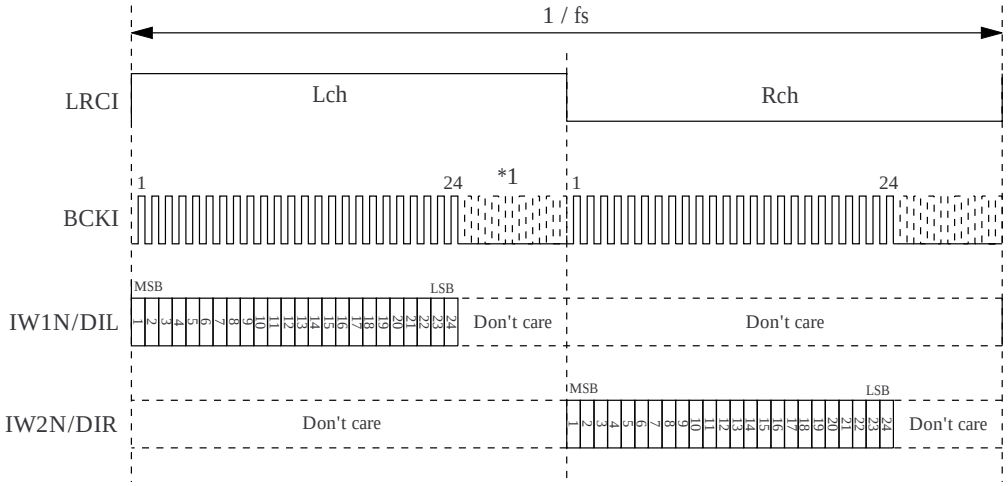
TIMING DIAGRAMS

Input Timing Examples



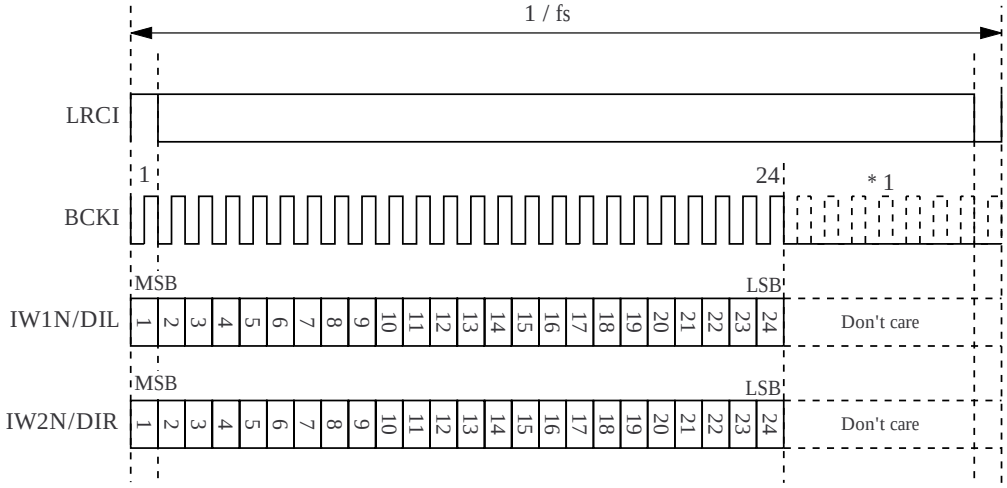
*1: Optional BCKI clock cycles

Figure 7. LR alternating, right-justified data, 2s complement, MSB first, INF1N = L



*1: There must be a minimum of 24 BCKI clock cycles. Data input after the LSB is ignored.

Figure 8. LR alternating, left-justified data, 2s complement, MSB first, INF1N = H, DI/INF2N = L, 24-bit



*1: There must be a minimum of 24 BCKI clock cycles. Data input after the LSB is ignored.

Figure 9. LR simultaneous, left-justified data, 2s complement, MSB first, INF1N = H, DI/INF2N = H, 24-bit

Output Timing Examples

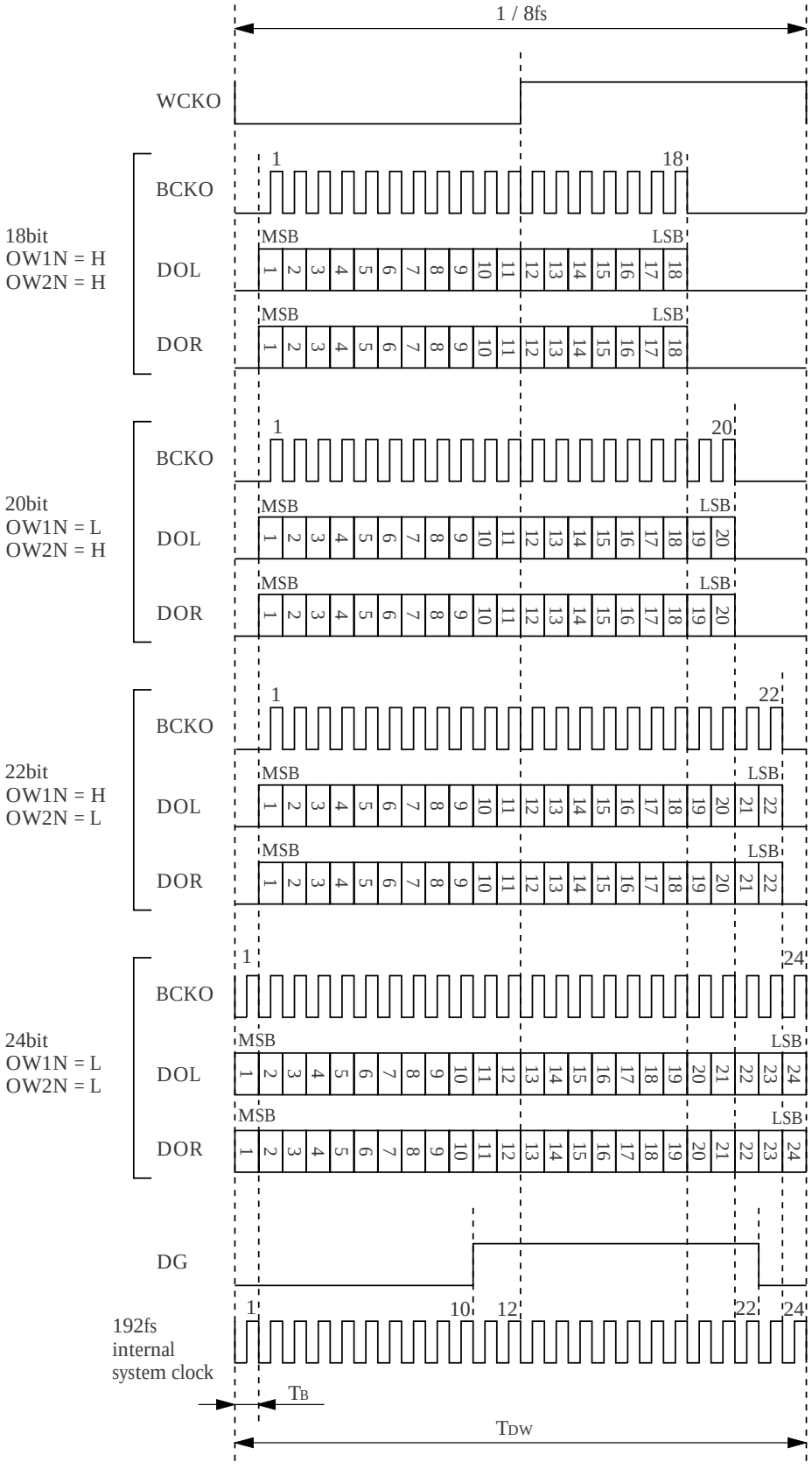


Figure 10. 2s complement, MSB first, CKSLN = H, OMD = H

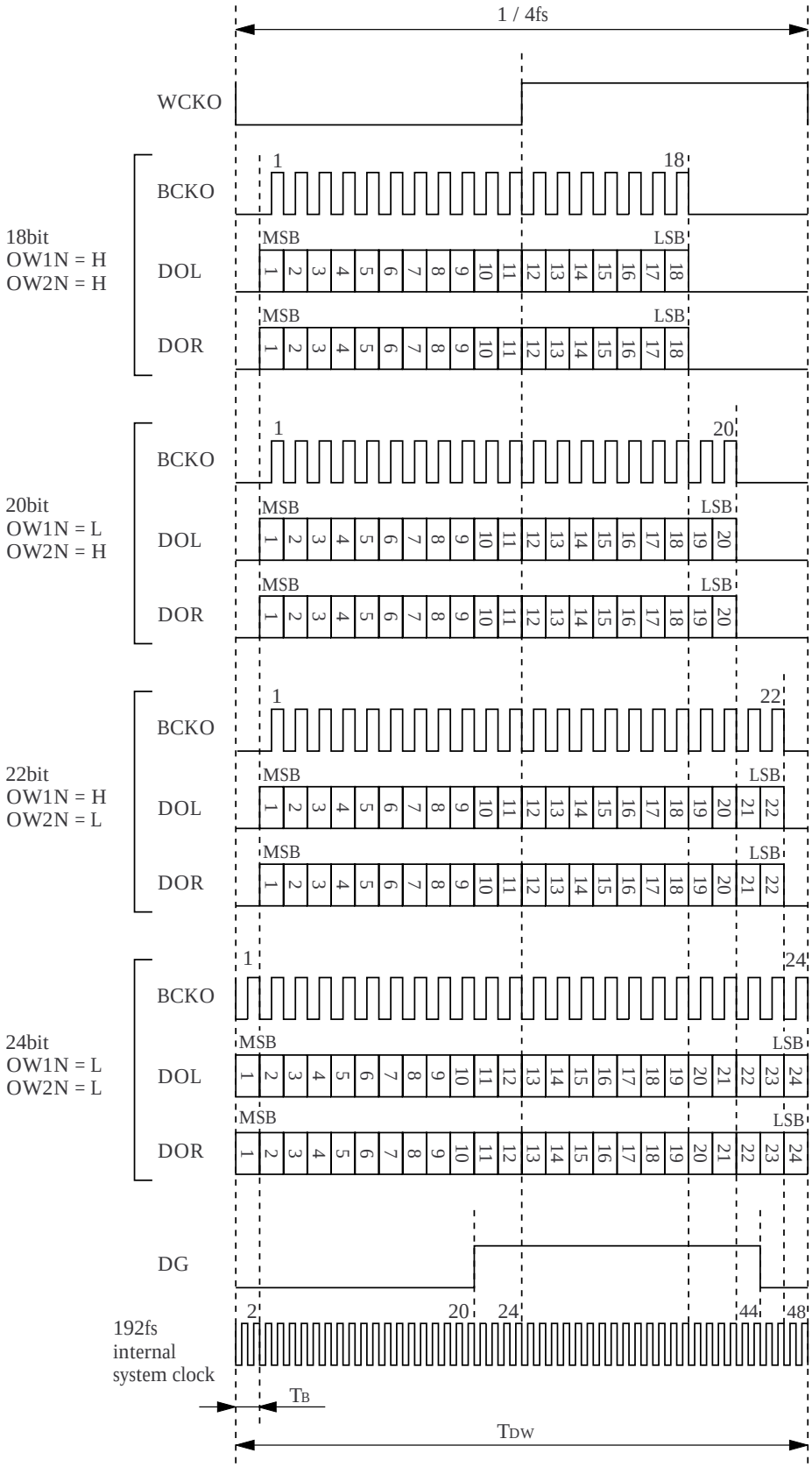


Figure 11. 2s complement, MSB first, CKSLN = H, OMD = L

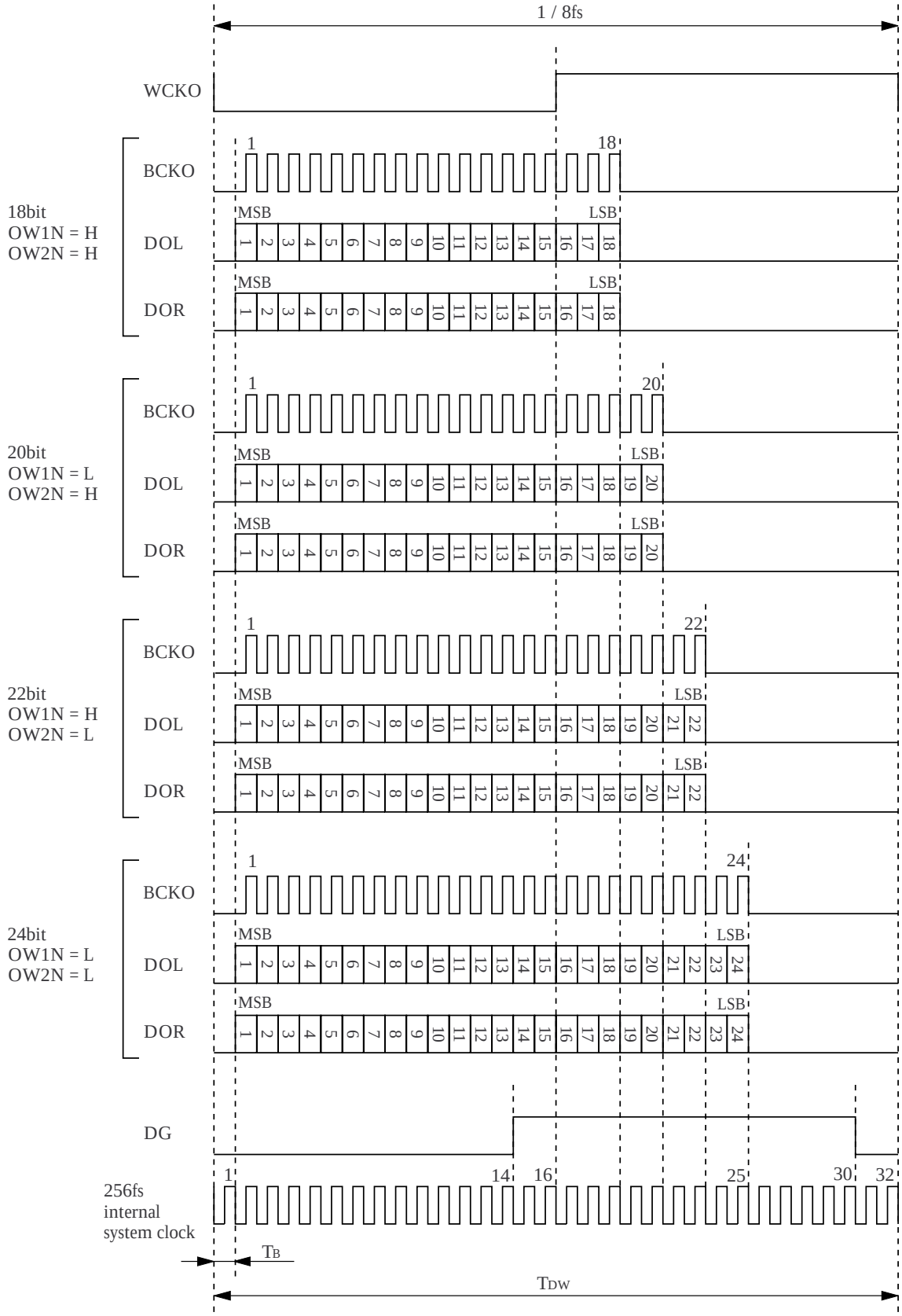


Figure 12. 2s complement, MSB first, CKSLN = L, OMD = H

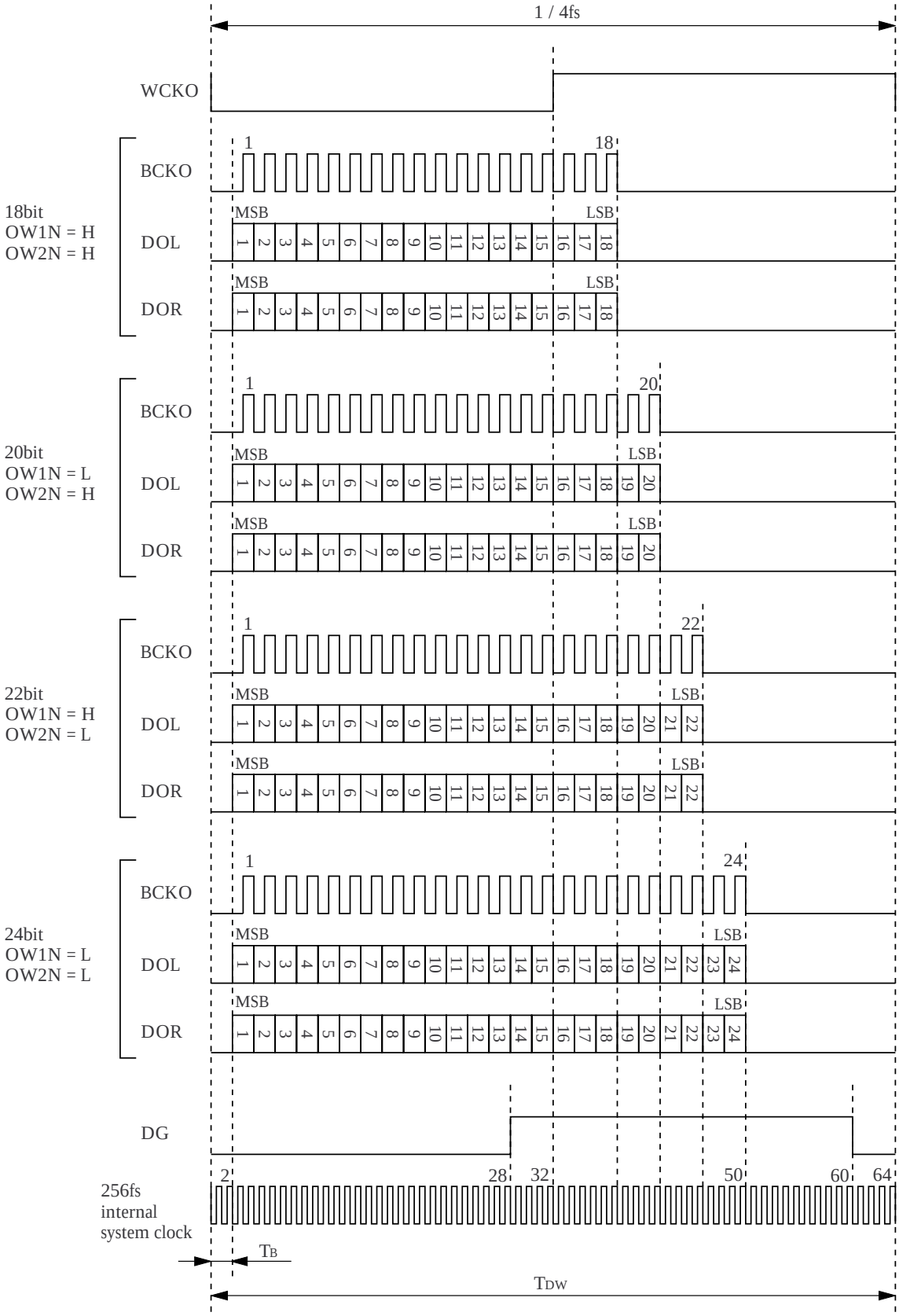


Figure 13. 2s complement, MSB first, CKSLN = L, OMD = L

TYPICAL APPLICATION (1)

This circuit shows a basic connection to a 24-bit input DAC (SM5865BM).

36.864 MHz external clock, 48/96/192 kHz sampling rate fs, 24-bit data, 8fs oversampling operation (Note that certain circuit details required for good DAC analog output characteristics have been omitted.)

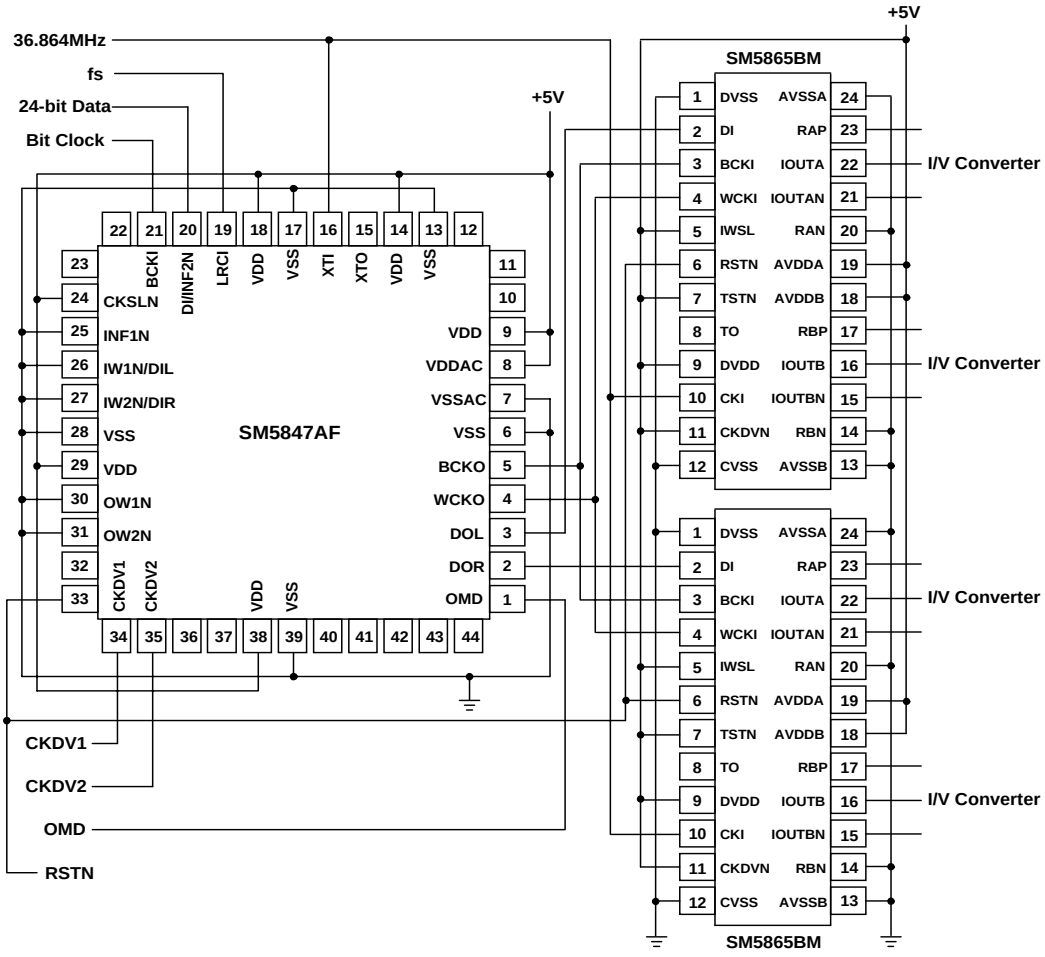


Figure 14. SM5847AF and SM5865BM connection

Table 14. Operating mode select

Sampling frequency fs (kHz)	Internal system clock frequency divider ratio select				Output mode select		External clock XTI (MHz)
	CKSLN = HIGH (192fs)						
	Mode	CKDV1	CKDV2	Divider	OMD	Output mode	
48	768fs	HIGH	LOW	4	HIGH	8fs	36.864
96	384fs	HIGH	HIGH	2	HIGH	8fs	
192	192fs	LOW	LOW	1	HIGH	8fs	

TYPICAL APPLICATION (2)

This circuit shows a basic connection to a 24-bit input DAC (Burr-Brown PCM1704U).

36.864 MHz external clock, 48/96/192 kHz sampling rate fs, 24-bit data, 8fs or 4fs oversampling operation (Note that certain circuit details required for good DAC analog output characteristics have been omitted.)

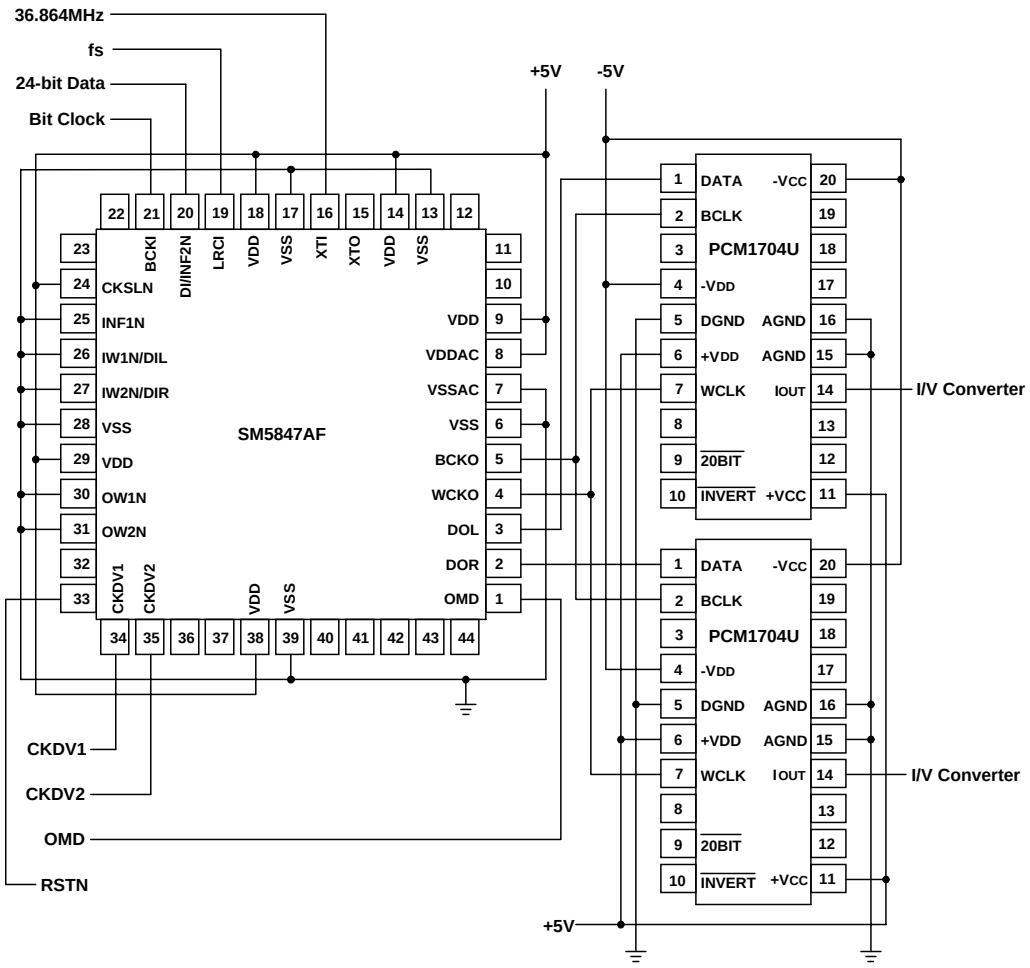


Figure 15. SM5847AF and Burr-Brown PCM1704U connection

Table 15. Operating mode select

Sampling frequency fs (kHz)	Internal system clock frequency divider ratio select				Output mode select		External clock XTI (MHz)
	CKSLN = HIGH (192fs)						
	Mode	CKDV1	CKDV2	Divider	OMD	Output mode	
48	768fs	HIGH	LOW	4	HIGH	8fs	36.864
96	384fs	HIGH	HIGH	2	HIGH	8fs	
192	192fs	LOW	LOW	1	LOW	4fs	

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