NIPPON PRECISION CIRCUITS INC.

SM5846AP

Multi-function Digital Filter

OVERVIEW

The SM5846AP is a multi-function digital filter that incorporates 4/8 times oversampling digital audio signal reproduction, digital deemphasis, digital attenuation and soft mute functions. The I/O interface allows serial data transmission of 16/20/24/32-bit input data and 20/24-bit output data.

FEATURES

Functions

- 8-times oversampling (interpolation)
- Switchable 8/4 times oversampling output
- Two master clock frequencies
  (refer to Clock Functions)
  - 384fs/512fs (normal-speed sampling)
  - 192fs/256fs (high-speed sampling)
- Digital deemphasis
  - Compatible with 32/44.1/48 kHz (normal-speed) and 64/88.2/96 kHz (high-speed) input sampling frequencies
  - ON/OFF control
- Digital attenuator
  - 128-step attenuation using linear 7-bit data setting
- Soft muting
  - 1016/fs (normal-speed sampling)
  - 2032/fs (high-speed sampling)
- Output data round-off operation (normal round-off or rectangular distribution dither round-off)
- Selectable LR clock polarity
- Microprocessor controllable
- Input data format
  - 2s complement, MSB first, alternating L/R serial
  - 16/20/24/32-bit data selectable
- Output data format
  - 2s complement, MSB first, simultaneous L/R serial
  - 20/24-bit data selectable.
- 24-bit internal data processing
- Jitter-free mode/synchronous mode selectable
- Crystal oscillator circuit built-in
- TTL-compatible outputs
- Molybdenum-gate CMOS

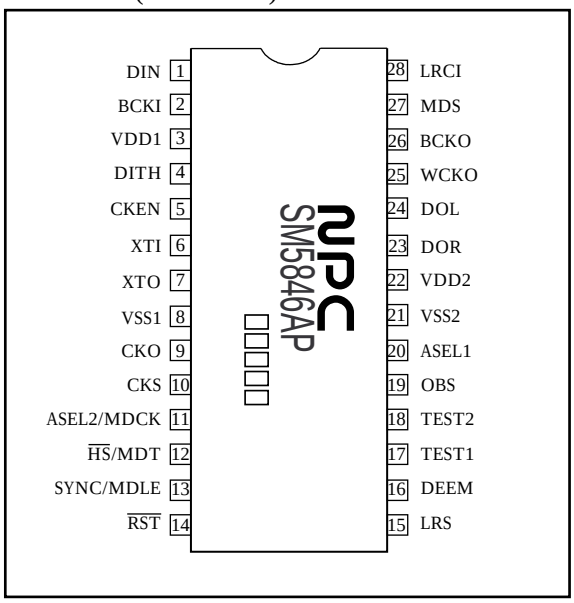
Filter Construction

- Interpolation filter (linear 3-stage FIR filter)
  - Normal-speed sampling mode
    1st stage (fs to 2fs) 121st order
    2nd stage (2fs to 4fs) 21st order
    3rd stage (4fs to 8fs) 13th order
  - High-speed sampling mode:
    1st stage (fs to 2fs) 177th order
    2nd stage (2fs to 4fs) 29th order
    3rd stage (4fs to 8fs) 17th order
- Deemphasis filter (IIR filter)
- Arithmetic units
  - 25× 24-bit parallel adder
  - 32-bit accumulator
- Overflow limiter built-in

Applications

- Digital audio equipment

PINOUT (TOP VIEW)



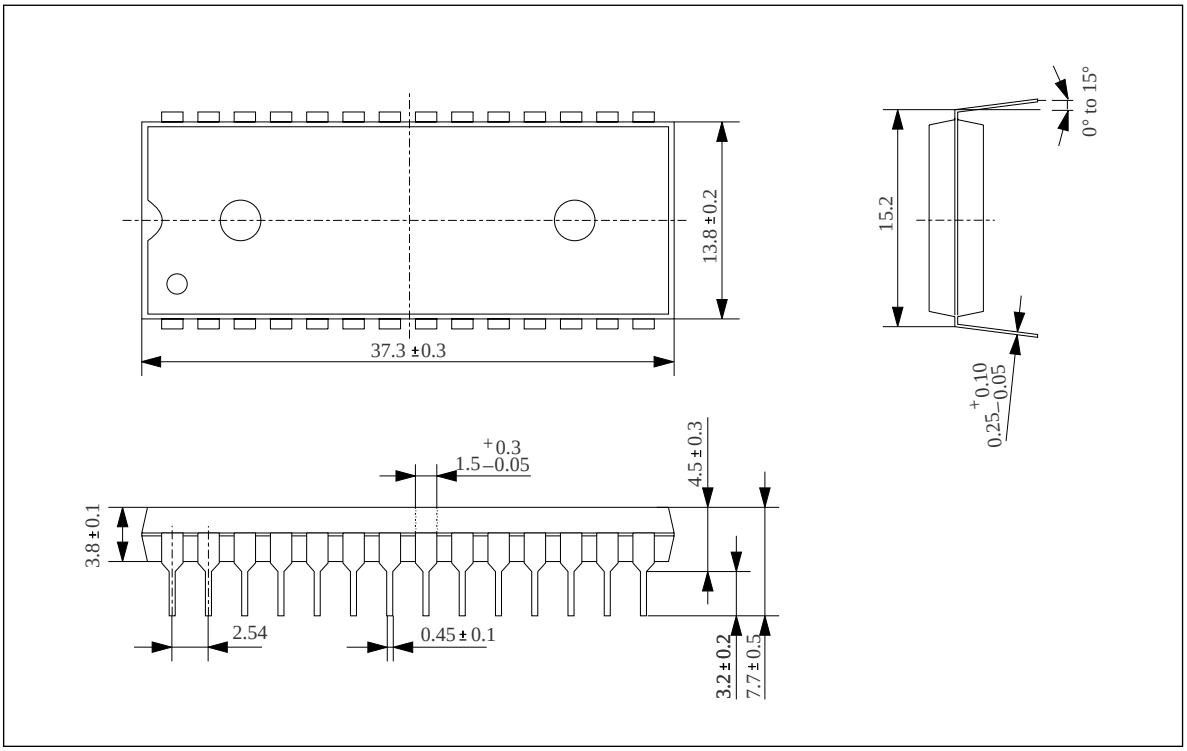
ORDERING INFOMATION

Device	Package
SM5846AP	28pin DIP

PACKAGE DIMENSIONS

Unit: mm

28-pin plastic DIP



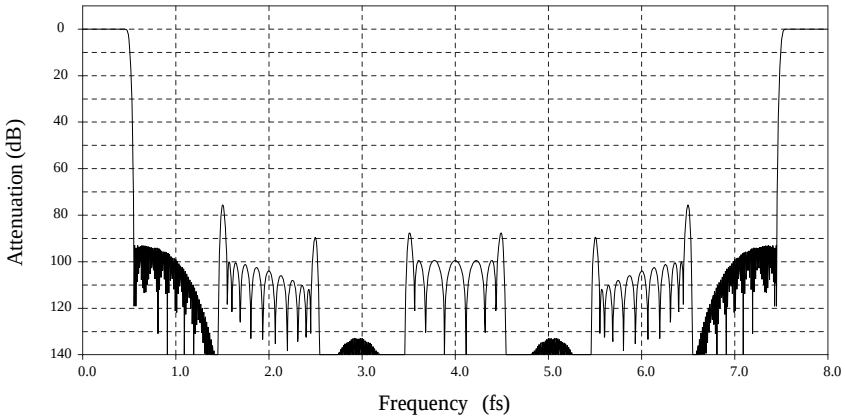
FILTER CHARACTERISTICS

Normal-speed Sampling

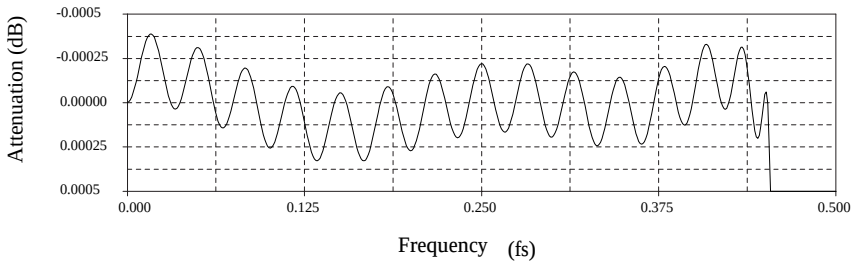
Parameter	Rating
Passband bandwidth	0 to 0.4535fs
Stopband bandwidth	0.5465 to 7.4535fs
Passband ripple	±0.0004 dB
Stopband attenuation	≥ 75 dB
Group delay time[1]	When CKS is HIGH: 63.89/fs (when SYNC is LOW) and 63.51/fs to 64.26/fs (when SYNC is HIGH) When CKS is LOW: 63.76/fs (when SYNC is LOW) and 63.59/fs to 64.14/fs (when SYNC is HIGH)

1. The time difference due to digital filter operation between the end of serial data input (at rate fs) and the start of serial data output (at rate 8fs).

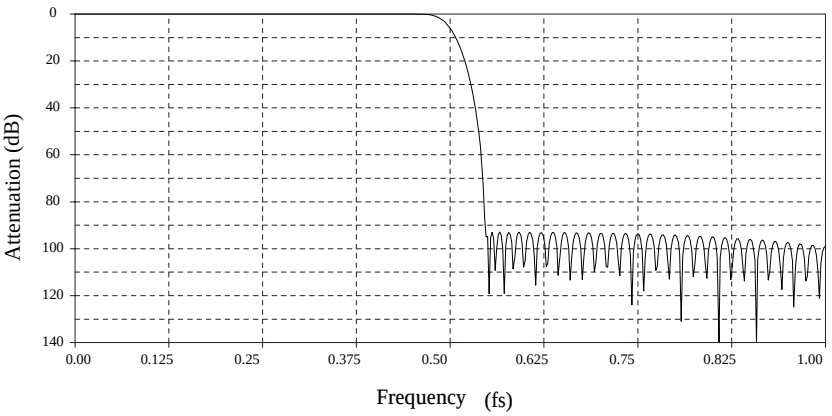
Overall frequency characteristic



Passband frequency characteristic



Transition band characteristic

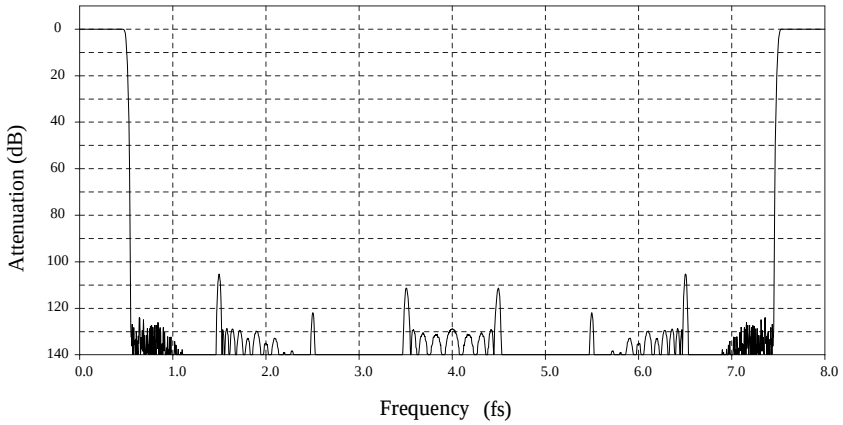


High-speed Sampling (8fs Output)

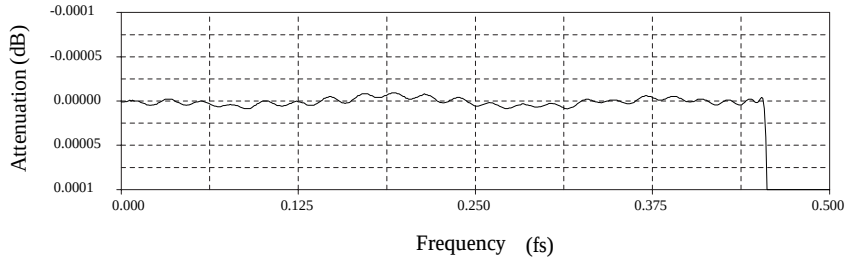
Parameter	Rating
Passband bandwidth	0 to 0.4535fs
Stopband bandwidth	0.5465 to 7.4535fs
Passband ripple	±0.00001 dB
Stopband attenuation	≥ 105 dB
Group delay time[1]	When CKS is HIGH: 51.91/fs (when SYNC is LOW) and 51.53/fs to 52.28/fs (when SYNC is HIGH) When CKS is LOW: 51.78/fs (when SYNC is LOW) and 51.40/fs to 52.15/fs (when SYNC is HIGH)

1. The time difference due to digital filter operation between the end of serial data input (at rate fs) and the start of serial data output (at rate 8fs).

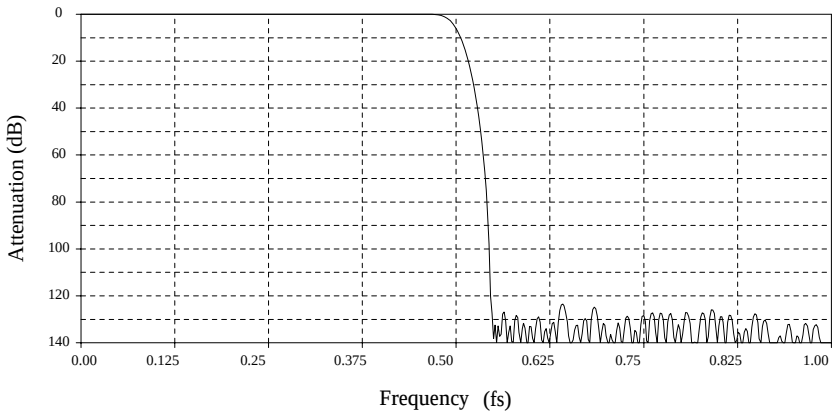
Overall frequency characteristic



Passband frequency characteristic



Transition band characteristic

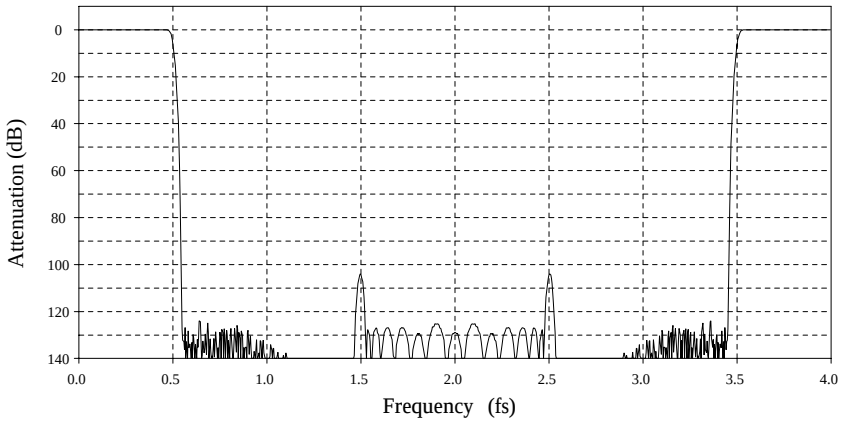


High-speed Sampling (4fs Output)

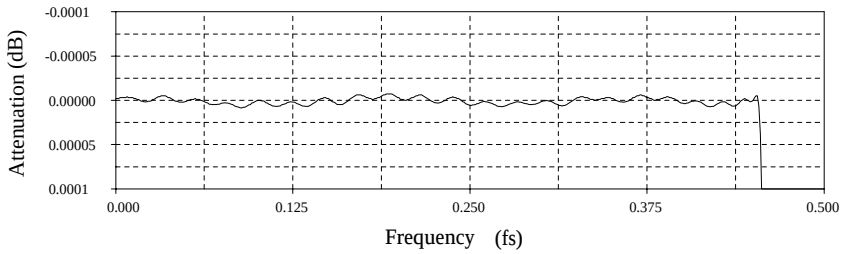
Parameter	Rating
Passband bandwidth	0 to 0.4535fs
Stopband bandwidth	0.5465 to 7.4535fs
Passband ripple	±0.00001 dB
Stopband attenuation	≥ 104 dB
Group delay time[1]	When CKS is HIGH: 50.78/fs (when SYNC is LOW) and 50.40/fs to 51.15/fs (when SYNC is HIGH) When CKS is LOW: 50.77/fs (when SYNC is LOW) and 50.40/fs to 51.15/fs (when SYNC is HIGH)

1. The time difference due to digital filter operation between the end of serial data input (at rate fs) and the start of serial data output (at rate 8fs).

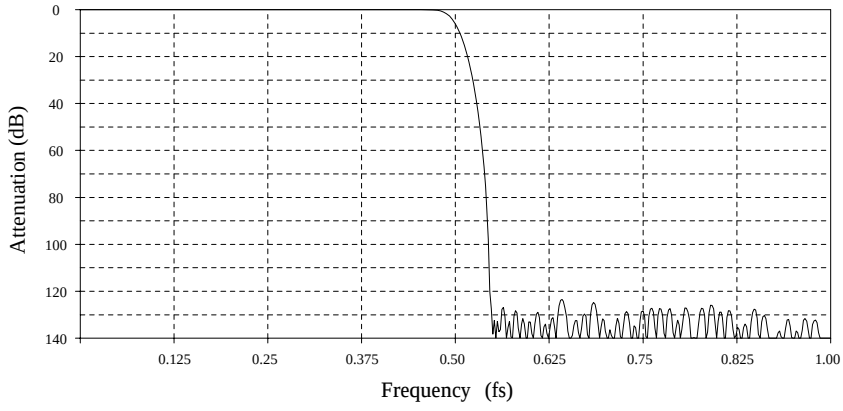
Overall frequency characteristic



Passband frequency characteristic



Transition band characteristic

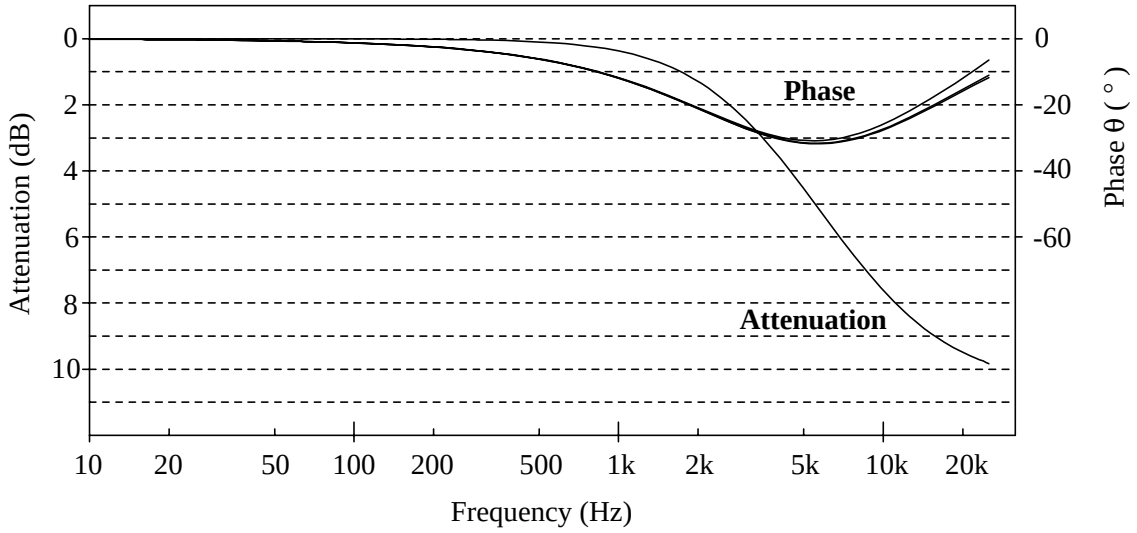


Deemphasis Filter Characteristics (Normal-speed Sampling)

Parameter		Rating		
Sampling frequency (fs)		32 kHz	44.1 kHz	48 kHz
Passband bandwidth		0 to 14.5 kHz	0 to 20.0 kHz	0 to 21.7 kHz
Deviation from ideal characteristics	Attenuation	±0.01 dB		
	Phase	0 to 6°		

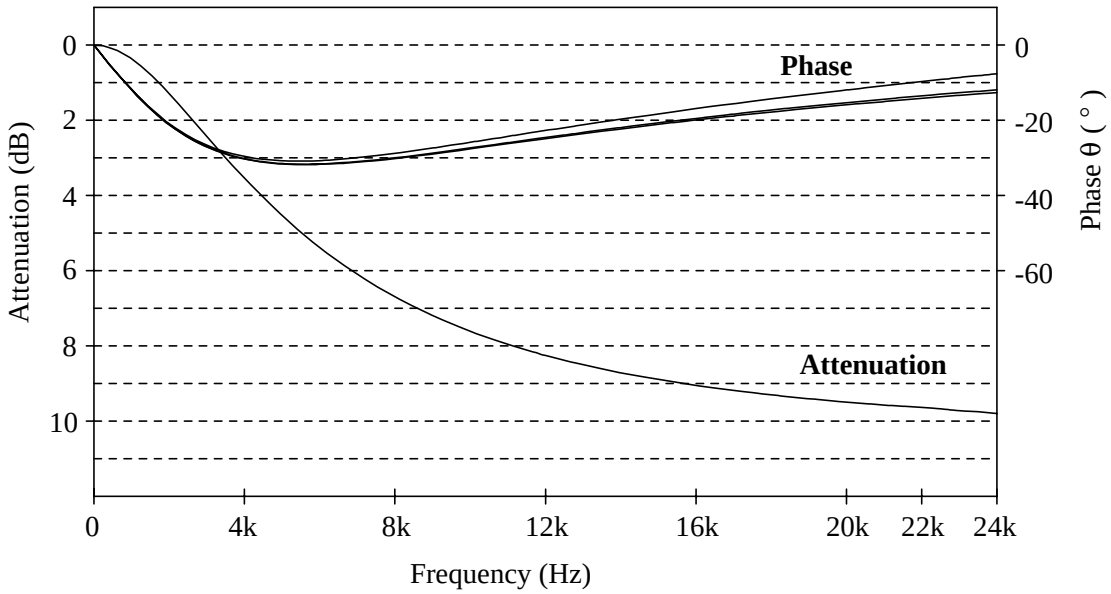
Deemphasis passband characteristic (logarithmic scale)

The phase traces are from top to bottom fs = 32/44.1/48 kHz, respectively.



Deemphasis passband characteristic (linear scale)

The phase traces are from top to bottom fs = 32/44.1/48 kHz, respectively.

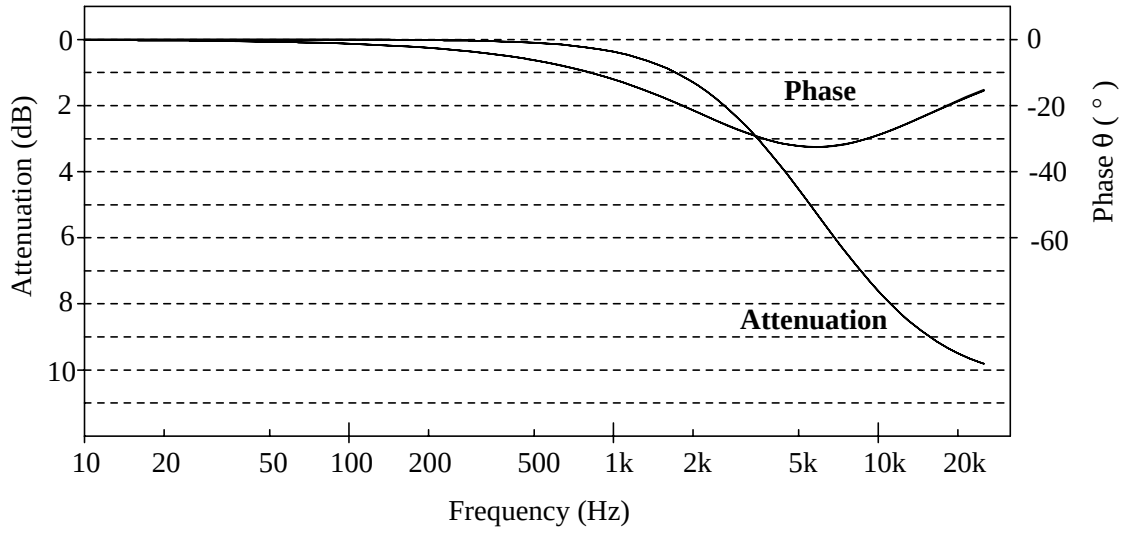


Deemphasis Filter Characteristics (High-speed Sampling)

Parameter		Rating		
Sampling frequency (fs)		64 kHz	88.2 kHz	96 kHz
Passband bandwidth		0 to 29.0 kHz	0 to 40.0 kHz	0 to 43.5 kHz
Deviation from ideal characteristics	Attenuation	±0.001 dB		
	Phase	0 to 1°		

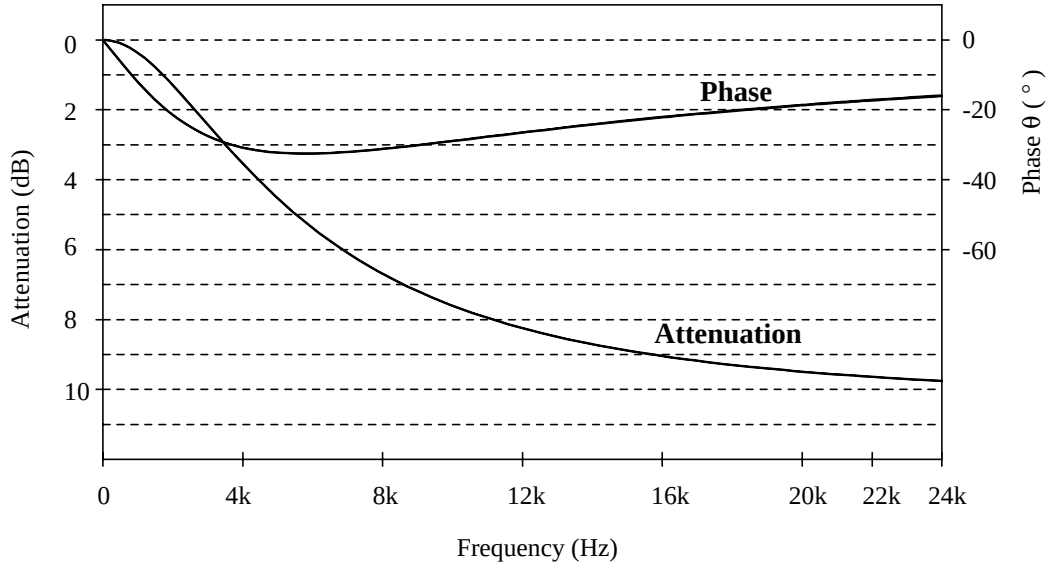
Deemphasis passband characteristic (logarithmic scale)

The phase traces are from top to bottom fs = 64/88.2/96 kHz, respectively.



Deemphasis passband characteristic (linear scale)

The phase traces are from top to bottom fs = 64/88.2/96 kHz, respectively.



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
Input voltage range	V_{IN}	– 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}	–40 to 125	°C
Power dissipation	P_D	750	mW
Soldering temperature	T_{sld}	255	°C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	–20 to 70	°C

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Supply current consumption[1]	I_{DD}		–	110	130	mA
HIGH-level input voltage	V_{IH}	All inputs	0.7V_{DD}	–	–	V
LOW-level input voltage	V_{IL}	All inputs	–	–	0.3V_{DD}	V
XTI AC-coupled input voltage	V_{INAC}		0.3V_{DD}	–	–	V_{p-p}
HIGH-level output voltage	V_{OH}	All outputs, I_{OH} = –1 mA	V_{DD} – 0.4	–	–	V
LOW-level output voltage	V_{OL}	All outputs, I_{OL} = 2 mA	–	–	0.4	V
XTI HIGH-level input current	I_{IH}	V_{IN} = V_{DD}	–	10	20	µA
XTI LOW-level input current	I_{IL}	V_{IN} = V_{SS}	–	10	20	µA
LOW-level input current	I_{IL}	Inputs excluding XTI, V_{IN} = V_{SS}	–	10	20	µA
Input leakage current	I_{LH}	Inputs excluding XTI, V_{IN} = DV_{DD}	–	–	1.0	µA

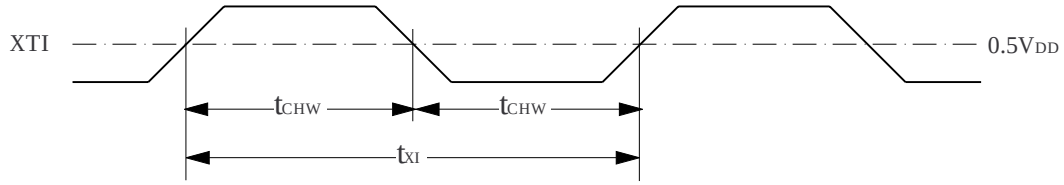
1. V_{DD} = 5.0 V, f_{sys} = 18.432 MHz, 384fs operation, no output load.

AC Characteristics

XTI input timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

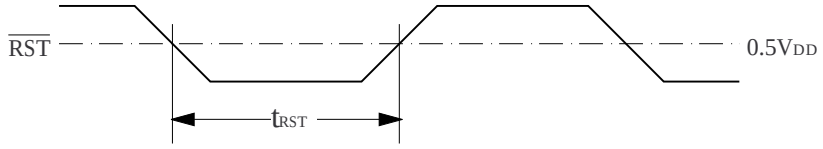
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Oscillator frequency	f_{OSC}		10	–	18.5	MHz
XTI clock pulse cycle time	t_{XI}		54	–	–	ns
XTI HIGH-level clock pulsewidth	t_{CWH}		24	–	–	ns
XTI LOW-level clock pulsewidth	t_{CWL}		24	–	–	ns



$\overline{\text{RST}}$ input timing

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

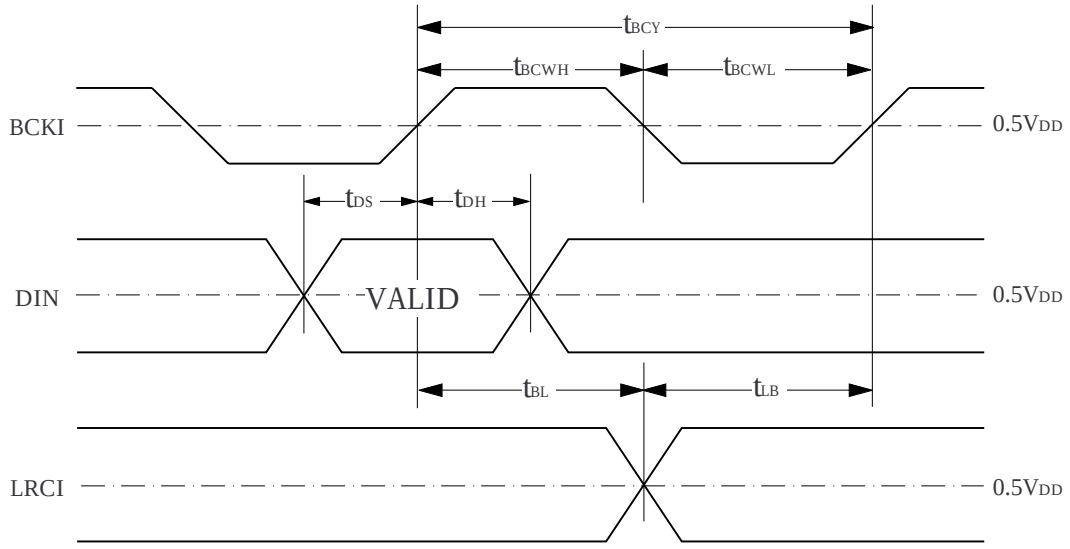
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Reset pulsewidth	t_{RST}	When power is applied	1	–	–	µs
		At all other times	50	–	–	ns



Serial data input timing (BCKI, DIN, LRCI)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

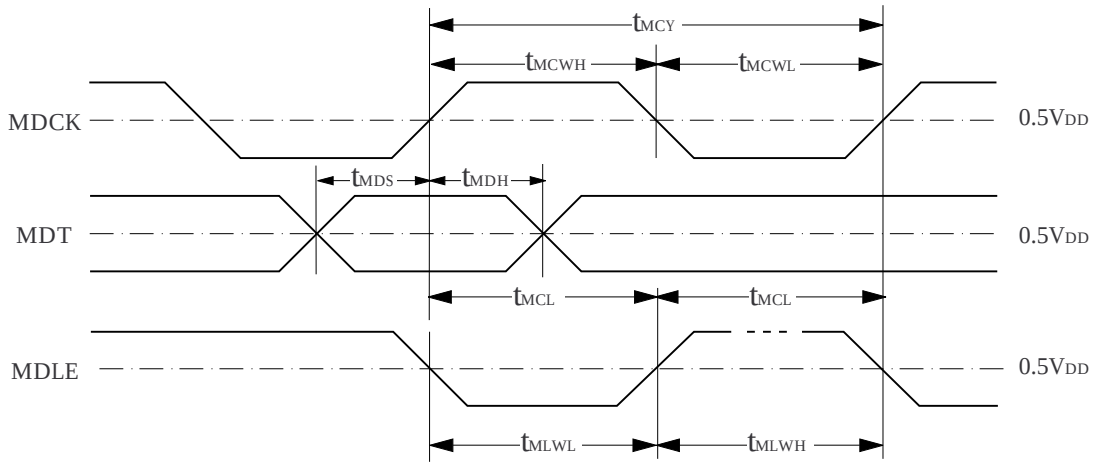
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
BCKI pulse cycle time	t_{BCY}		100	–	–	ns
BCKI HIGH-level pulsewidth	t_{BCWH}		50	–	–	ns
BCKI LOW-level pulsewidth	t_{BCWL}		50	–	–	ns
DIN setup time	t_{DS}		20	–	–	ns
DIN hold time	t_{DH}		20	–	–	ns
BCKI rising edge to LRCI edge time	t_{BL}		50	–	–	ns
LRCI edge to BCKI rising edge time	t_{LB}		50	–	–	ns



Microprocessor serial interface timing (MDCK, MDT, MDLE)

V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
MDCK pulse cycle time	t_{MCY}		100	–	–	ns
MDCK HIGH-level pulsewidth	t_{MCWH}		50	–	–	ns
MDCK LOW-level pulsewidth	t_{MCWL}		50	–	–	ns
MDT setup time	t_{MDS}		20	–	–	ns
MDT hold time	t_{MDH}		20	–	–	ns
MDCK rising edge to MDLE edge time	t_{MCL}		50	–	–	ns
MDLE edge to MDCK rising edge time	t_{MLC}		50	–	–	ns
MDLE HIGH-level pulsewidth	t_{MLWH}		20	–	–	ns
MDLE LOW-level pulsewidth	t_{MLWL}		20	–	–	ns

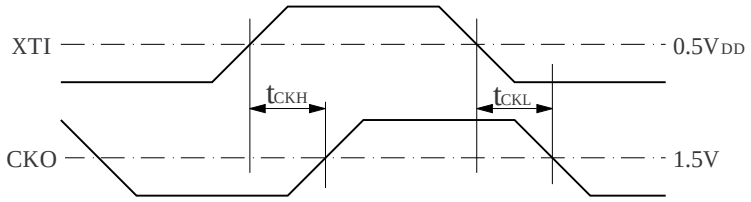


Output signal timing (CKO, BCKO, DOR, DOL, WCKO)

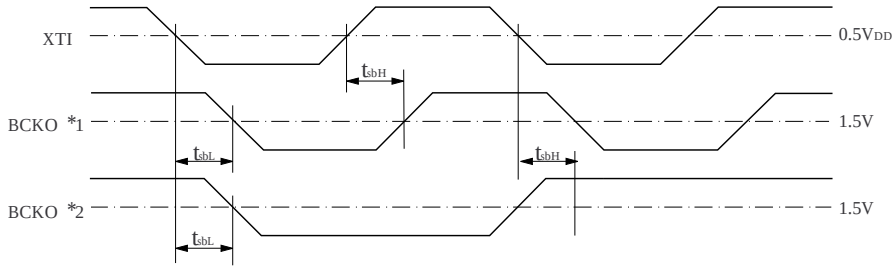
V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 70 °C, C_L = 15 pF

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
XTI to CKO propagation delay time	t_{CKH}		–	17	35	ns
	t_{CKL}		–	17	35	
XTI to BCKO propagation delay time	t_{sbH}	Normal and high-speed mode 4fs output	–	20	60	ns
	t_{sbL}		–	20	60	
	t_{sbH}	High-speed mode 8fs output	–	20	60	
	t_{sbL}		–	20	60	
BCKO to DOR propagation delay time	t_{bdH}		–5	–	15	ns
	t_{bdL}		–5	–	15	
BCKO to DOL propagation delay time	t_{bdH}		–5	–	15	ns
	t_{bdL}		–5	–	15	
BCKO to WCKO propagation delay time	t_{bdH}		–5	–	15	ns
	t_{bdL}		–5	–	15	

CKO output

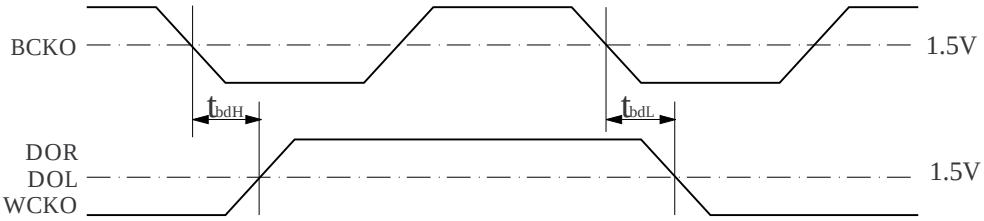


BCKO output



*1 : High speed mode 8fs output
*2 : Normal and high-speed mode 8fs output

DOR, DOL, WCKO output

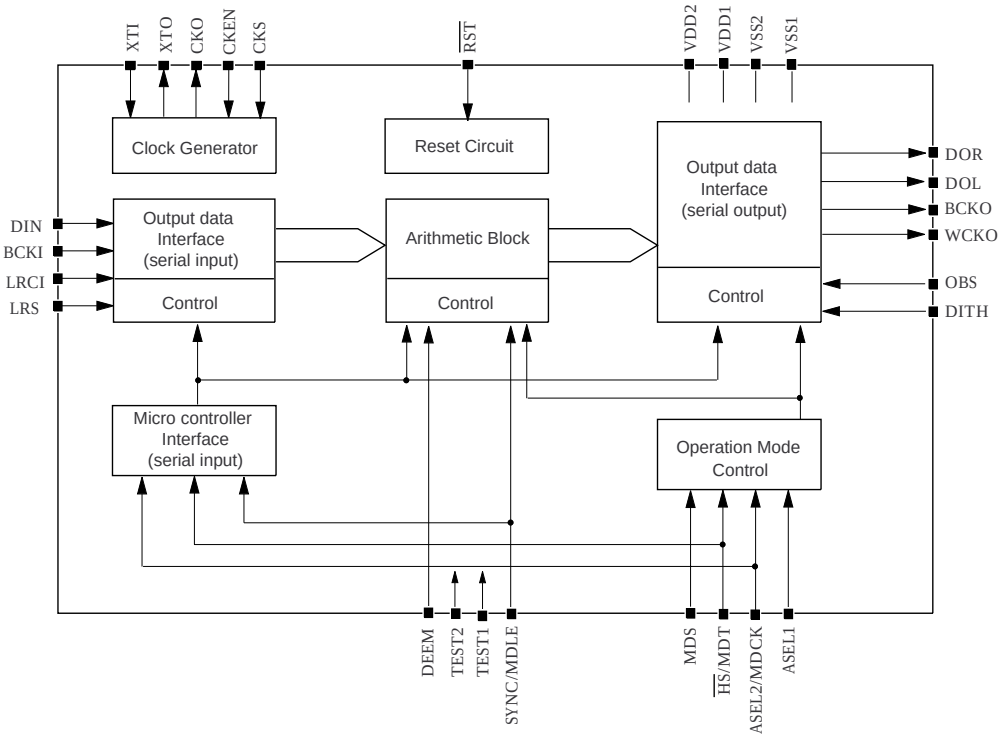


PIN DESCRIPTION

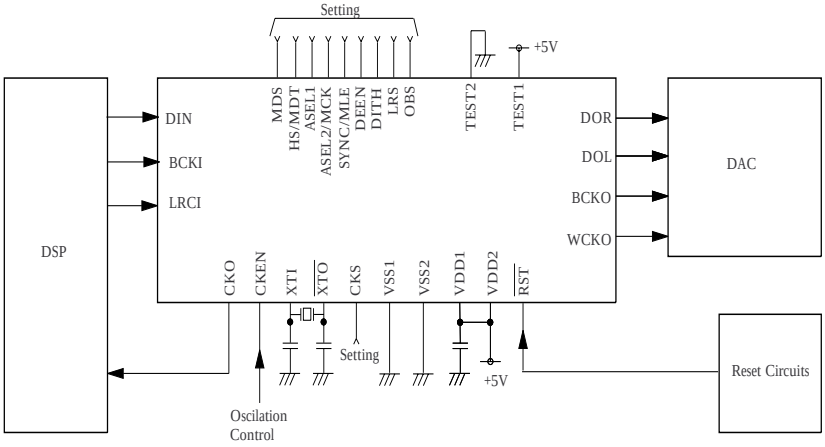
Number	Name	I/O[1]	Description
1	DIN	Ip	Data input
2	BCKI	Ip	Bit clock input
3	VDD1	–	5 V supply voltage
4	DITH	Ip	Dither ON/OFF control
5	CKEN	Ip	Crystal oscillator operation enable
6	XTI	I	Crystal oscillator input/external clock input
7	XTO	O	Crystal oscillator output
8	VSS1	–	Ground
9	CKO	O	Master clock output
10	CKS	Ip	Master clock input frequency select
11	ASEL2/MDCK	Ip	Operating mode select/microprocessor interface clock input
12	$\overline{HS}$/MDT	Ip	Operating mode select/microprocessor interface data input
13	SYNC/MDLE	Ip	Sync mode select/microprocessor interface latch enable input
14	$\overline{RST}$	Ip	Reset input
15	LRS	Ip	LR clock polarity select
16	DEEM	Ip	Deemphasis ON/OFF select
17	TEST1	Ip	Test pin 1. Tie HIGH or leave open for normal operation.
18	TEST2	Ip	Test pin 2. Tie LOW for normal operation.
19	OBS	Ip	Output data length select
20	ASEL1	Ip	Operating mode select
21	VSS2	–	Ground
22	VDD2	–	5 V supply voltage
23	DOR	O	Right-channel data output
24	DOL	O	Left-channel data output
25	WCKO	O	Word clock output
26	BCKO	O	Output data bit clock output
27	MDS	Ip	Mode set method select
28	LRCI	Ip	LR clock input

1. Ip = input pin with pull-up resistor, I = input, O = output

BLOCK DIAGRAM



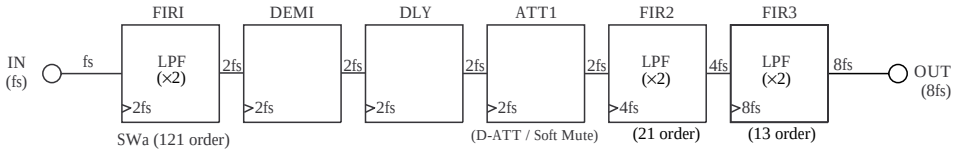
SYSTEM CONFIGURATION



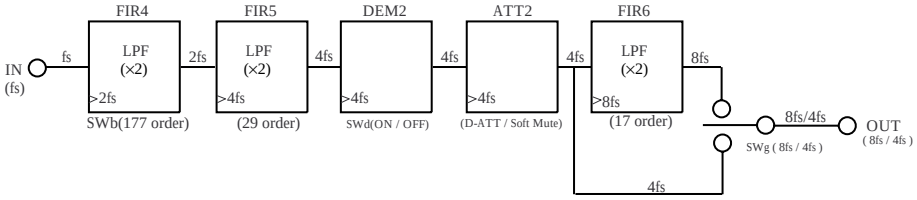
DATA FLOW

ATT1/ATT2 soft muting uses the D-ATT function to set the gain to −∞.

Normal-speed sampling (fs = 32/44.1/48 kHz)



High-speed sampling (fs = 64/88.2/96 kHz)



FUNCTIONAL DESCRIPTION

Mode Switching and Function Switching

The SM5846AP supports several operating modes and function switches. Internal control flags, set by the digital inputs or serial data input signal from a microprocessor, determine the status of those function switches.

Mode switching/function switch controls

Stage	Name	Control request		Function
		Input	Control flag	
System	MDS	Yes		IC control request switch (input pin/control flag)
Operating mode switch	$\overline{HS}$	Yes	Yes	Operating mode switching
	ASEL2	Yes	Yes	
	ASEL1	Yes	Yes	
Clock switch	CKS	Yes		Input clock frequency switching
	CKEN	Yes		Crystal oscillator operating control switching
Filter switch	DEEM	Yes	Yes	Deemphasis ON/OFF switching
	FSEL2		Yes	Deemphasis filter sampling frequency set
	FSEL1		Yes	
	$\overline{MUTE}$		Yes	Mute ON/OFF control
	DITH	Yes (pos. logic)	Yes (neg. logic)	Dither ON/OFF control
Input interface switch	SYNC	Yes	Yes	Jitter-free/sync mode switching
	LRS	Yes		LRCI (LR clock) input polarity switching
	IBS2		Yes	Input data length set
	IBS1		Yes	
Output interface switch	OBS	Yes	Yes	Output data length set

Control request switching

MDS input and device control

Mode switching/function switching is performed under input pin control when MDS is HIGH, and under internal flag control when MDS is LOW.

MDS[1]	Control request
HIGH	Input pins
LOW	Control flags

1. Switching MDS during device operation is prohibited.

Input pin functions when MDS is LOW

All pins that are part of the microprocessor interface can be used whenever MDS is LOW.

Pin name	Function	Notes
$\overline{HS}$/MDT	Serial data transfer data clock	Used for the microprocessor interface
ASEL2/MDCK	Serial data transfer clock input	
SYNC/MDLE	Serial data transfer latch enable input	
CKS	CKS function switch input	Input pin control only because there is no corresponding control flag.
CKEN	CKEN function switch input	
LRS	LRS function switch input	

Control flag functions when MSD is HIGH (default)

Other requests are controlled by internal flag only because there is no corresponding input pin. These control flags are valid when MDS is HIGH. The default values are shown in the following table.

Flag name	Default value	Default setting
FSEL2	HIGH	44.1 kHz deemphasis filter sampling frequency
FSEL1	HIGH	
$\overline{\text{MUTE}}$	HIGH	Muting OFF
IBS2	LOW	16-bit input data length
IBS1	HIGH	

Clock Functions

Input clock frequency switching (CKS)

This switch is used to select the input clock frequency—384fs or 512fs (normal-speed sampling), and 192fs or 256fs (high-speed sampling).

CKS	Input sampling frequency fs (kHz)	System clock		Notes
		Frequency (MHz)	(× fs)	
LOW	32	16.384	512fs	Normal-speed sampling mode
	64	16.384	256fs	High-speed sampling mode
HIGH	32	12.288	384fs	Normal-speed sampling mode
	44.1	16.9344		
	48	18.432		
	64	12.288	192fs	High-speed sampling mode
	88.2	16.9344		
	96	18.432		

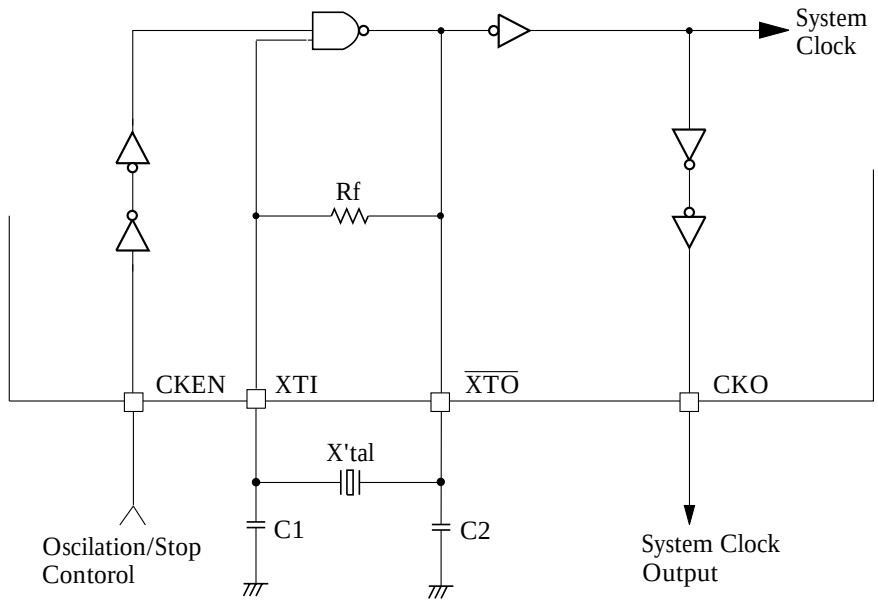
Crystal oscillator control switch (CKEN)

This switch is used to start/stop the crystal oscillator circuit.

CKEN	Crystal oscillator operation
HIGH	Oscillating
LOW	Stopped

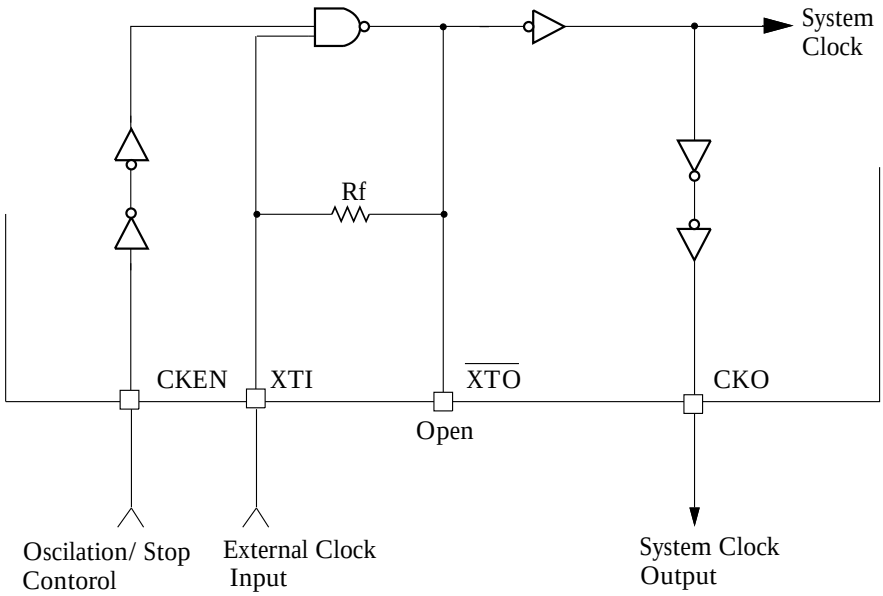
Crystal oscillator circuit

The built-in crystal oscillator circuit comprises a feedback resistor and several logic gates. The system clock can be generated using an external quartz crystal and 2 capacitors.



External clock

When an external clock is used, XTO is left open-circuit and the clock signal is input on XTI.



Other control settings

Input data length select

ISB1 and ISB2 flags are used to set the input data length.

IBS2	IBS1	Input data length	Notes
HIGH	HIGH	20 bits	The length is set to the default value of 16 bits (IBS2 = LOW and IBS1 = HIGH) after a reset.
HIGH	LOW	24 bits	
LOW	HIGH	16 bits	
LOW	LOW	32 bits	

LRCI input polarity select

Pin LRS is used to set the LRCI input polarity.

LRS	LRCI	Input channel
HIGH	HIGH	Left
HIGH	LOW	Right
LOW	HIGH	Right
LOW	LOW	Left

Sync mode select

The SYNC pin or flag setting can be used to select either jitter-free mode or sync mode to control synchronization between input data and internal arithmetic blocks.

SYNC	Mode	Notes
HIGH	Jitter-free mode	The SYNC flag is set HIGH (default) after a reset.
LOW	Sync mode	

Filter Stage

Operating mode

The SM5846A supports 3 different operating modes to control output data rate switching. The operating mode is selected by the state of $\overline{HS}$, ASEL1 and ASEL2.

$\overline{HS}$	ASEL1	ASEL2	Operating mode[1]	
			Speed	Oversampling
HIGH	LOW	HIGH	Normal-speed sampling	8-times
LOW	HIGH	HIGH	High-speed sampling	8-times
		LOW		4-times

1. Only the above 3 modes are valid.

Operating speed and sampling frequency

The SM5846AP supports sampling frequencies of 32/44.1/48 kHz (normal-speed sampling mode) and 64/88.2/96 kHz (high-speed sampling mode).

Operating speed	Input sampling frequency
Normal-speed sampling	32/44.1/48 kHz
High-speed sampling	64/88.2/96 kHz

Deemphasis filter

The SM5846AP contains a digital deemphasis filter controlled by DEEM.

DEEM	Deemphasis
HIGH	ON
LOW	OFF

The sampling frequency is selected by FSEL1 and FSEL2.

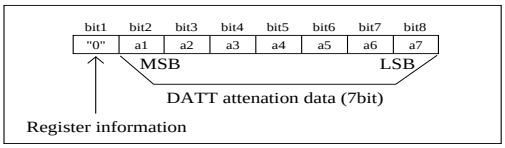
FSEL2	FSEL1	Sampling frequency fs (kHz)	
		Normal-speed sampling	High-speed sampling
HIGH	HIGH	44.1	88.2
HIGH	LOW	48	96
LOW	HIGH	44.1	88.2
LOW	LOW	32	64

Digital attenuator

The digital attenuator is controlled by serial data from the microprocessor interface. This data can set attenuation and muting. Note that the digital attenuator is only enabled when MDS is LOW. ATT1 and ATT2 are used to set the attenuation in normal-speed sampling and high-speed sampling, respectively.

Attenuation setting

The data stored in the D-ATT attenuation register, accessed through the microprocessor interface, determines the attenuation setting of the digital attenuator. The D-ATT register data format is shown below.



The attenuation setting is given by the following equations.

$$Attenuation = 0 \text{ [dB]} \qquad (\text{DATT} = 0)$$

$$Attenuation = 20\log_{10}\left(\frac{127 - DATT}{128}\right) \text{[dB]} \qquad (0 < \text{DATT} < 127)$$

$$Attenuation = -\infty \qquad (\text{DATT} = 127)$$

The attenuation for a selection of values is given in the following table.

DATT register value	Microprocessor or command (hex)	Attenuation (dB)	Relative gain
0	00H	0	× 1.0
1	01H	–0.137	× 0.984375
2	02H	–0.206	× 0.9765625
↓	↓	↓	↓
63	3FH	–6.021	× 0.5
64	40H	–6.157	× 0.4921875
↓	↓	↓	↓
125	7DH	–36.12	× 0.015625
126	7EH	–42.14	× 0.0078125
127	7FH	–∞	× 0

Digital attenuator operation

The attenuation register is reset to 0 (attenuation = 0 dB) after a system reset signal.

When data is written to the attenuation register, through the microprocessor interface, the attenuation changes from the current value to the new value at the speed shown in the following table.

Operating speed	Speed of attenuation change	Time from min. to max. attenuation
Normal-speed sampling	8/fs per step change	1016/fs (23.0 ms at 44.1 kHz)
High-speed sampling	16/fs per step change	2032/fs (23.0 ms at 88.2 kHz)

Soft muting operation

Soft muting ON/OFF is controlled by the $\overline{\text{MUTE}}$ flag, accessed through the microprocessor interface.

$\overline{\text{MUTE}}$	Muting	Notes
HIGH	OFF	The $\overline{\text{MUTE}}$ flag is set HIGH (default) after a system reset.
LOW	ON	

When muting is ON, the attenuation ramps down to –∞ at the speed shown in the table. Similarly when muting is OFF, the attenuation level returns to the original value at the same speed.

If the contents of the DATT attenuation register are changed while muting is ON (attenuation = –∞), only the register contents are replaced. If muting is subsequently turned OFF, the attenuation value changes to the new value at the same speed as shown in the table.

Output data round-off

Output data round-off processing is required because the internal data length of the digital filter is different from the output data length (internal data processing width > output data width).

The SM5846AP can select either normal round-off or dither round-off on the output data. Round-off processing can be selected either by input pin or control flag settings.

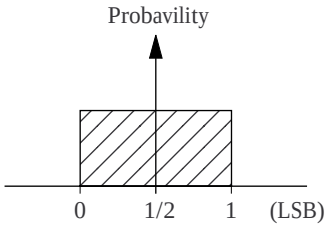
MDS	$\overline{\text{DITH}}$ pin	$\overline{\text{DITH}}$ flag	Output data round-off	Notes
HIGH	HIGH	×	Dither round-off	The $\overline{\text{DITH}}$ flag is set HIGH (default) after a system reset.
	LOW		Normal round-off	
LOW	×	HIGH	Normal round-off	
		LOW	Dither round-off	

Normal round-off

Normal round-off is carried out by adding 1/2 LSB to the filter output data to form 20/24-bit output data, depending on the selected output data length.

Dither round-off

Dither round-off is carried out by adding a pseudo-random number between 0 and 1 LSB, derived from a rectangular distribution, to the filter output data to form 20/24-bit output data, depending on the selected output data length. The random number rectangular distribution is shown below (average = 1/2 LSB).



Overflow limiter

If an overflow or underflow condition occurs after round-off or filter arithmetic processing, the output data will be fixed at positive or negative maximum value.

Audio Data Input Interface

Serial data transmission is used for the digital audio data input.

The data has the following format:

- 16/20/24/32-bit data length
- Alternating left/right-channel serial data transmission
- MSB first
- Rear packed
- 2s complement for negative values

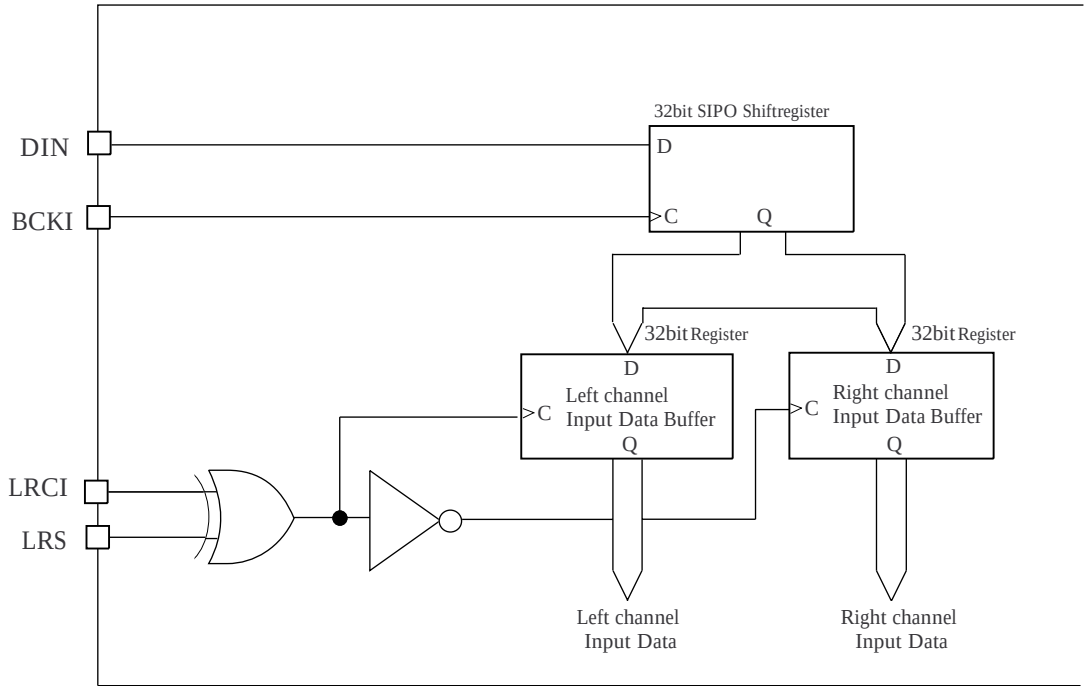
Audio data input interface pins

Audio data is input using pins LRCI, BCKI, and DIN. The LRCI input polarity is determined by pin LRS.

Pin name	Function
LRCI	Left/right-channel latch clock input
BCKI	Bit transfer clock input
DIN	Serial data input
LRS	LRCI input polarity switch

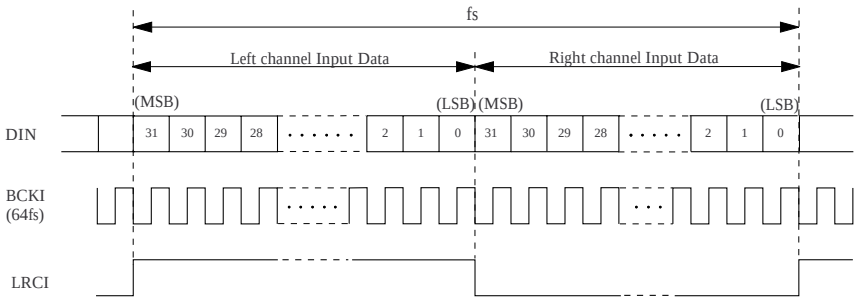
Serial data on DIN is input to the serial-to-parallel shift register on the falling edge of the bit transfer clock BCKI. The parallel data is then stored in the left/right-channel input buffers on the HIGH/LOW-level pulse of the LRCI latch clock signal, depending on the selected polarity of the LRCI clock.

Audio data input interface schematic

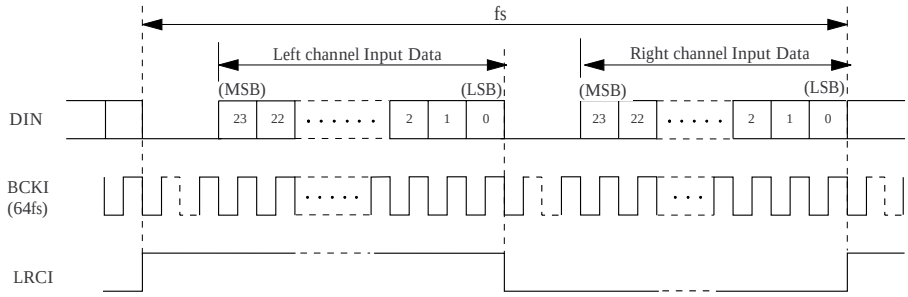


Input data interface example (LRS = HIGH)

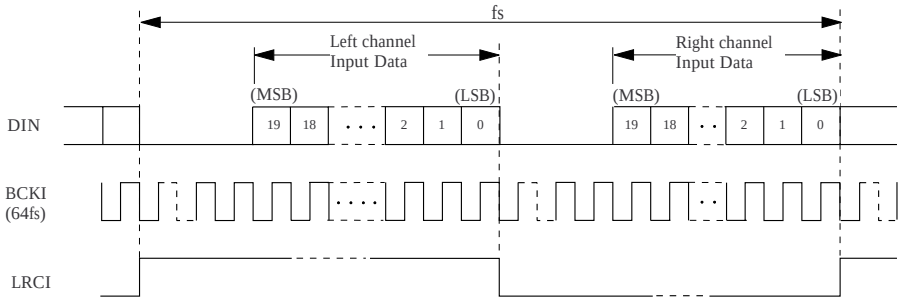
32-bit input data length



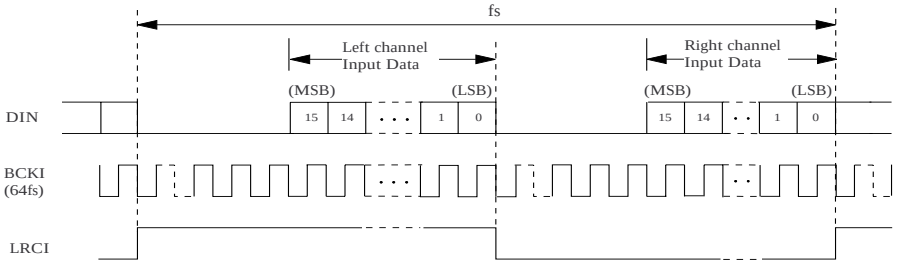
24-bit input data length



20-bit input data length

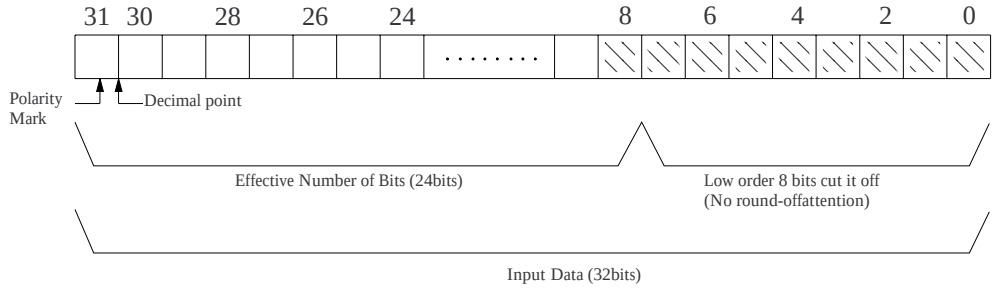


16-bit input data length

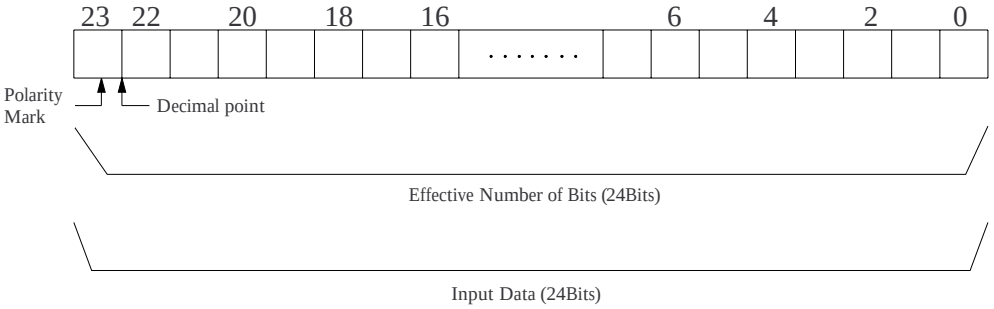


Input data validity

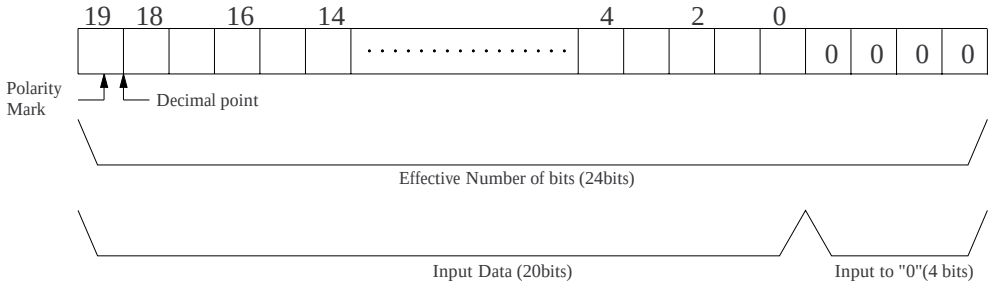
32-bit input data length



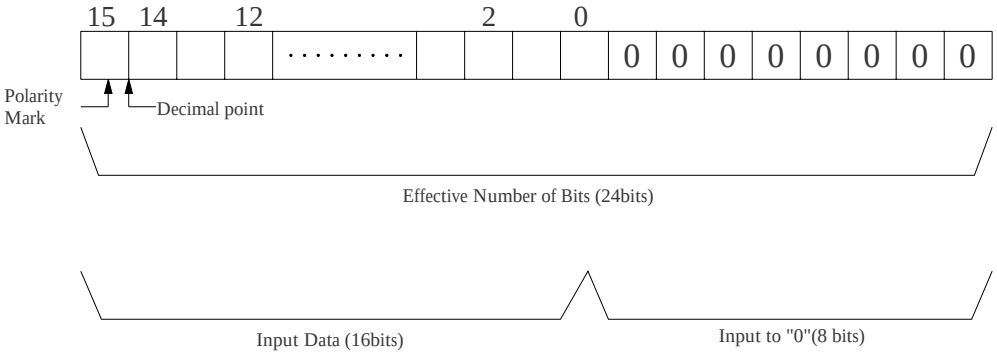
24-bit input data length



20-bit input data length



16-bit input data length



Audio Data Output Interface

Serial data transmission is used for the digital audio data output.

The data has the following format:

- 20/24-bit data length
- Simultaneous left/right-channel serial data transmission
- MSB first
- Bit transfer clock burst (NPC format)
- 2s complement for negative values

Audio data output interface pins

Audio data is output using pins WCKO, BCKO, DOL and DIN.

Pin name	Function
WCKO	Word clock output
BCKO	Bit transfer clock output
DOL	Left-channel serial data output
DOR	Right-channel serial data output

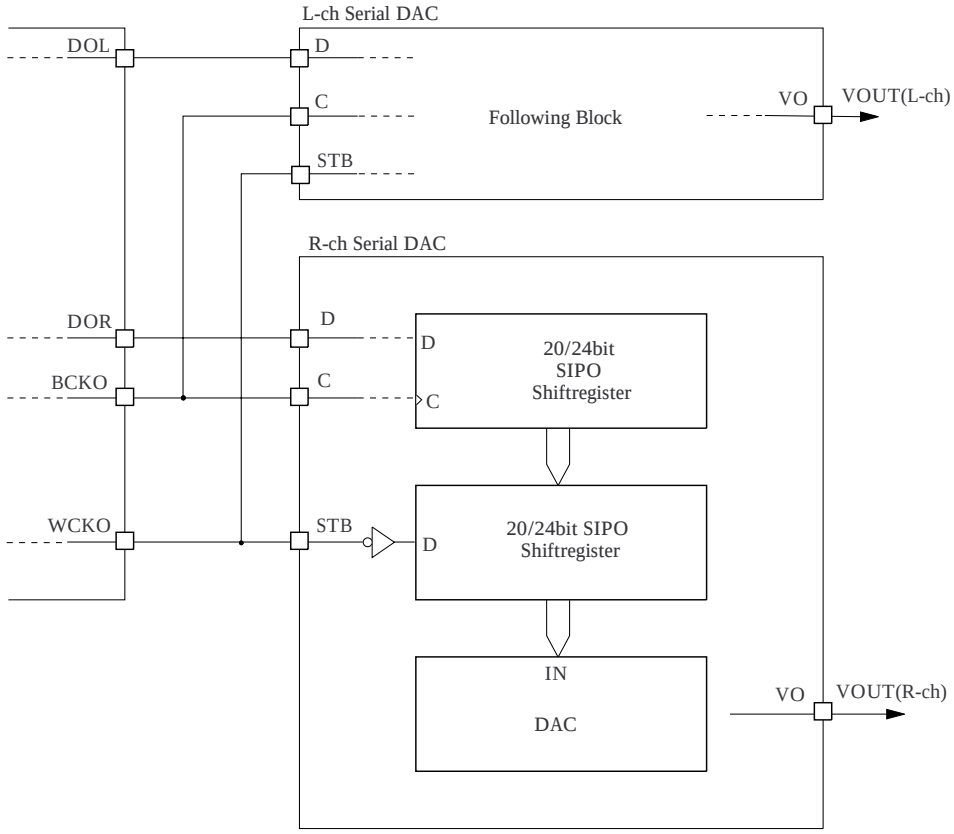
Serial data is output on DOL and DOR on the falling edge of the bit transfer clock BCKO. Generally, external circuits, such as a serial D/A converter, sample the serial data output on DOL and DOR on the rising edge of the bit transfer clock signal, and then shift the data into a register. At the completion of one data cycle (20/24-bit selectable) transfer, the word clock WCKO goes LOW with a 50% duty ratio. Then the external circuit writes parallel data to a buffer register on the falling edge of word clock WCKO.

Output data length select

The output data length is set by either the OBS pin or flag.

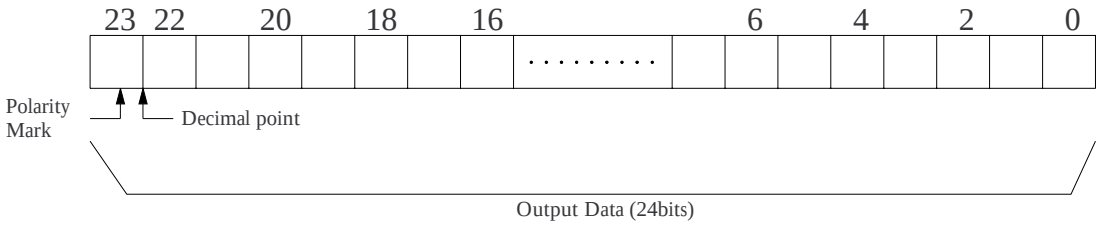
OBS	Output data length	Notes
HIGH	24 bits	The OBS flag is set LOW (default) after a system reset.
LOW	20 bits	

Audio data output interface

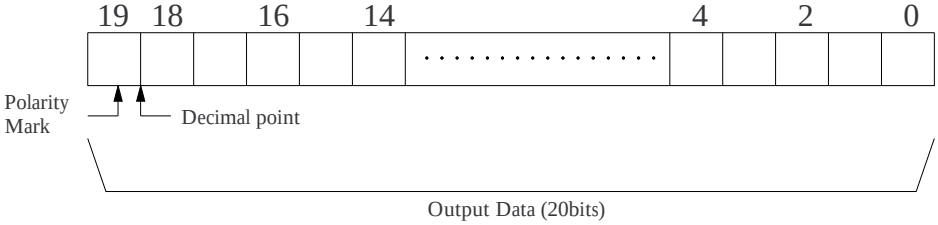


output data format

24-bit output data length

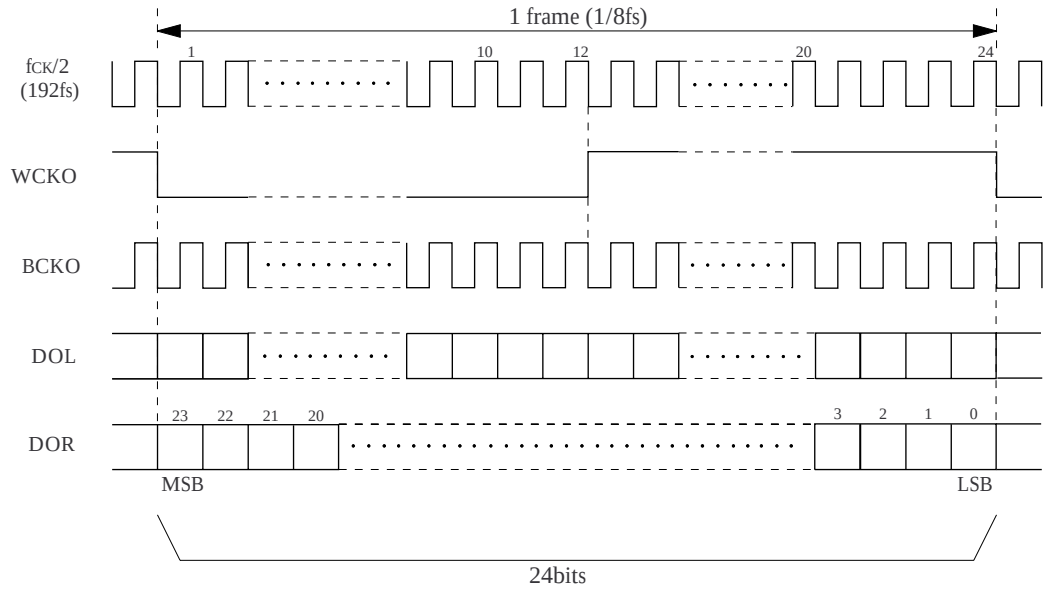


20-bit output data length

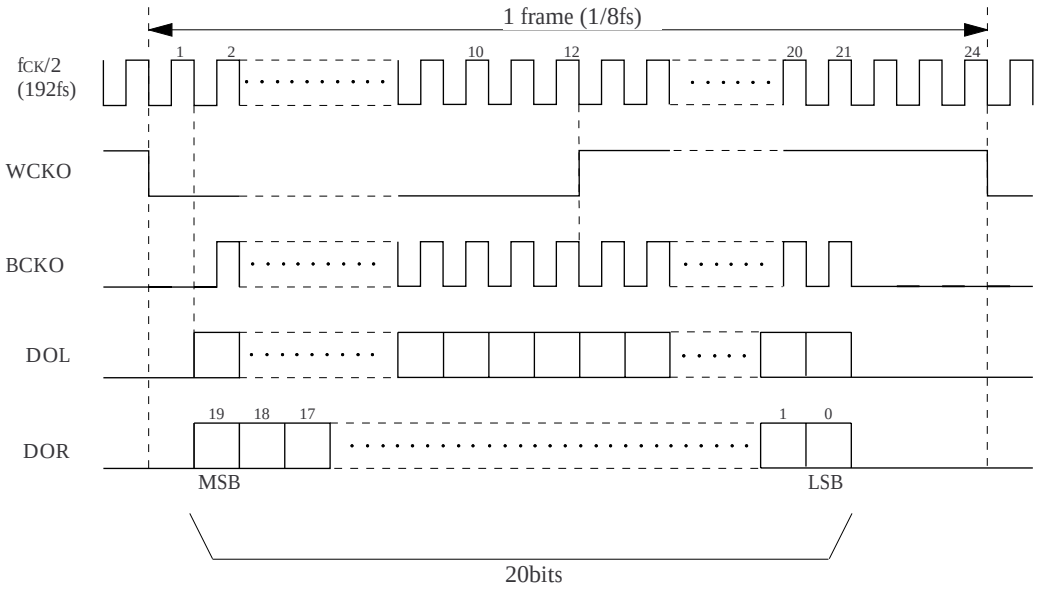


Audio data output timing

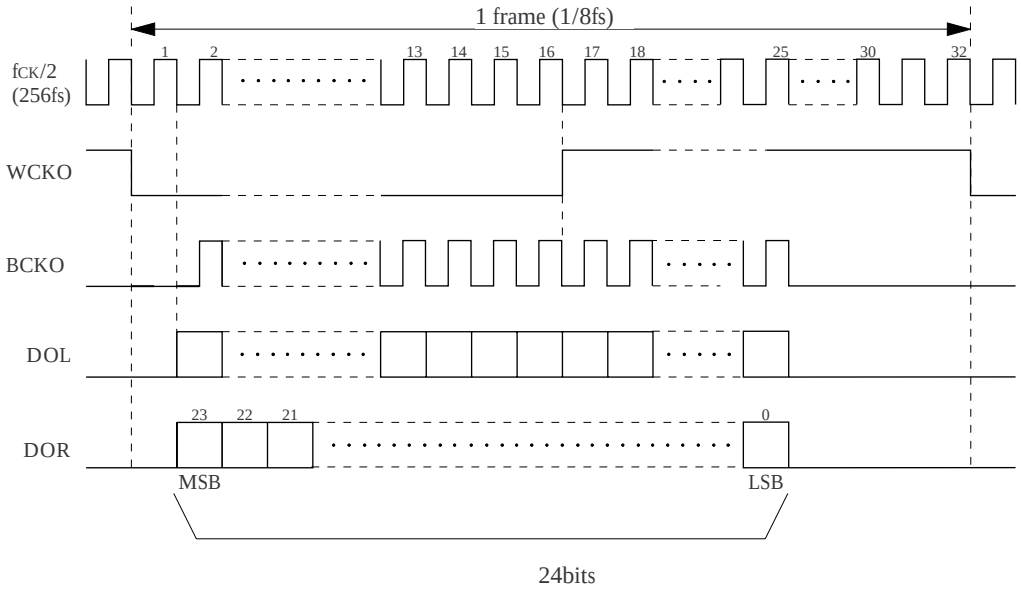
Normal-speed sampling: 384fs clock, 24-bit data output, 8fs output data rate



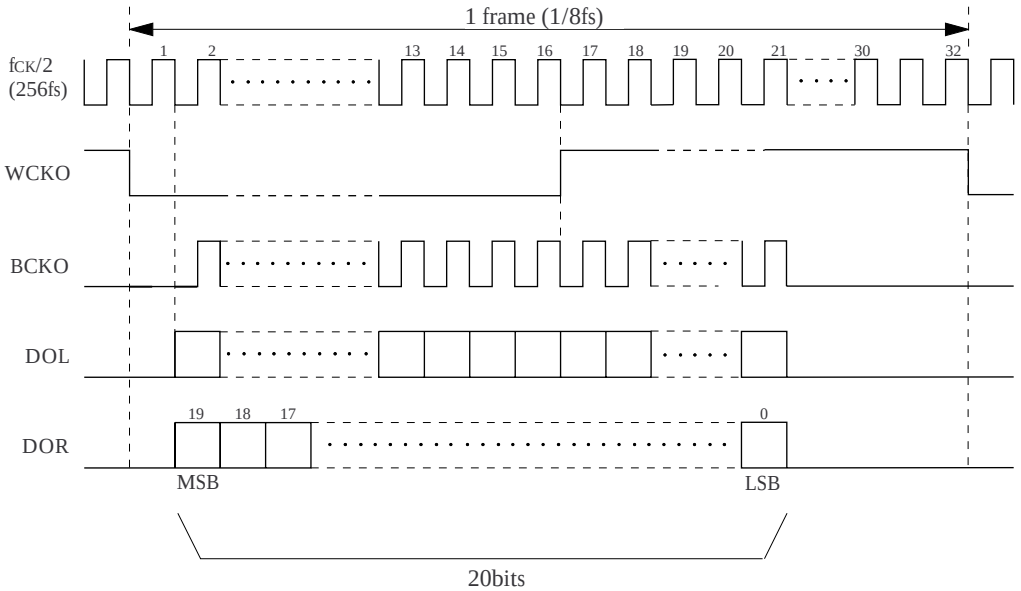
Normal-speed sampling: 384fs clock, 20-bit data output, 8fs output data rate



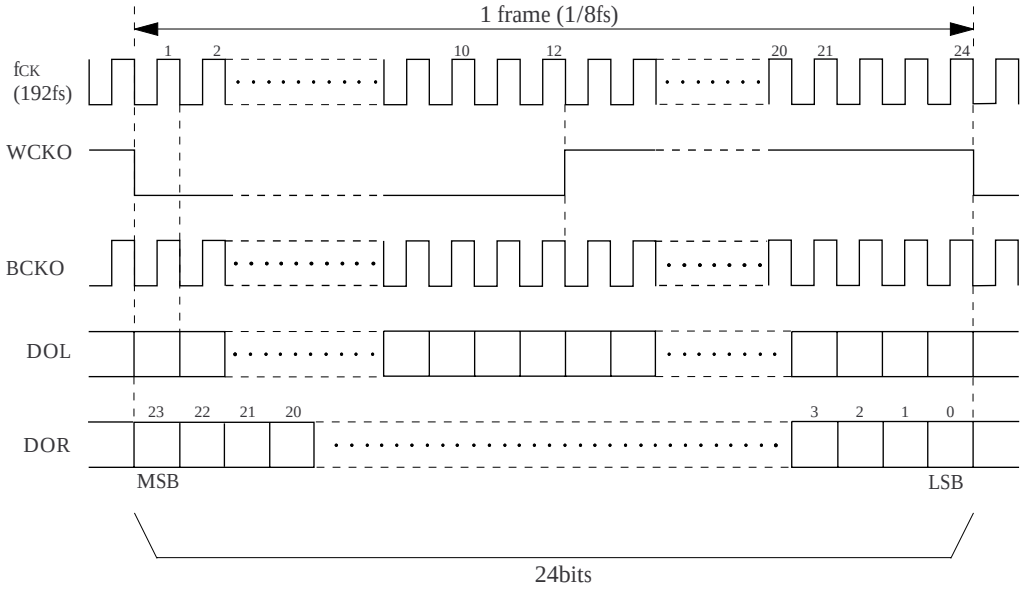
Normal-speed sampling: 512fs clock, 24-bit data output, 8fs output data rate



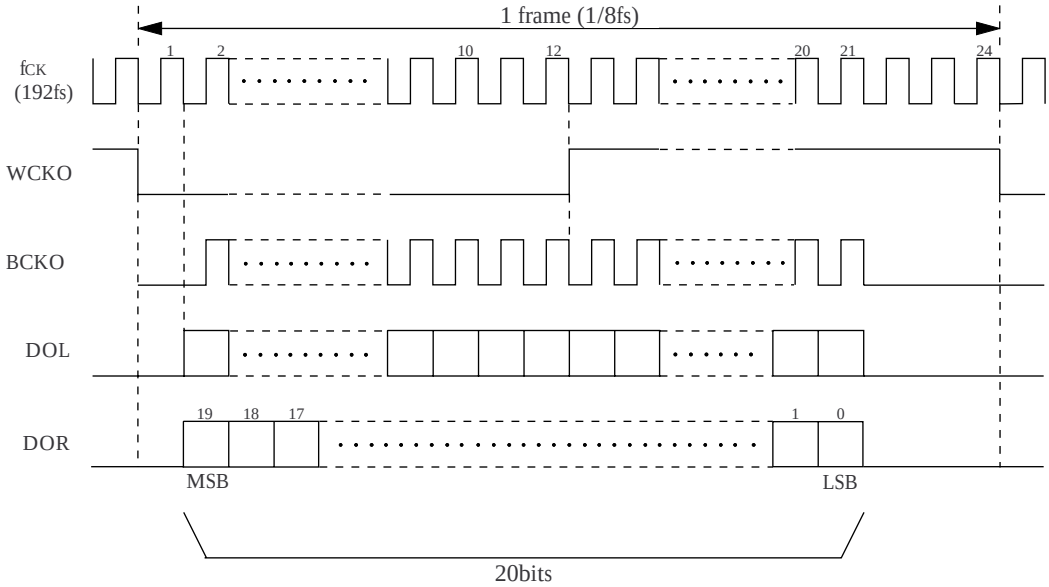
Normal-speed sampling: 512fs clock, 20-bit data output, 8fs output data rate



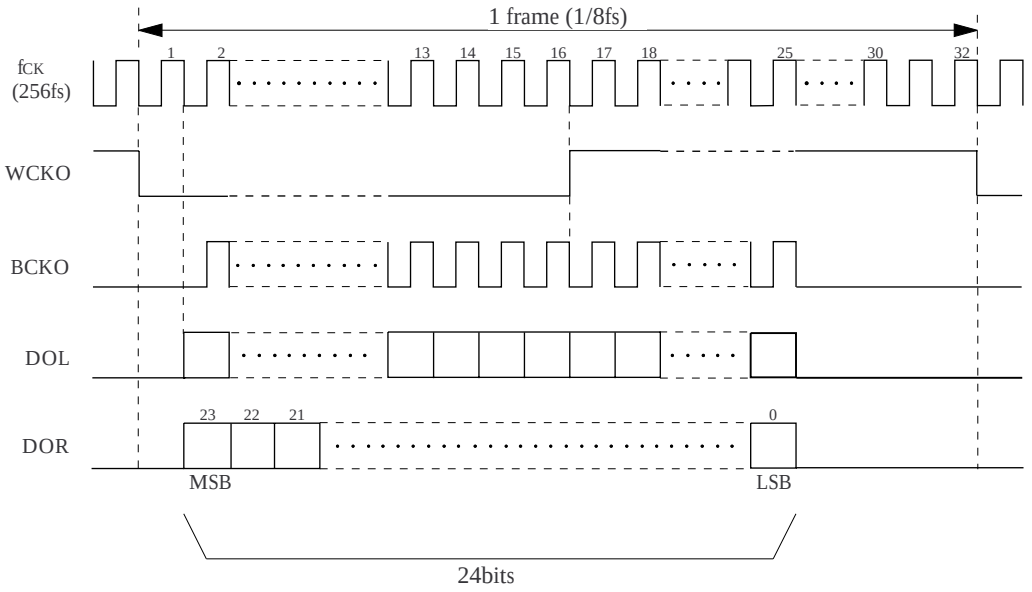
High-speed sampling: 192fs clock, 24-bit data output, 8fs output data rate



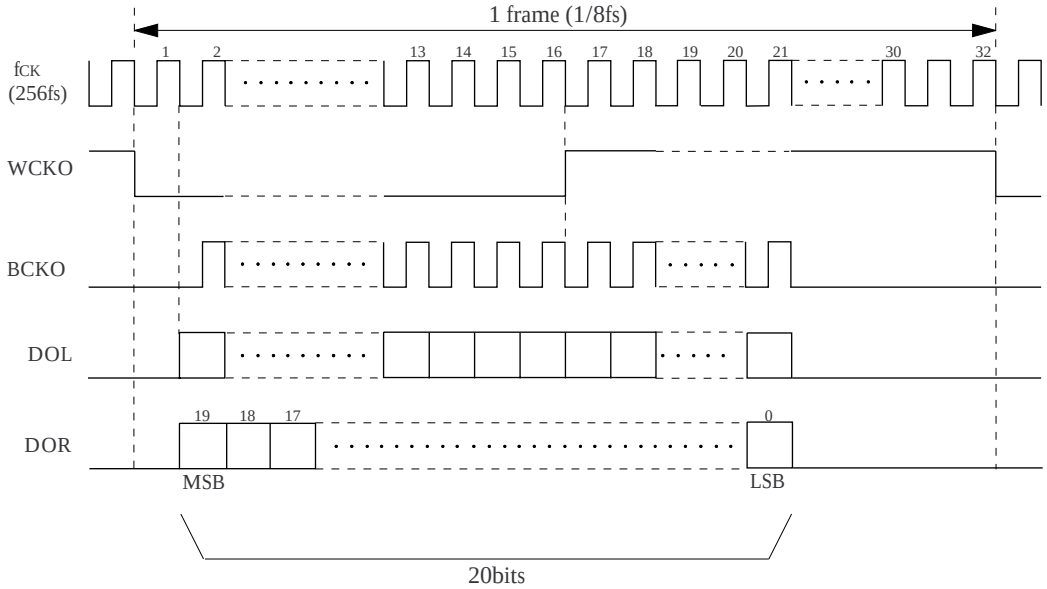
High-speed sampling: 192fs clock, 20-bit data output, 8fs output data rate



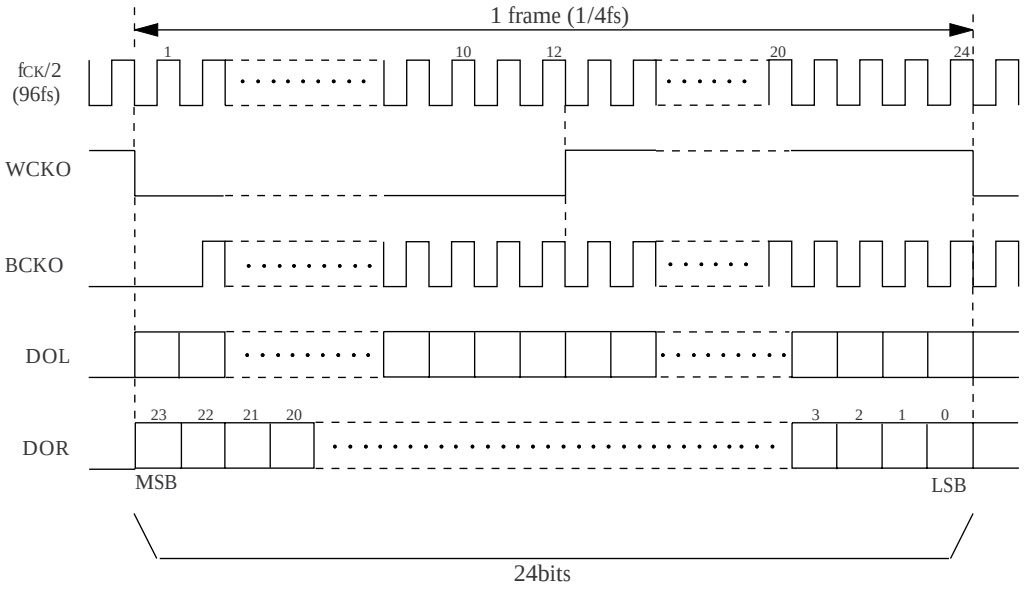
High-speed sampling: 256fs clock, 24-bit data output, 8fs output data rate



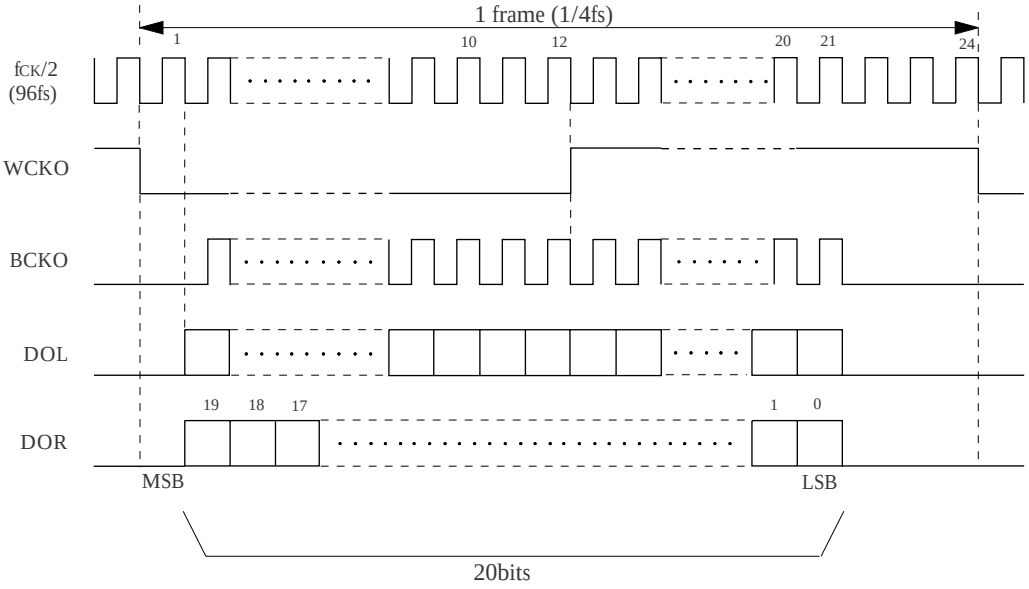
High-speed sampling: 256fs clock, 20-bit data output, 8fs output data rate



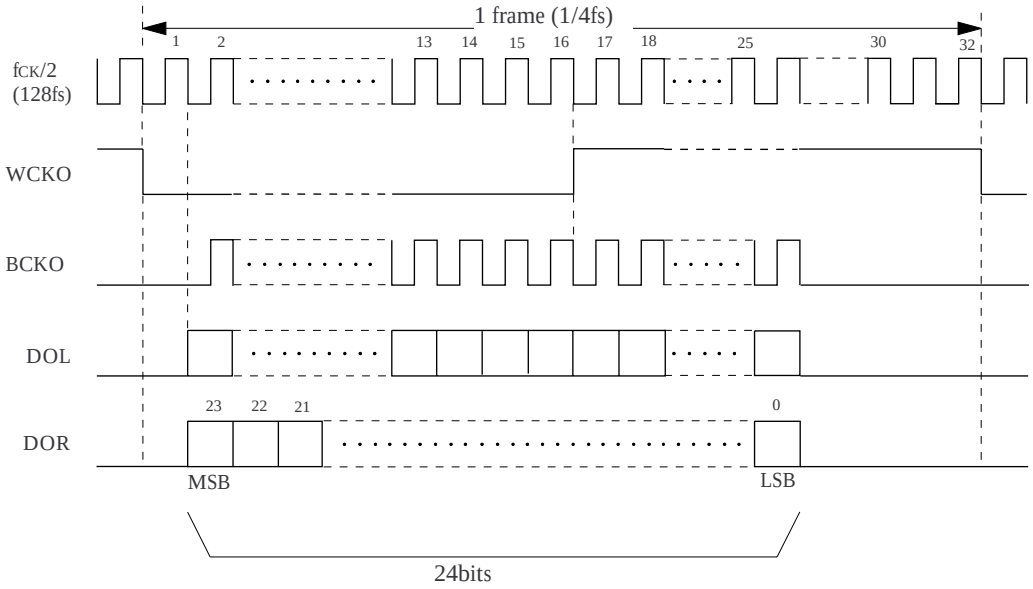
High-speed sampling: 192fs clock, 24-bit data output, 4fs output data rate



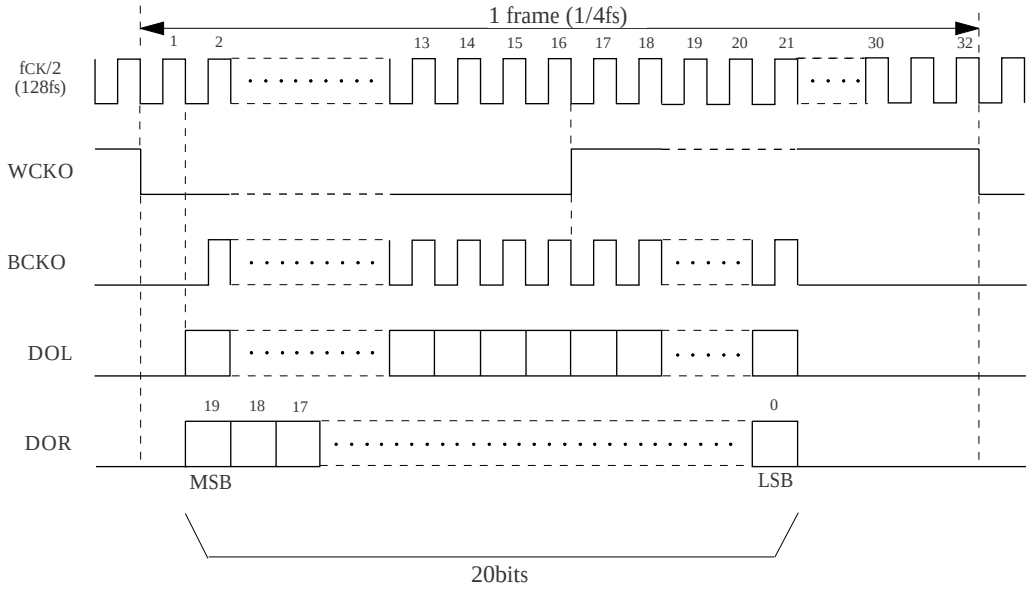
High-speed sampling: 192fs clock, 20-bit data output, 4fs output data rate



High-speed sampling: 256fs clock, 24-bit data output, 4fs output data rate



High-speed sampling: 256fs clock, 20-bit data output, 4fs output data rate



Microprocessor Interface

Microprocessor interface pins

When MDS is LOW, the SM5846AP is controlled by internal flags set by serial data transferred over the microprocessor interface comprising MDLE, MDCK and MDT.

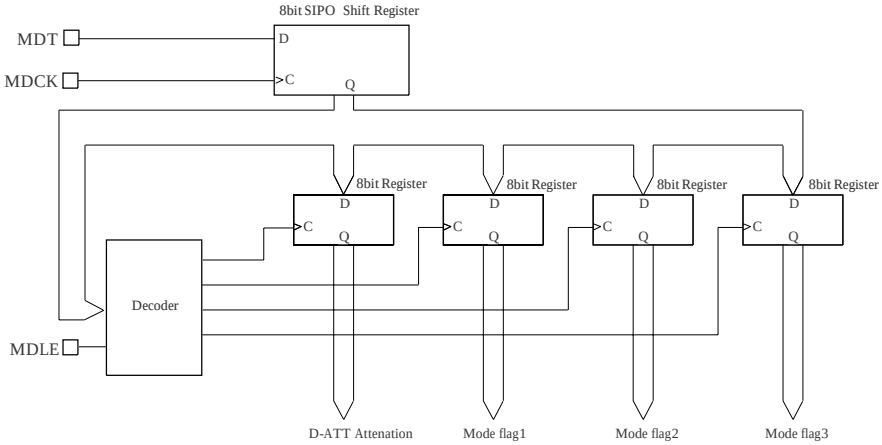
Pin name	Function
MDLE	Microprocessor data latch enable input
MDCK	Microprocessor data transfer clock input

Pin name	Function
MDT	Serial data input

Internal control flag serial data on MDT is input into an internal shift register on the rising edge of MDCK. After 8-bit data has been input, the data in the shift register is stored in one of four internal flag registers on the rising edge of MDLE latch enable.

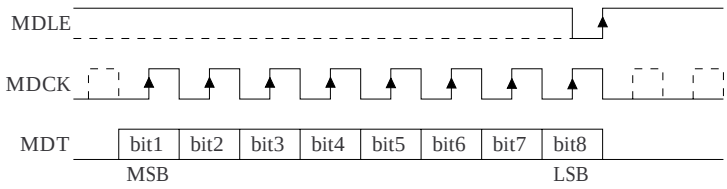
The address of the flag register is derived by decoding bits 1 to 3 of the 8-bit data.

Microprocessor interface



Microprocessor interface data input timing

MDCK and MDLE can also follow the dotted lines above



Serial data format

Register	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
D-ATT attenuation	0	a1	a2	a3	a4	a5	a6	a7
Mode flag 1	1	0	SYNC	TEST1 = 0	$\overline{HS}$	FSEL1	FSEL2	DEEM
Mode flag 2	1	1	$\overline{MUTE}$	$\overline{DITH}$	OBS	IBS1	IBS2	1
Mode flag 3	1	1	ASEL1	ASEL2	1	TEST2 = 0	1	0

Address information is displayed in double-line cells of the table.
Test bits (mode flag 1 bit 4 and mode flag 3 bit 6) should be set to 0.

System Reset

When a reset is necessary

The device must be reset under the following conditions.

- When power is first applied
- When the LRCI clock or system clock stop

Reset input conditions

The $\overline{RST}$ input is active LOW.

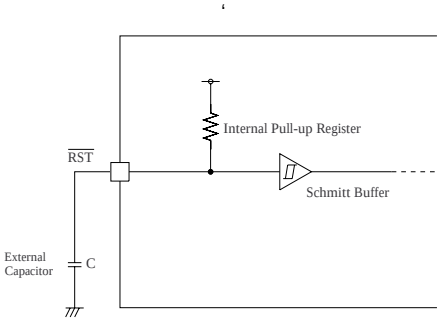
At power-ON reset, $\overline{RST}$ must go LOW and then go HIGH after the XTI and LRCI clocks stabilize (reset release).

Reset timing

The internal arithmetic registers and output sequence are initialized on the rising edge of the LRCI clock after reset release. The internal control flags and D-ATT attenuation register are initialized after RST goes LOW. Outputs DOL and DOR are tied LOW while $\overline{RST}$ is LOW.

Power-ON reset using a capacitor

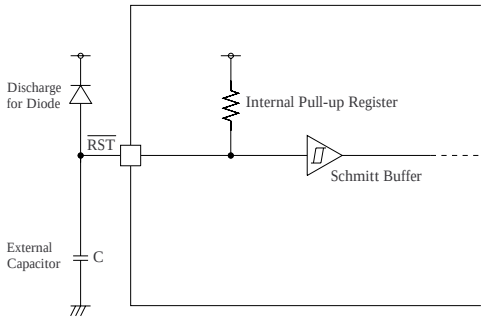
The $\overline{RST}$ input configuration is a Schmitt-trigger input with a pull-up resistor, which means that a simple power-ON reset circuit can be made by connecting a capacitor between $\overline{RST}$ and VSS as shown below.



A 0.01 µF external capacitor is recommended. However, the time constant can be lengthened if longer time is required for the XTI and LRCI clocks to stabilize after power-ON.

The external capacitor discharges through the internal pull-up resistor at power-OFF as this is the only possible discharge path. This could cause reset failure if power is reapplied while the external capacitor is discharging. Therefore, a diode should be connected between $\overline{RST}$ and VDD to quickly discharge the capacitor and ensure correct power-ON reset operation.

External power-ON reset circuit



Internal control flag/D-ATT attenuator register initial values

Register	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
D-ATT attenuation	0	a1 = 0	a2 = 0	a3 = 0	a4 = 0	a5 = 0	a6 = 0	a7 = 0
Mode flag 1	1	0	SYNC = 1	TEST1 = 0	$\overline{HS}$ = 1	FSEL1 = 1	FSEL2 = 1	DEEM = 0
Mode flag 2	1	1	$\overline{MUTE}$ = 1	$\overline{DITH}$ = 1	OBS = 0	IBS1 = 1	IBS2 = 0	1
Mode flag 3	1	1	ASEL1 = 1	ASEL2 = 1	1	TEST2 = 1	1	0

When external muting is required

The SM5846AP has a relatively long group delay time because multi-stage filters are employed to achieve the desired filter characteristics. Under the following conditions, undesirable noise output can occur during the group delay time period. In this case, it may be necessary to use external muting.

- When power is first applied.
  The state of internal registers may be undefined during power-ON.
- When switching the operating mode.
  When switching the operating mode using HS, ASEL1 and ASEL2, the internal register assignments may be changed.
- If the LRCI and/or XTI clock stop.
  If a disturbance occurs during an input data cycle, normal filter output may not be achieved.
- When switching deemphasis ON/OFF.
  Switching the deemphasis filter parameters may cause switching noise output.
- When switching the sampling frequency (clock frequency).
- When switching between input/output data formats (including LRCI clock polarity switching).

Note that switching MDS is inhibited during system operation.

Test Precautions

The following conditions should be maintained for normal operation.

- MDS and DITH inputs should not be simultaneously LOW.
- TEST1 (bit 4 of mode flag 1 register) should not be set to 1.
- TEST2 (bit 4 of mode flag 3 register) should be set to 0 after system reset (including power-ON).
- Mode flag 3 register bit 5 and/or bit 7 should not be set to 0.

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