NIPPON PRECISION CIRCUITS INC.

SM5837AF

Variable-length 1H Delay Line LSI

OVERVIEW

The SM5837AF is a variable-length delay line LSI. It has 12-bit input/output signal which can be set to undergo a delay in the range of 31 to 2078 delay bits. Maximum operating frequency is 40 MHz, making it ideal for use in video signal processing applications.

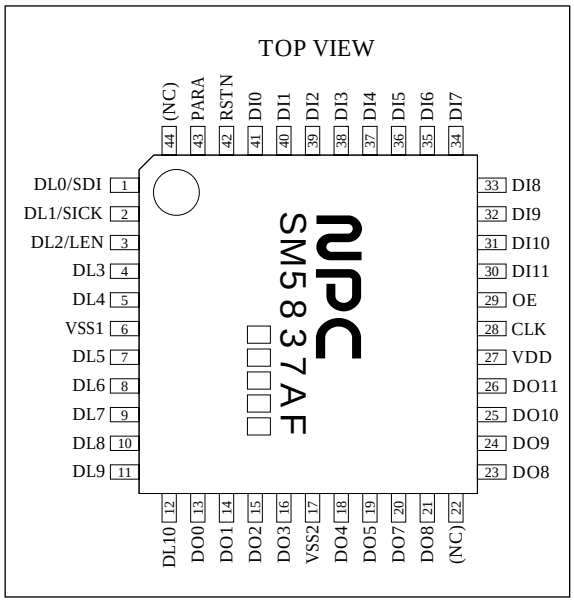
FEATURES

- Variable-length 1H delay
- 12-bit input/output signal width
- 31 to 2078- bit delay length range
- 40 MHz maximum operating frequency
- Selectable delay setting method
  - 11-bit parallel input
  - 3-line serial input
- TTL-compatible input/outputs
- Tristate outputs
- 4.75 to 5.25 V operating voltage
- 44-pin QFP
- Molybenum-gate CMOS process

APPLICATIONS

- Video signal image processing

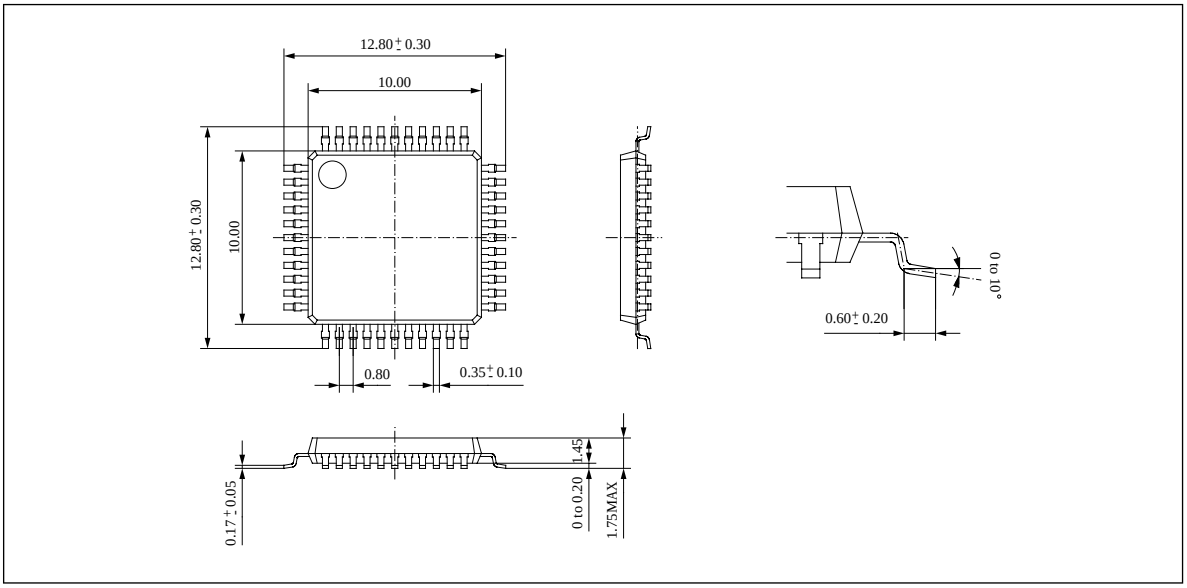
PINOUT



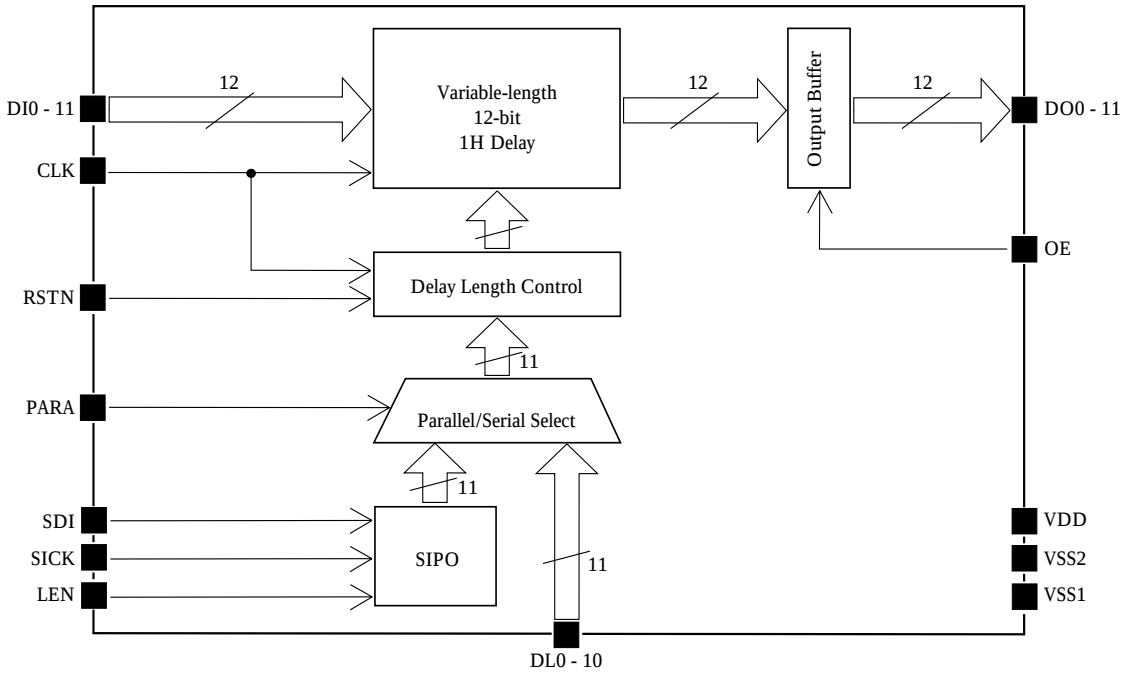
PACKAGE DIMENSIONS

Unit: mm

44-pin QFP



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O (1)	Function
1	DL0/SDI	Ip	Delay length set parallel data bit DL0 (LSB) when PARA is HIGH, and SDI serial data input when PARA is LOW.
2	DL1/SICK	Ip	Delay length set parallel data bit DL1 (bit 1) when PARA is HIGH, and SICK shift clock when PARA is LOW.
3	DL2/LEN	Ip	Delay length set parallel data bit DL2 (bit 2) when PARA is HIGH, and LEN latch clock when PARA is LOW.
4	DL3	Ip	Delay length set data bit 3
5	DL4	Ip	Delay length set data bit 4
6	VSS1	–	Ground (0 V) pin 1
7	DL5	Ip	Delay length set data bit 5
8	DL6	Ip	Delay length set data bit 6
9	DL7	Ip	Delay length set data bit 7
10	DL8	Ip	Delay length set data bit 8
11	DL9	Ip	Delay length set data bit 9
12	DL10	Ip	Delay length set data bit 10
13	DO0	O	Signal output data bit 0
14	DO1	O	Signal output data bit 1
15	DO2	O	Signal output data bit 2
16	DO3	O	Signal output data bit 3
17	VSS2	–	Ground (0 V) pin 2
18	DO4	O	Signal output data bit 4
19	DO5	O	Signal output data bit 5
20	DO6	O	Signal output data bit 6
21	DO7	O	Signal output data bit 7

Number	Name	I/O (1)	Function
22	NC	–	No connection
23	DO8	O	Signal output data bit 8
24	DO9	O	Signal output data bit 9
25	DO10	O	Signal output data bit 10
26	DO11	O	Signal output data bit 11
27	VDD	–	Supply (5 V) pin
28	CLK	I	Clock input
29	OE	Ip	Tristate output enable. Enable when HIGH, and disable when LOW.
30	DI11	Ip	Signal input data bit 11
31	DI10	Ip	Signal input data bit 10
32	DI9	Ip	Signal input data bit 9
33	DI8	Ip	Signal input data bit 8
34	DI7	Ip	Signal input data bit 7
35	DI6	Ip	Signal input data bit 6
36	DI5	Ip	Signal input data bit 5
37	DI4	Ip	Signal input data bit 4
38	DI3	Ip	Signal input data bit 3
39	DI2	Ip	Signal input data bit 2
40	DI1	Ip	Signal input data bit 1
41	DI0	Ip	Signal input data bit 0
42	RSTN	Ip	Reset pin. Normal operation when HIGH, and reset operation when LOW.
43	PARA	Ip	Delay length setting method select. Parallel data (DL0 to DL10) when HIGH, and serial input (SDI, SICK, LEN) when LOW.
44	NC	–	No connection

1. Ip = input pin with built-in pull-up resistor, O = output.

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = V_{SS1} = V_{SS2} = 0$ V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		–0.3 to 7.0	V
Input voltage range	V_{IN}		V_{SS} – 0.3 to V_{DD} + 0.3	V
Storage temperature range	T_{stg}		–40 to 125	°C
Power dissipation	P_D		450	mW
Soldering temperature	T_{sld}		255	°C
Soldering time	t_{sld}		10	s

Recommended Operating Conditions

$V_{SS} = 0$ V

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range	V_{DD}		4.75 to 5.25	V
Operating temperature	T_{opr}		–20 to 70	°C

DC Characteristics

V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C unless otherwise specified

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V, CLK frequency f_C = 40 MHz, OE = 0 V	–	–	85	mA
Input voltage(1) (2)	V_{IH}		2.4	–	–	V
	V_{IL}		–	–	0.5	V
Output voltage(3)	V_{OH}	I_{OH} = –0.4 mA	4.0	–	–	V
	V_{OL}	I_{OL} = 1.6 mA	–	–	0.4	V
Input current(2)	I_{IL}	V_{IN} = 0 V	–	10	20	µA
Input leakage current(1) (2)	I_{LH}	V_{IN} = V_{DD}	–	–	1	µA
Input leakage current(1)	I_{LL}	V_{IN} = 0 V	–	–	1	µA
Output high-impedance leakage current(3)	I_{ZH}	V_{OUT} = V_{DD}	–	–	5	µA
	I_{ZL}	V_{OUT} = 0 V	–	–	5	µA

1. Pin CLK.
2. Pins DI0 to DI11, PARA, DL0/SDI, DL1/SICK, DL2/LEN, DL3 to DL10, OE and RSTN.
3. Pins DO0 to DO11.

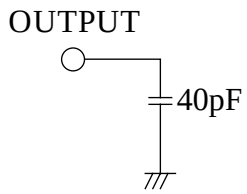
AC Characteristics

V_{DD} = 4.75 to 5.25 V, V_{SS} = 0 V, T_a = –20 to 70 °C unless otherwise specified

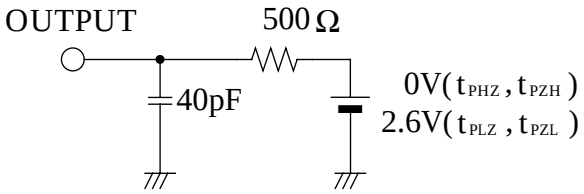
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CLK clock cycle	t_{CP1}		25	–	–	ns
CLK clock HIGH-level pulsewidth	t_{CH1}		10	–	–	ns
CLK clock LOW-level pulsewidth	t_{CL1}		10	–	–	ns
SICK clock cycle	t_{CP2}		50	–	–	ns
SICK clock HIGH-level pulsewidth	t_{CH2}		20	–	–	ns
SICK clock LOW-level pulsewidth	t_{CL2}		20	–	–	ns
CLK, SICK and LEN rise time	t_{CR}	1.0 to 2.0 V	–	–	10	ns
CLK, SICK and LEN fall time	t_{CF}	1.0 to 2.0 V	–	–	10	ns
DI0 to DI11, DL0 to DL10 and RSTN setup time	t_{S1}		10	–	–	ns
DI0 to DI11, DL0 to DL10 and RSTN hold time	t_{H1}		0	–	–	ns
SDI setup time	t_{S2}		25	–	–	ns
SD1 hold time	t_{H2}		25	–	–	ns
SICK rising edge → LEN rising edge	t_{CE}		25	–	–	ns
LEN rising edge → SICK rising edge	t_{EC}		25	–	–	ns
CLK → DO0 to D011 output delay	t_{PD}	See “Load conditions 1”.	–	–	20	ns
CLK → DO0 to D011 output hold time	t_{OH}		5	–	–	ns
OE HIGH-level pulsewidth	t_{OEH}		50	–	–	ns
OE LOW-level pulsewidth	t_{OEL}		50	–	–	ns

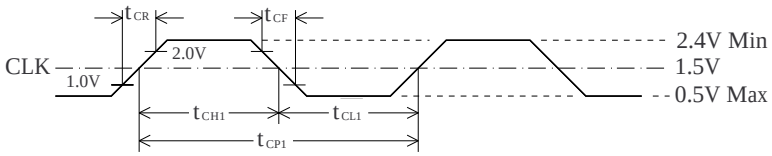
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
OE → DO0 to DO11 output enable delay	t_{PZL}	See "Load conditions 2".	–	–	25	ns
	t_{PZH}		–	–	25	ns
OE → DO0 to DO11 output disable delay	t_{PLZ}		–	–	25	ns
	t_{PHZ}		–	–	25	ns
Input capacitance	C_{IN}	f = 1 MHz	–	–	10	pF
Output capacitance	C_{OUT}	f = 1 MHz, OE = V_{IL}	–	–	15	pF

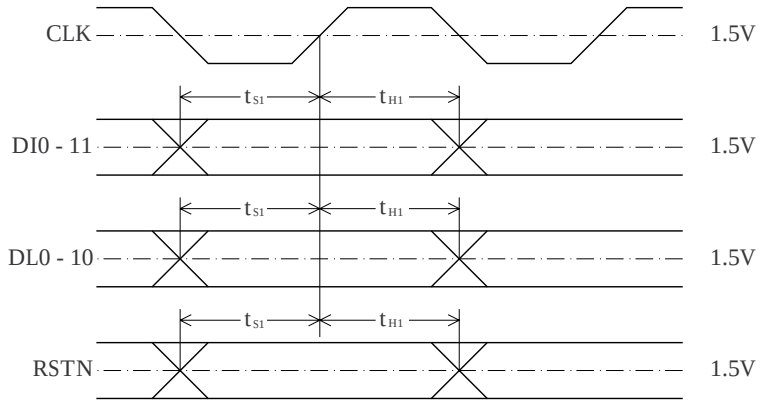
Load conditions 1

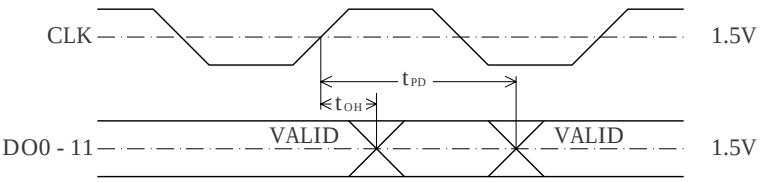


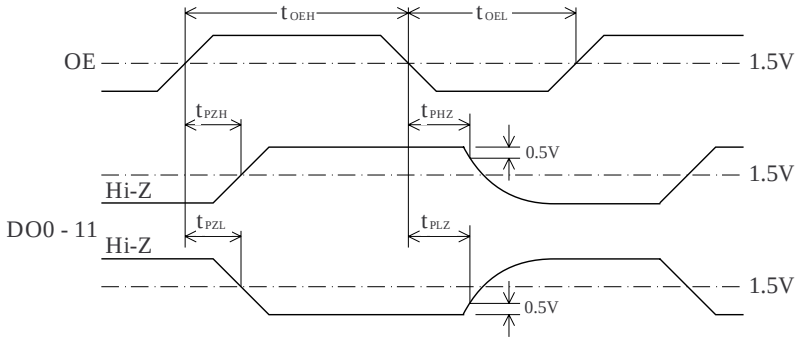
Load conditions 2

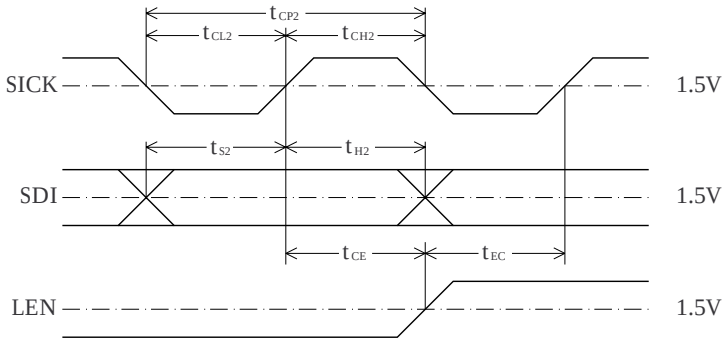












FUNCTIONAL DESCRIPTION

The SM5837AF provides a built-in 1H delay for video signal processing. The delay can be set to a length of 31 to 2078 clock delay bits. The delay length (L_H) can be set using 2 methods, selected by the state of PARA. When PARA is HIGH, the delay length is set by parallel input data on DL0 to DL10. When PARA is LOW, the delay length is set by serial input data using SDI, SICK and LEN. Accordingly, the function of DL0/SDI, DL1/SICK and DL2/LEN is determined by PARA.

Parallel Input Set Method (PARA, DL0 to DL10)

When PARA is HIGH, parallel input data is used to set the delay length. The delay length (L_H) is determined by the input data on DL0 to DL10 as shown in equation 1 and table 1.

$$L_H = 31 + \sum_{k=0}^{10} \{DLk \times 2^k\} \qquad (1)$$

Table 1. Delay bit length setting

DL10	DL9	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	Delay length
0	0	0	0	0	0	0	0	0	0	0	31
0	0	0	0	0	0	0	0	0	0	1	32
0	0	0	0	0	0	0	0	0	1	0	33
0	0	0	0	0	0	0	0	0	1	1	34
0	0	0	0	0	0	0	0	1	0	0	35
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	0	1	1	1	1	0	0	0	0	1	512

Table 1. Delay bit length setting

DL10	DL9	DL8	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	Delay length
0	0	1	1	1	1	0	0	0	1	0	513
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	1	1	0	0	0	0	1	1024
0	1	1	1	1	1	0	0	0	1	0	1025
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	0	0	0	0	1	2048
1	1	1	1	1	1	0	0	0	1	0	2049
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
1	1	1	1	1	1	1	1	1	1	0	2077
1	1	1	1	1	1	1	1	1	1	1	2078

Serial Input Set Method (PARA, SDI, SICK, LEN)

When PARA goes LOW, 3-input serial data set method is used to set the delay length. Inputs DL3 to DL10 are ignored. SDI, SICK and LEN function as the serial data input, serial data shift clock and latch clock enable, respectively.

The serial input data format, shown in figure XREF, comprises 11-bit serial data (S0 to S10) input on SDI in sync with SICK. The data on SDI is clocked into the serial-to-parallel converter shift register on the rising edge of SICK, and 11-bit parallel data is then latched into the delay length set register on the rising edge of LEN.

The delay length (L_H) is determined by the input data S0 to S10 (just as for parallel input data DL0 to DL10) as shown in equation 2. See also table 1.

Note that SICK and CLK can be asynchronous.

$$L_H = 31 + \sum_{k=0}^{10} \{Sk \times 2^k\} \qquad (2)$$

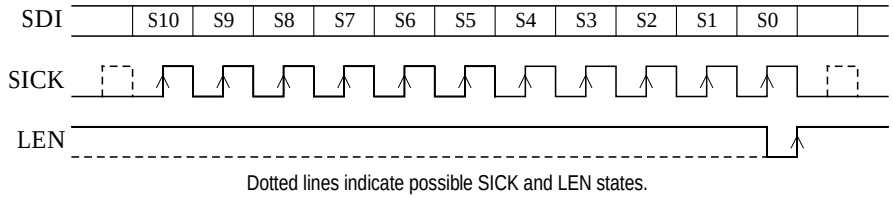


Figure 1. Serial input data format

Delay Clock Input (CLK)

All 1H delay registers operate in sync with the delay clock CLK. The maximum clock frequency is 40 MHz.

Input Data (DI0 to DI11)

DI0 to DI11 are the 12-bit data inputs.

Output Data (DO0 to DO11,OE)

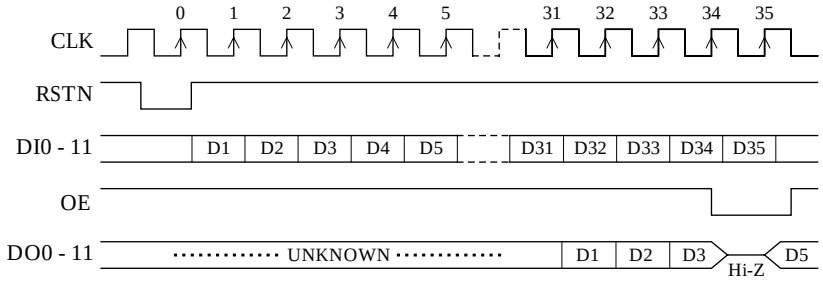
DO0 to DO11 are the 12-bit data outputs. They are tristate outputs, with the output state selected by OE. When OE is HIGH, the outputs are enabled. When OE is LOW, the outputs are disabled (high-impedance state).

Reset (RSTN)

At power-ON, the internal timing generator circuits must be initialized by a LOW-level input on RSTN. After RSTN goes HIGH, the set delay length becomes active.

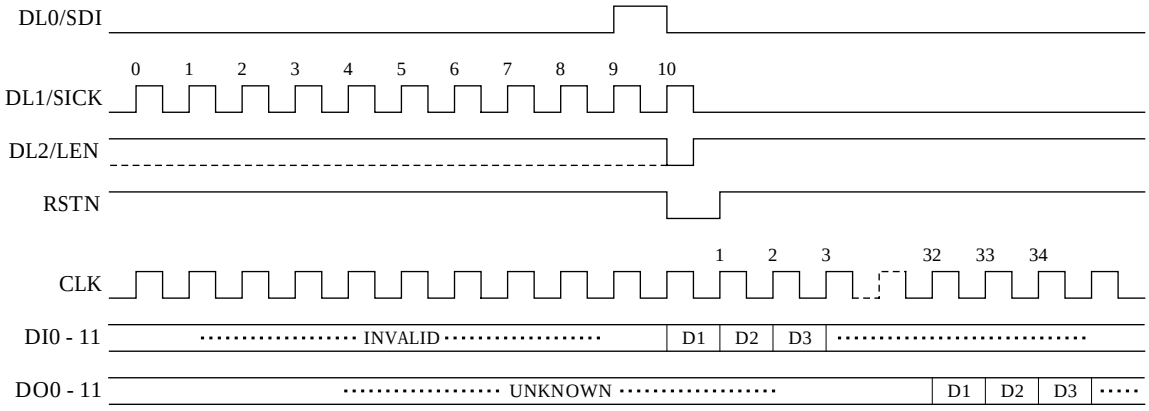
TIMING DIAGRAMS

Parallel Set Data (Delay Length = 31)



PARA=H , DL0-10=L

Serial Set Data (Delay Length = 32)



PARA=L , DL3-10=Don't Care , OE=H

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