NIPPON PRECISION CIRCUITS LTD.

SM5831F

Digital Filter for Video Signal Processors

OVERVIEW

The SM5831F is an FIR digital filter fabricated in Molybdenum-gate CMOS for video signal processors.

The SM5831F processes 9-bit signal data using mathematical blocks set by 8-bit coefficient data. It comprises four 9 × 8-bit multipliers and eight 14-bit adders, enabling it to be configured as a single-chip, asymmetrical 4-tap filter, or a symmetrical 7-tap or 8-tap filter. Several devices can be cascaded to realize longer filters.

The filter coefficients are stored in four programmable registers. The maximum signal sampling frequency is 15 MHz.

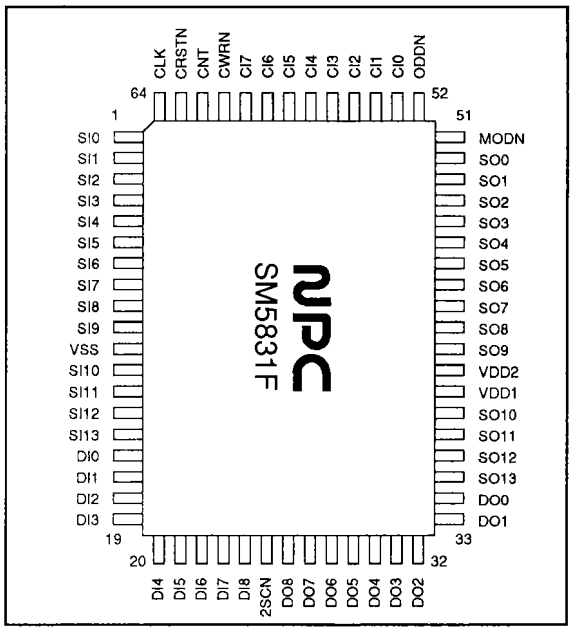
FEATURES

- Filter configuration
  - Symmetrical 8-tap FIR filter (Mode I)
  - Symmetrical 7-tap FIR filter (Mode II)
  - Asymmetrical 4-tap FIR filter (Mode III)
  - Devices can be cascaded for longer filters
- Data format
  - 9-bit unsigned-magnitude or 2s-complement input data
  - 8-bit 2s-complement coefficient data
  - 14-bit 2s-complement internal processing
- 15 MHz maximum sampling rate
- Arithmetic blocks
  - Four 9 × 8-bit → 14-bit multipliers
  - Four 8-bit coefficient registers
  - Eight 14 + 14-bit → 14-bit adders
- Programmable coefficient registers
- 5 ±0.5 V supply
- 64-pin QFP
- Molybdenum-gate CMOS process

APPLICATIONS

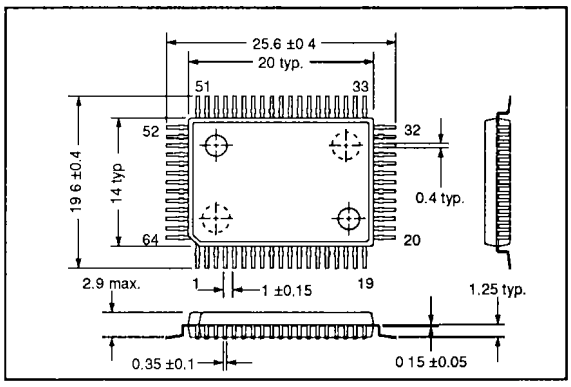
- Digital video
- One-dimensional and two-dimensional filtering
- Correlators
- Adaptive filters

PINOUT

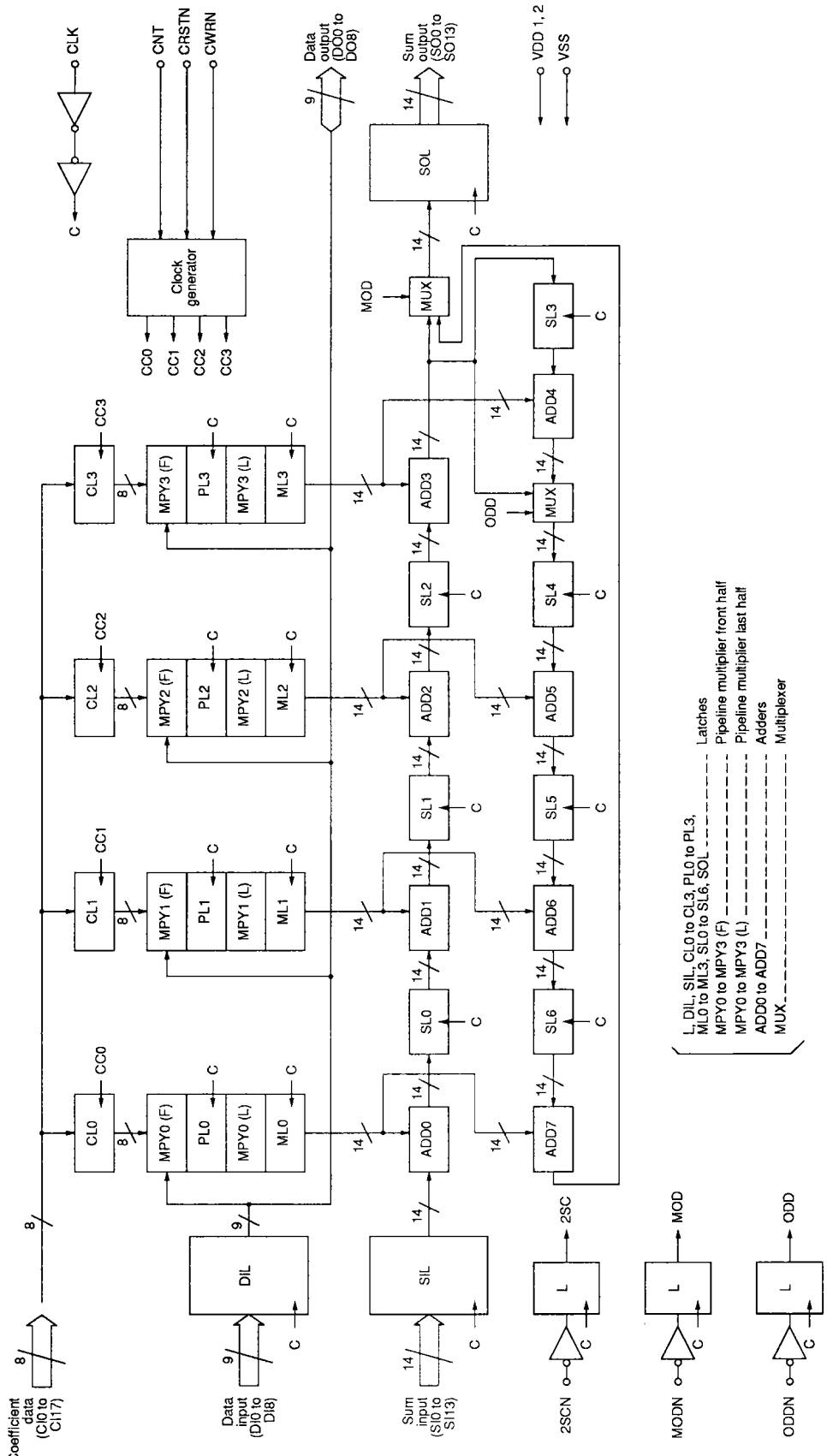


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1 to 10, 12 to 15	SI0 to SI13	i	Cascade sum inputs (SI0 is LSB, SI13 is MSB)
16 to 24	DI0 to DI8	i	Signal data inputs (DI0 is LSB, DI8 is MSB)
25	2SCN	ip	Input signal data format select. Unsigned-magnitude when HIGH and 2s complement when LOW.
26 to 34	DO8 to DO0	o	Signal data outputs (DO0 is LSB, DO8 is MSB)
35 to 38, 41 to 50	SO13 to SO0	o	Sum outputs (SO0 is LSB, SO13 is MSB)
51	MODN	ip	Filter type select. Symmetrical when HIGH and asymmetrical when LOW.
52	ODDN	ip	Symmetrical filter tap length select. Eight when HIGH and seven when LOW.
53 to 60	CI0 to CI7	i	Coefficient data inputs (CI0 is LSB, CI7 is MSB)
61	CWRN	ip	Coefficient write clock
62	CNT	ip	Coefficient write control signal
63	CRSTN	ip	Coefficient clock generator reset signal
64	CLK	i	Clock signal
11	VSS		Ground
39	VDD1		5 ±0.5 V supply
40	VDD2		

Note

i = input, ip = input with pull-up resistance, o = output

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_{IN}	−0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	400	mW
Storage temperature range	T_{stg}	−40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	−20 to 70	deg. C

DC Electrical Characteristics

T_a = –20 to 70 deg. C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			
			min	typ	max	
Current consumption	I_{DD}	V_{DD} = 5.0 V, f_{CLK} = 15 MHz, V_{IN}(CLK) = 0.5 to 2.4 V	–	–	70	mA
HIGH-level input voltage	V_{IH}	See notes 1 and 2.	2.4	–	–	V
LOW-level input voltage	V_{IL}	See notes 1 and 2.	–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = –1.0 mA. See note 3.	V_{DD} – 0.5	–	–	V
LOW-level output voltage	V_{OL}	I_{OL} = 4.0 mA. See note 3.	–	–	0.4	V
HIGH-level input leakage current	I_{LH}	V_{IN} = V_{DD}. See notes 1 and 2.	–	–	1	µA
LOW-level input leakage current	I_{LL}	V_{IN} = V_{SS}. See note 1.	–	–	1	µA
LOW-level input current	I_{IL}	V_{IN} = V_{SS}. See note 2.	–	10	20	µA

Notes

1. Pins SI0 to SI13, DI0 to DI8, CI0 to CI7 and CLK are TTL-level input pins.
2. Pins 2SCN, MODN, ODDN, CWRN, CNT and CRSTN are TTL-level inputs with pull-up resistances.
3. Pins DO0 to DO8 and SO0 to SO13 are TTL-level outputs.

AC Electrical Characteristics

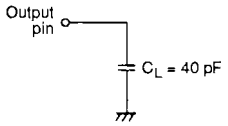
T_a = –20 to 70 deg. C, V_{DD} = 4.5 to 5.5 V, V_{SS} = 0 V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Clock frequency	f_{CLK}	See figure 1.	0.1	–	15	MHz
LOW-level clock pulsewidth	t_{PWL}	See figure 1.	18	–	–	ns
HIGH-level clock pulsewidth	t_{PWH}	See figure 1.	25	–	–	ns
Input setup time	t_{S1}	See note 4. See figure 2.	15	–	–	ns
	t_{S2}	See note 5. See figure 3.	25	–	–	ns
Input hold time	t_{H1}	See note 4. See figure 2.	5	–	–	ns
	t_{H2}	See note 5. See figure 3.	5	–	–	ns
CRSTN clock pulsewidth	t_{PWR}	See figure 4.	25	–	–	ns
CRSTN to CNT time	t_{RN}	See figure 4.	0	–	–	ns
Output delay time	t_D	See note 3. See figure 5.	10	–	45	ns
Input capacitance	C_{IN}	f = 1 MHz. See notes 1 and 2.	–	–	15	pF

Notes

1. Pins SI0 to SI13, DI0 to DI8, CI0 to CI7 and CLK are TTL-level input pins.

2. Pins 2SCN, MODN, ODDN, CWRN, CNT and CRSTN are TTL-level inputs with pull-up resistances.
3. Pins DO0 to DO8 and SO0 to SO13 are TTL-level outputs.
4. Pins SI0 to SI13, DI0 to DI8, 2CSN, MODN and ODDN are signal inputs.
5. Pins CI0 to CI7, CNT and CWRN are coefficient inputs.
6. Output load circuit



Timing Diagrams

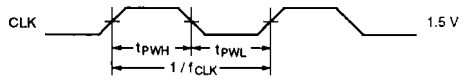


Figure 1. Clock input waveform

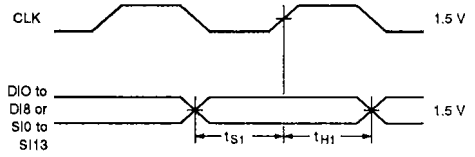


Figure 2. Signal and sum input setup/hold timing

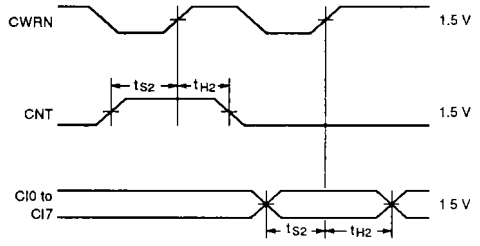


Figure 3. Coefficient input setup/hold timing

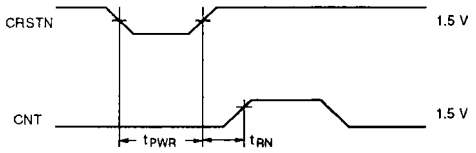


Figure 4. Coefficient clock generator reset timing

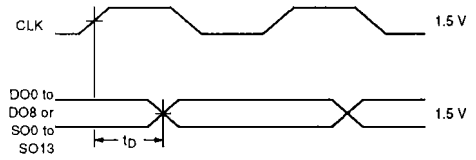


Figure 5. Output delay timing

FUNCTIONAL DESCRIPTION

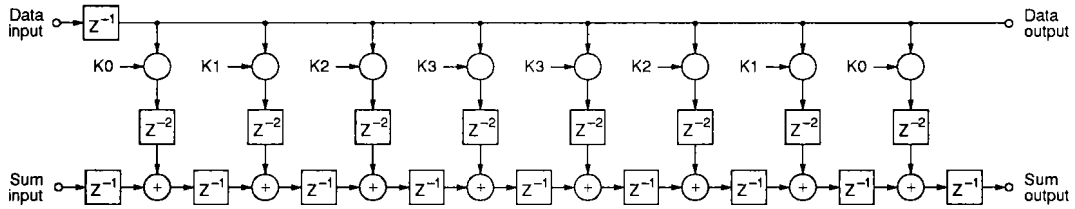
Filter Type Select

The SM5831F can be configured as a symmetrical filter—with filter coefficients symmetrical about the center tap—or an asymmetrical filter as shown in the following table.

Mode	MODN	ODDN	Filter configuration
I	HIGH or open	HIGH or open	Symmetrical 8-tap FIR filter
II	HIGH or open	LOW	Symmetrical 7-tap FIR filter
III	LOW	HIGH or open	Asymmetrical 4-tap FIR filter

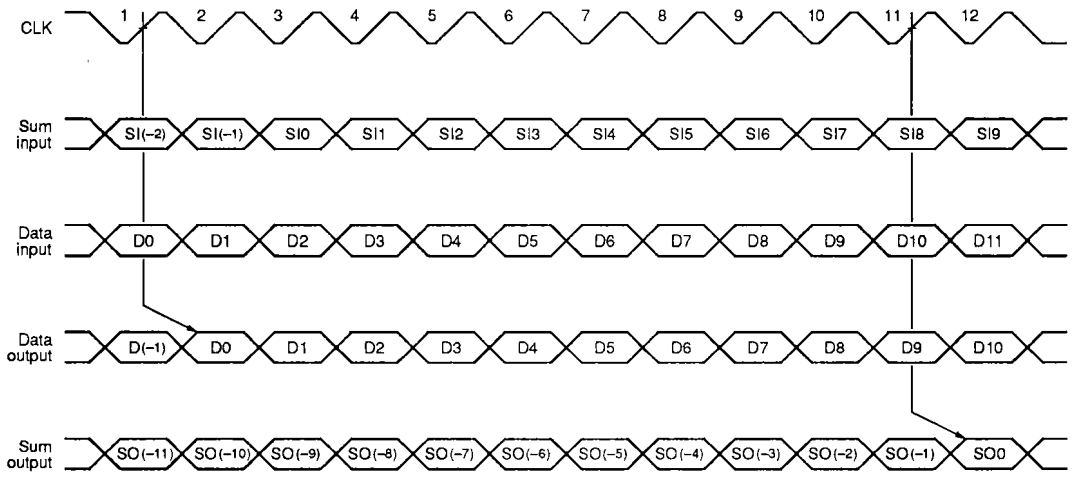
Mode I

Flow diagram



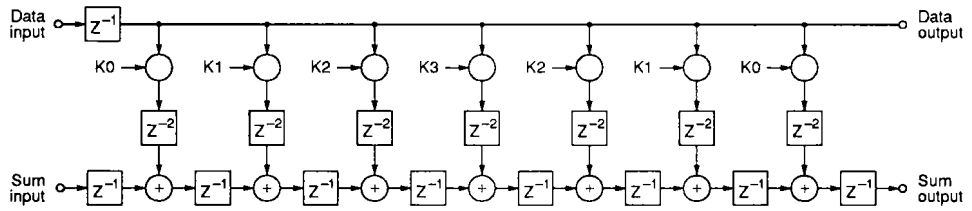
$$S_o0 = K0 \cdot (D0 + D7) + K1 \cdot (D1 + D6) + K2 \cdot (D2 + D5) + K3 \cdot (D3 + D4) + S_i0$$

Timing



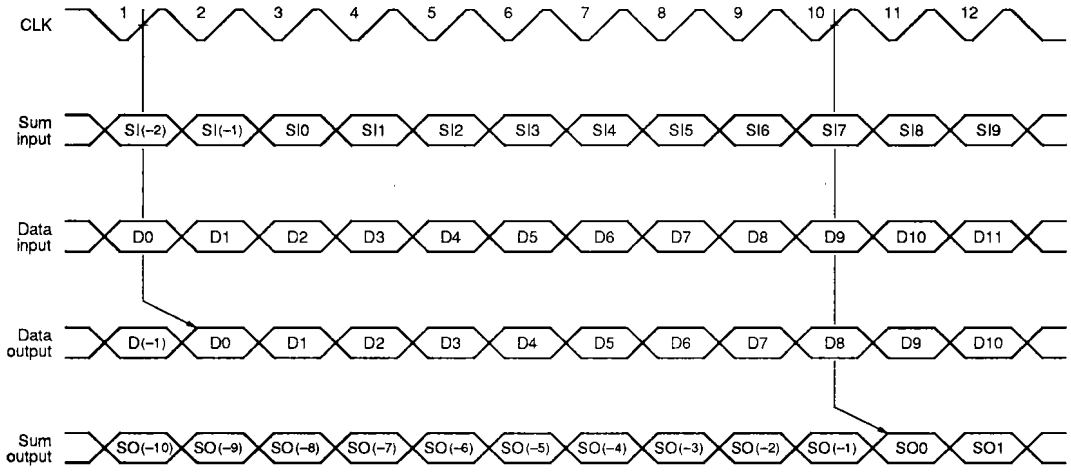
Mode II

Flow diagram



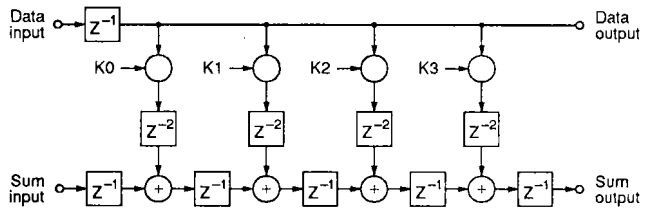
$$S_o0 = K0 \cdot (D0 + D6) + K1 \cdot (D1 + D5) + K2 \cdot (D2 + D4) + K3 \cdot D3 + S_i0$$

Timing



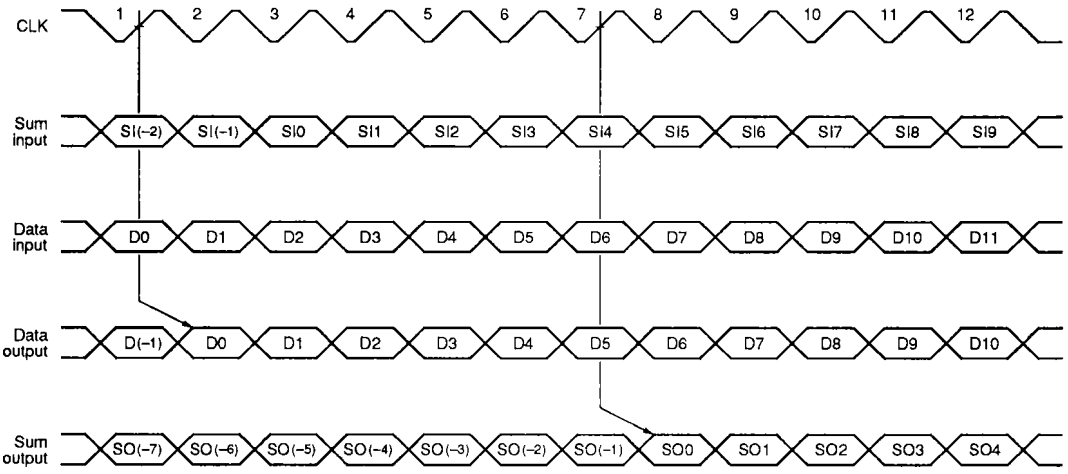
Mode III

Flow diagram



$S_o0 = K0 \cdot D0 + K1 \cdot D1 + K2 \cdot D2 + K3 \cdot D3 + S_i0$

Timing



Signal Data Format Select

The 9-bit input signal data format is determined by the state of pin 2SCN.

2SCN	Signal data format
HIGH or open	Unsigned magnitude
LOW	2s complement

Unsigned magnitude (with decimal point)

Decimal point

DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

(MSB) (LSB)

2s complement (with decimal point)

Decimal point

DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

(MSB) (LSB)

Coefficient Data Format

Coefficient data is in 8-bit 2s-complement format.

Decimal point

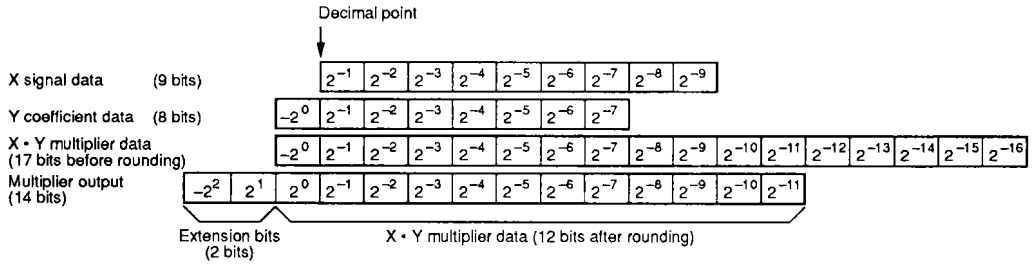
CI7	CI6	CI5	CI4	CI3	CI2	CI1	CI0
-2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}

(MSB) (LSB)

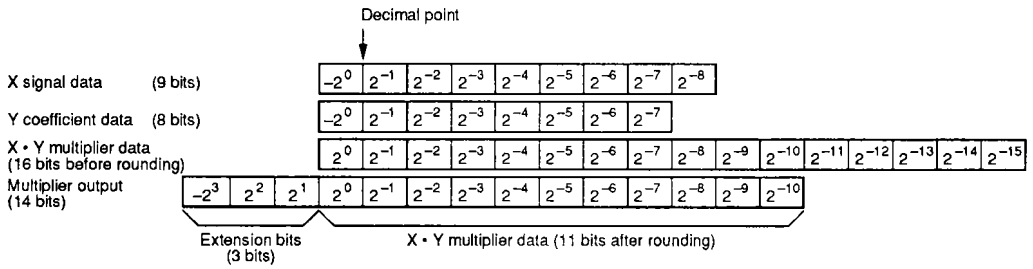
Multiplier Input/Output Data

The following figures show the relationship between the input data, coefficient data and output data.

Unsigned-magnitude input data



2s-complement input data

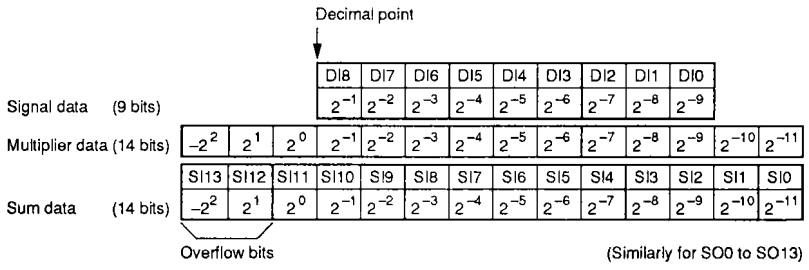


In both data formats, the five least-significant bits from the multiplier output are rounded off. The multiplier output sign bit is extended to the total of 14 bits. The multiplier output is in 14-bit, 2s-complement format.

Adder Arithmetic Data Format

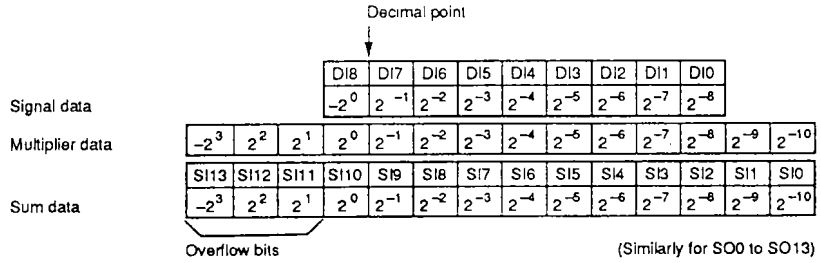
All internal arithmetic operations are performed using 14-bit 2s-complement format.

Unsigned-magnitude input data



The range of the sum result before overflow is ($-4 < SUM < 4 - 2^{-11}$).

2s-complement input data

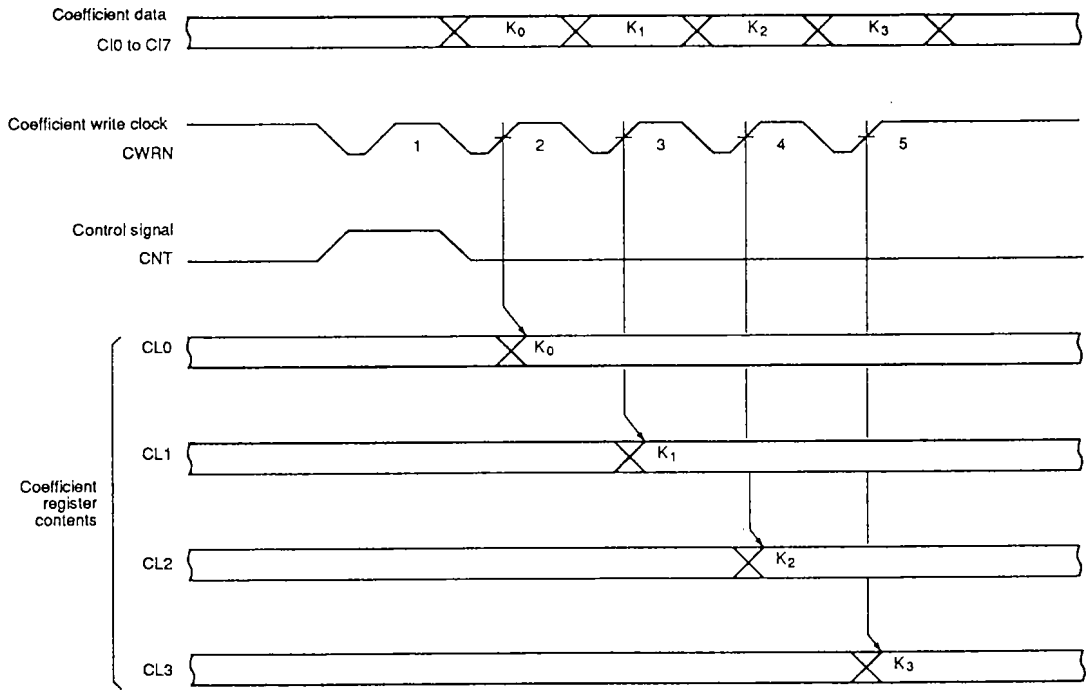


The range of the sum result before overflow is $(-8 < SUM < 8 - 2^{-10})$.

Coefficient Data Program

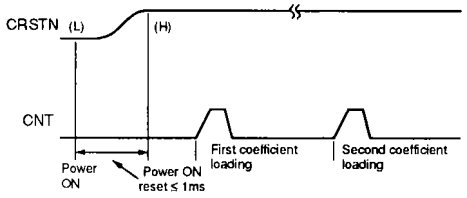
The four coefficient registers are written consecutively using the CWRN write clock and CNT control signal. See the following figure.

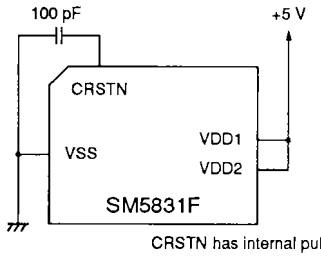
- The write counter is reset when a CWRN rising edge occurs when CNT is HIGH (point 1).
- Subsequent CWRN rising edges (points 2, 3, 4 and 5) starts write operations to registers CL0, CL1, CL2 and CL3, respectively.
- Writing to registers does not occur again until CNT goes from LOW to HIGH.



Power-ON Intialization

The internal coefficient write clock generator must be reset after power-ON by taking CRSTN LOW. The following figures show just one example circuit that implements the reset function and it's related timing.





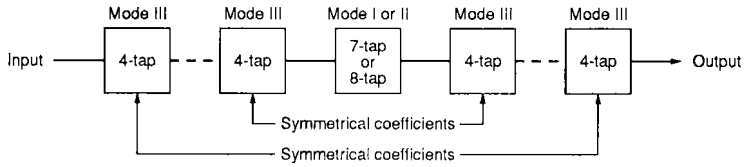
CRSTN has internal pull-up

Cascade Connection

Two or more SM5831F ICs can be cascaded to realize longer filters. In a cascade connection, the sum outputs (SO0 to SO13) are connected to the sum inputs (SI0 to SI13) of the next device.

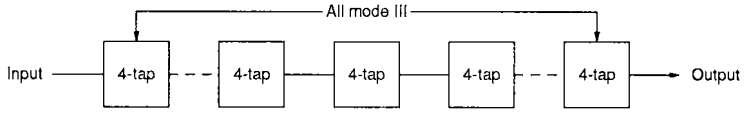
Symmetrical filter cascade configuration

The center device in the filter chain is configured as either a symmetrical 7-tap or 8-tap filter surrounded by asymmetrical 4-tap filters.



Asymmetrical filter cascade configuration

All devices are configured as asymmetrical 4-tap filters.



Filter Coefficient Limitations

The range of permissible filter coefficients is

$$-1 \leq C_i \leq 1 - 2^{-7} \quad (0 \leq i \leq N - 1)$$

where N is the number of filter taps.

The sum result range before overflow is

1. For unsigned-magnitude input data

$$C\ SUM \leq 4 - 2^{-7}$$

2. For 2s-complement input data

$$C\ SUM \leq 8 - 2^{-7}$$

$$\text{where } C\ SUM = \sum_{i=0}^{N-1} |C_i|$$

assuming that the magnitude of the input data is less than one.

Filter Tap Number Limitations

Multiplier output is rounded to 14 bits in each stage, which generates quantization noise that accumulates in the final stage. The quantization noise generated by each multiplier stage is

1. For unsigned-magnitude input data

$$N_{QM} = \frac{(2^{-11})^2}{12}$$

2. For 2s-complement input data

$$N_{QM} = \frac{(2^{-10})^2}{12}$$

and the quantization noise caused at the output by rounding at the mth bit is

$$N_{QO} = \frac{(2^{-m})^2}{12}$$

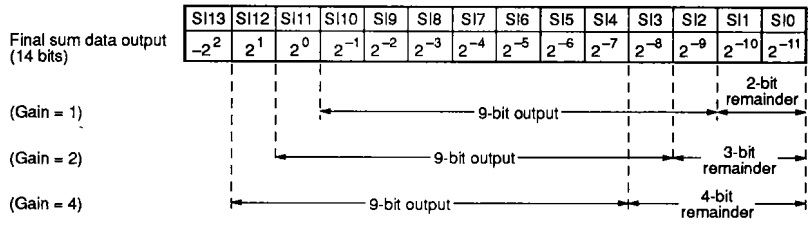
Therefore, the maximum number of taps a filter can have, N_F, before the internal quantization noise exceeds the output noise is given by

$$N_F \leq \frac{N_{QO}}{N_{QM}}$$

The range of bits of the sum output word depends on the gain of the filter. The output signal, therefore, should not exceed the maximum value represented by the selected bits.

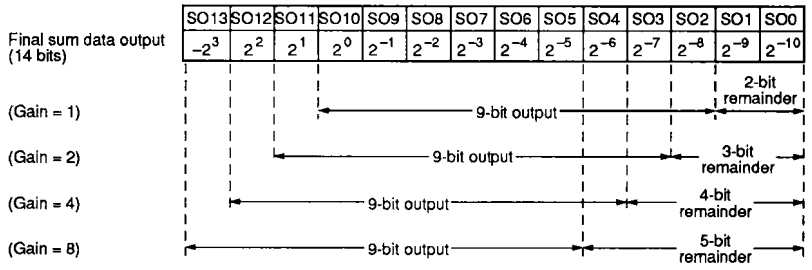
The following two examples demostrate this limitation.

For 9-bit unsigned-magnitude input data



Maximum gain	Maximum number of taps
1	16
2	64
4	256

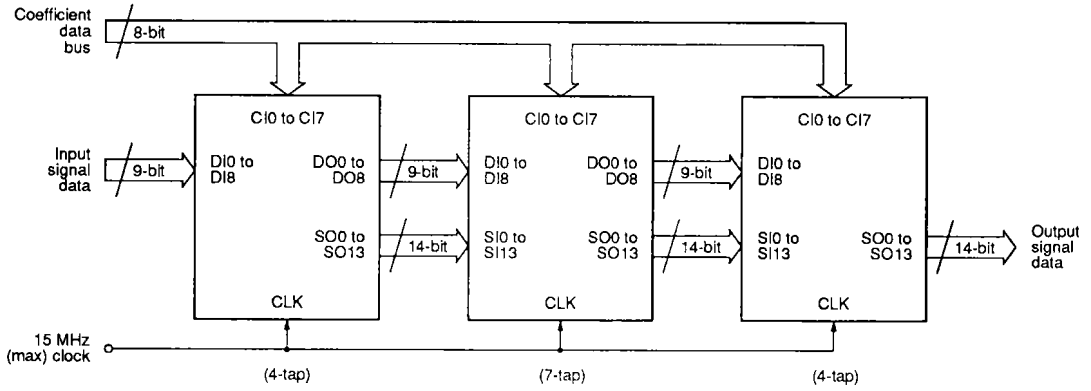
For 9-bit 2s-complement input data



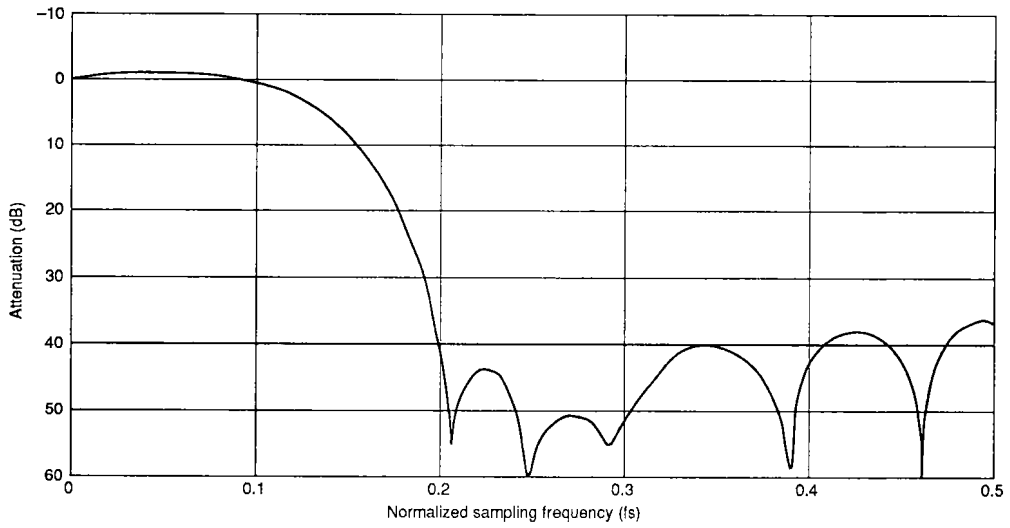
Maximum gain	Maximum number of taps
1	16
2	64
4	256
8	1024

TYPICAL APPLICATION

15-tap Linear Phase Filter



Typical Filter Characteristic



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