NIPPON PRECISION CIRCUITS LTD.

SM5823AP

High-speed, 24-bit SIPO/PISO Converter

OVERVIEW

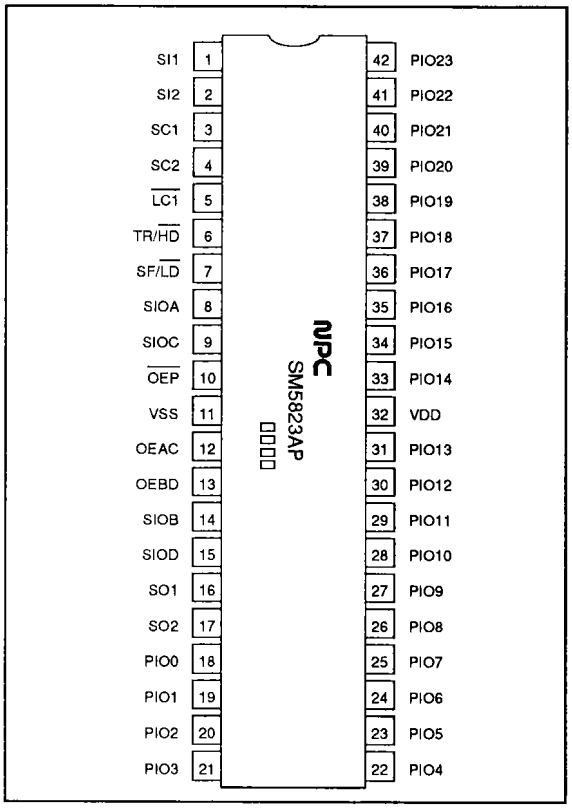
The SM5823AP is a high-speed, 24-bit serial-to-parallel converter and parallel-to-serial converter fabricated in Molygate ® CMOS.

The SM5823AP features a mode selection scheme that allows it to operate as 8-, 16- or 24-bit converters (SIPO and PISO). It also features TTL-compatible, buffered input/outputs for easy bus interfacing, 30 MHz maximum operating frequency and low power consumption, making it ideal for digital video and audio signal processing applications.

FEATURES

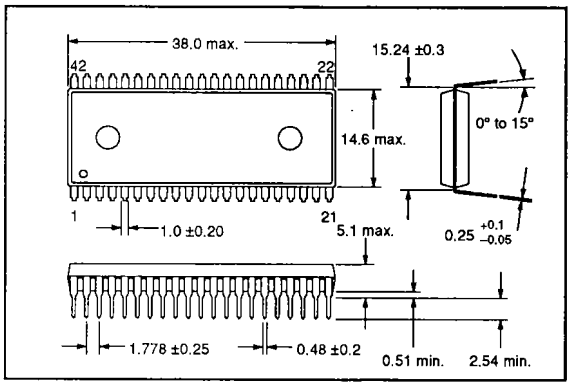
- Functions
  - 8/16/24-bit serial-to-parallel converter and parallel-to-serial converter
  - 30 MHz maximum operating frequency
  - 24-bit parallel I/O, general-purpose port bus interface
  - Extendable to lengths greater than 24 bits for both SIPO and PISO conversion
  - TTL-compatible input/outputs
  - 5 ±0.5 V supply
  - 42-pin shrink DIP
- Component blocks
  - Three 8-bit SIPO registers
  - Three 8-bit parallel output registers
  - Three 8-bit parallel input latches
  - Three 8-bit PISO registers
  - One 24-bit parallel input/output

PINOUT

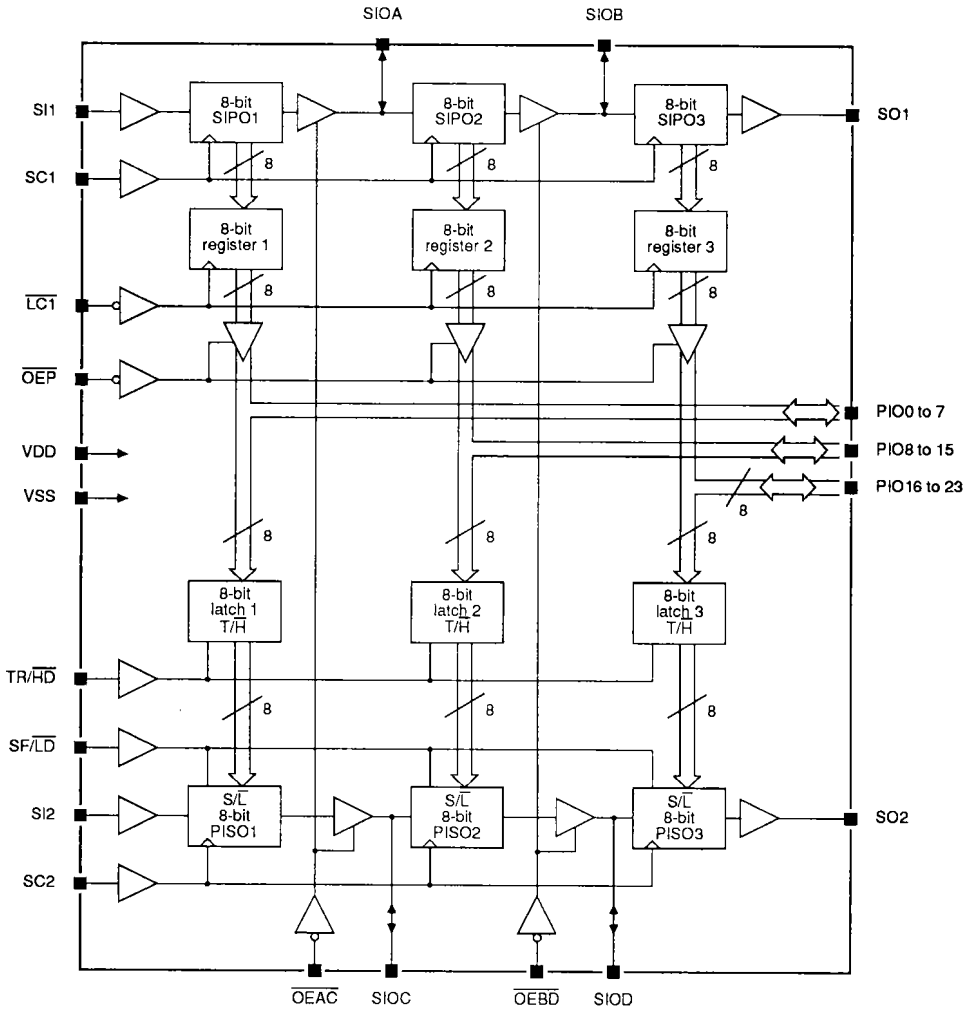


PACKAGE DIMENSIONS

Unit: mm



BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	I/O	Description
1	SI1	I	SIPO serial data 1
2	SI2	I	PISO serial data 1
3	SC1	I	SIPO shift clock (rising-edge trigger)
4	SC2	I	PISO shift clock (rising-edge trigger)
5	$\overline{LC1}$	I	SIPO data latch clock (falling-edge trigger)
6	TR/$\overline{HD}$	I	PISO data latch clock. Transparent when HIGH and hold when LOW
7	SF/$\overline{LD}$	I	PISO shift/load control signal. Shift when HIGH and load when LOW
8	SIOA	I/O	SIPO serial output 1 and SIPO serial input 2
9	SIOC	I/O	PISO serial output 1 and PISO serial input 2
10	$\overline{OEP}$	I	Parallel output enable signal. Enable when LOW and disable when HIGH
11	VSS		Ground

Number	Name	I/O	Description
12	$\overline{OEAC}$	I	SIOA and SIOC serial output enable signal. Enable when LOW and disable when HIGH
13	$\overline{OEBD}$	I	SIOB and SIOD serial output enable signal. Enable when LOW and disable when HIGH
14	SIOB	I/O	SIPO serial output 2 and SIPO serial input 3
15	SIOD	I/O	PISO serial output 2 and PISO serial input 3
16	SO1	O	SIPO serial output 3
17	SO2	O	PISO serial output 3
18 to 31	PIO0 to PIO13	I/O	Parallel input/outputs
32	VDD		5 ±0.5 V supply
33 to 42	PIO14 to PIO23	I/O	Parallel input/outputs

SPECIFICATIONS

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	−0.3 to 7.0	V
Input voltage range	V_{IN}	−0.3 to V_{DD} +0.3	V
Power dissipation	P_D	500	mW
Storage temperature range	T_{stg}	−40 to 125	deg. C
Soldering temperature	T_{sld}	255	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	4.5 to 5.5	V
Operating temperature range	T_{opr}	−20 to 70	deg. C

DC Electrical Characteristics

V_{DD} = 4.5 to 5.5 V, T_a = −20 to 70 deg. C, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Standby current consumption	I_S	V_{IN} = V_{DD} or 0 V	–	–	1.0	µA
Operating current consumption	I_{DD}	V_{DD} = 5 V, f = 30 MHz, all outputs open	–	–	20	mA
HIGH-level input voltage	V_{IH}	See notes 1 and 2.	2.4	–	–	V
LOW-level input voltage	V_{IL}	See notes 1 and 2.	–	–	0.5	V
HIGH-level output voltage	V_{OH}	I_{OH} = −1.0 mA. See notes 2 and 3.	2.5	–	–	V

Parameter	Symbol	Condition		Rating min	Rating typ	Rating max	Unit
LOW-level output voltage	V_{OL1}	See notes 2 and 3.	I_{OL} = 4.0 mA	–	–	0.4	V
	V_{OL2}		I_{OL} = 16.0 mA	–	–	0.8	
HIGH-level input current	I_{IH}	$V_{IN} = V_{DD}$. See note 1.		–	–	1.0	µA
LOW-level input current	I_{IL}	V_{IN} = 0 V. See note 1.		–	10	20	µA
High-impedance output HIGH-level leakage current	I_{ZH}	$V_{\overline{OEP}} = V_{\overline{OEAC}} = V_{\overline{OEBD}} = V_{IH}$, $V_{OUT} = V_{DD}$. See note 2.		–	–	5.0	µA
HIGH-impedance output LOW-level leakage current	I_{ZL}	$V_{\overline{OEP}} = V_{\overline{OEAC}} = V_{\overline{OEBD}} = V_{IH}$, V_{OUT} = 0 V. See note 2.		–	–	5.0	µA

Notes

1. Pins SI1, SI2, SC1, SC2, $\overline{LC1}$, TR/$\overline{HD}$, SF/$\overline{LD}$, $\overline{OEP}$, $\overline{OEAC}$ and $\overline{OEBD}$ are TTL-level inputs with pull-up resistances.
2. Pins SIOA, SIOB, SIOC, SIOD and PIO0 to PIO23 are TTL-level input/outputs.
3. Pins SO1 and SO2 are TTL-level outputs.

AC Electrical characteristics

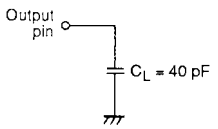
V_{DD} = 4.5 to 5.5 V, T_a = –20 to 70 deg. C, V_{SS} = 0 V unless otherwise noted

Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
SC1 and SC2 shift clock frequency	f_{SC}	50% duty. See figures 1 and 2.	0	–	30	MHz
SI1 to SC1 setup time	t_{S1}	See figure 1.	15	–	–	ns
SI1 to SC1 hold time	t_{H1}		0	–	–	ns
SI2 to SC2 setup time	t_{S2}	See figure 2.	20	–	–	ns
SI2 to SC2 hold time	t_{H2}		0	–	–	ns
SC1 to $\overline{LC1}$ setup time	t_{S3A}	See figure 3.	15	–	–	ns
	t_{S3B}		5	–	–	
SF/$\overline{LD}$ to SC2 setup time	t_{S4}	See figure 4.	15	–	–	ns
SF/$\overline{LD}$ to SC2 hold time	t_{H4}		0	–	–	ns
SIOA, SIOB to SC1 setup time	t_{S5}	See figure 5.	20	–	–	ns
SIOA, SIOB to SC1 hold time	t_{H5}		0	–	–	ns
SIOC, SIOD to SC2 setup time	t_{S6}	See figure 6.	20	–	–	ns
SIOC, SIOD to SC2 hold time	t_{H6}		0	–	–	ns
PIO*n* to SC2 setup time	t_{S7}	$V_{TR/\overline{HD}} = V_{IH}$. See figure 7.	30	–	–	ns
PIO*n* to SC2 hold time	t_{H7}		0	–	–	ns
PIO*n* to TR/$\overline{HD}$ setup time	t_{S8}	See figure 8.	20	–	–	ns
PIO*n* to TR/$\overline{HD}$ hold time	t_{H8}		0	–	–	ns
SC1 and SC2 pulsewidth	t_{W1}	See figures 1 and 2.	15	–	–	ns
$\overline{LC1}$ pulsewidth	t_{W2}	See figure 3.	20	–	–	ns

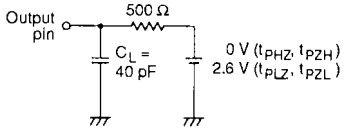
Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
TR/$\overline{HD}$ pulsewidth	t_{W3}	See figure 8.	20	–	–	ns
$\overline{OEP}$ pulsewidth	t_{W4}	See figure 14.	40	–	–	ns
$\overline{OEAC}$ and $\overline{OEBD}$ pulsewidth	t_{W5}	See figure 15.	40	–	–	ns
Clock rise time	t_r	See figures 1 and 2.	–	–	100	ns
Clock fall time	t_f		–	–	100	ns
PIO0 to PIO23 output propagation delay time	t_{PLH1}	See note 1. See figure 9.	–	–	60	ns
	t_{PHL1}		–	–	60	
SIOA and SIOB output propagation delay time	t_{PLH2}	See note 1. See figure 10.	–	–	40	ns
	t_{PHL2}		–	–	40	
SIOC and SIOD output propagation delay time	t_{PLH3}	See note 1. See figure 11.	–	–	40	ns
	t_{PHL3}		–	–	40	
SO1 output propagation delay time	t_{PLH4}	See note 1. See figure 12.	–	–	35	ns
	t_{PHL4}		–	–	35	
SO2 output propagation delay time	t_{PLH5}	See note 1. See figure 13.	–	–	35	ns
	t_{PHL5}		–	–	35	
PIO0 to PIO23 enable propagation delay time	t_{PZL1}	See note 2. See figure 14.	–	–	50	ns
	t_{PZH1}		–	–	50	
PIO0 to PIO23 disable propagation delay time	t_{PLZ1}	See note 2. See figure 14.	–	–	50	ns
	t_{PHZ1}		–	–	50	
SIOA to SIOD enable propagation delay time	t_{PZL2}	See note 2. See figure 15.	–	–	40	ns
	t_{PZH2}		–	–	40	
SIOA to SIOD disable propagation delay time	t_{PLZ2}	See note 2. See figure 15.	–	–	40	ns
	t_{PHZ2}		–	–	40	
Input capacitance	C_{in}	f = 1 MHz	–	–	10	pF
Input/output capacitance	C_{io}	f = 1 MHz, $V_{\overline{OEP}}$ = $V_{\overline{OEAC}}$ = $V_{\overline{OEBD}}$ = V_{IH}	–	–	20	pF

Notes

1. Measurement circuit 1



2. Measurement circuit 2



Timing Characteristics

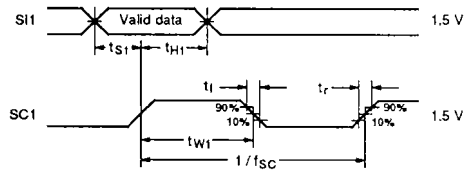


Figure 1.

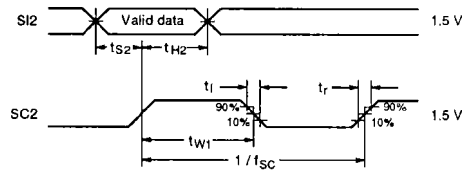


Figure 2.

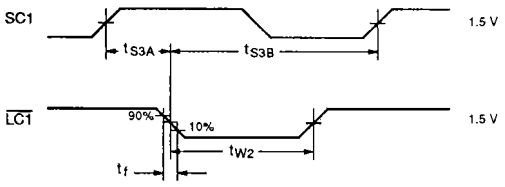


Figure 3.

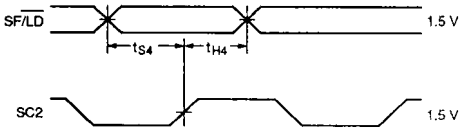
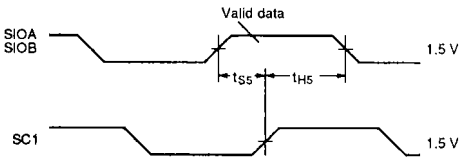


Figure 4.



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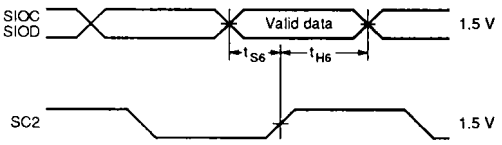
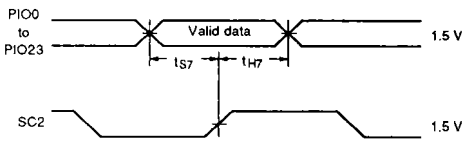


Figure 6.



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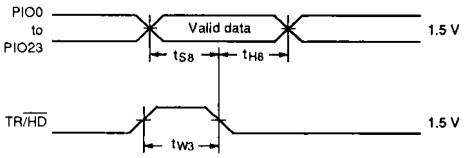


Figure 8.

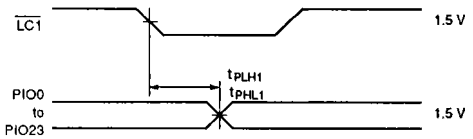


Figure 9.

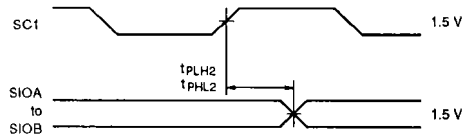


Figure 10.

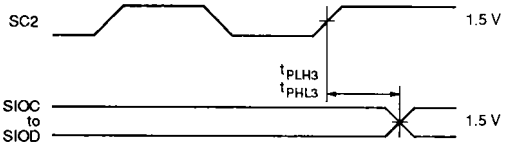


Figure 11.

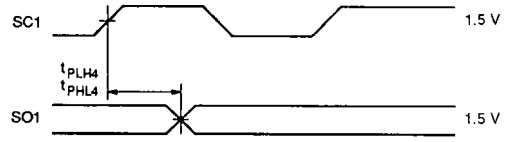


Figure 12.

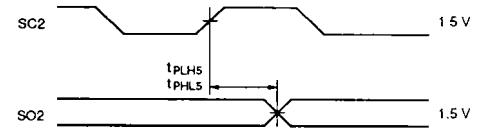


Figure 13.

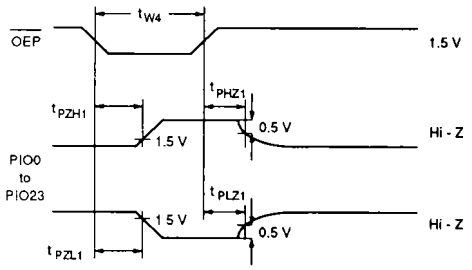


Figure 14.

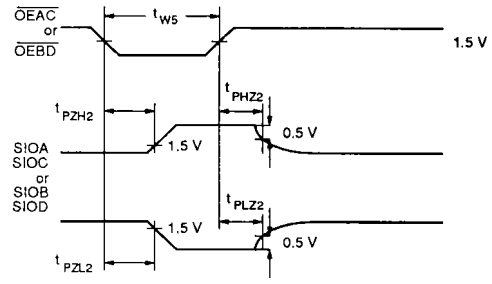


Figure 15.

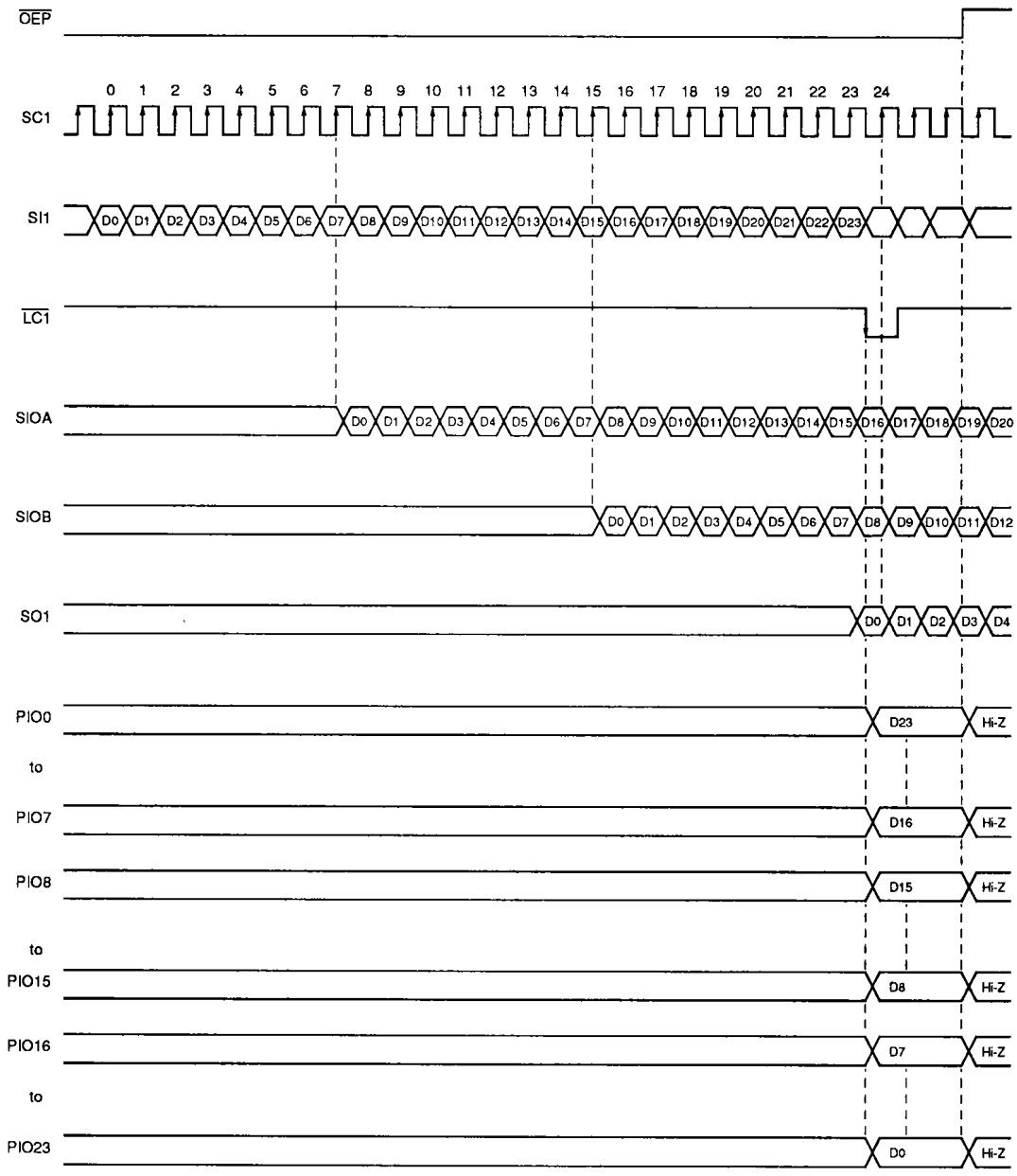


Figure 16. 24-bit SIPO ($\overline{\text{OEAC}}$ = LOW, $\overline{\text{OEBD}}$ = LOW)

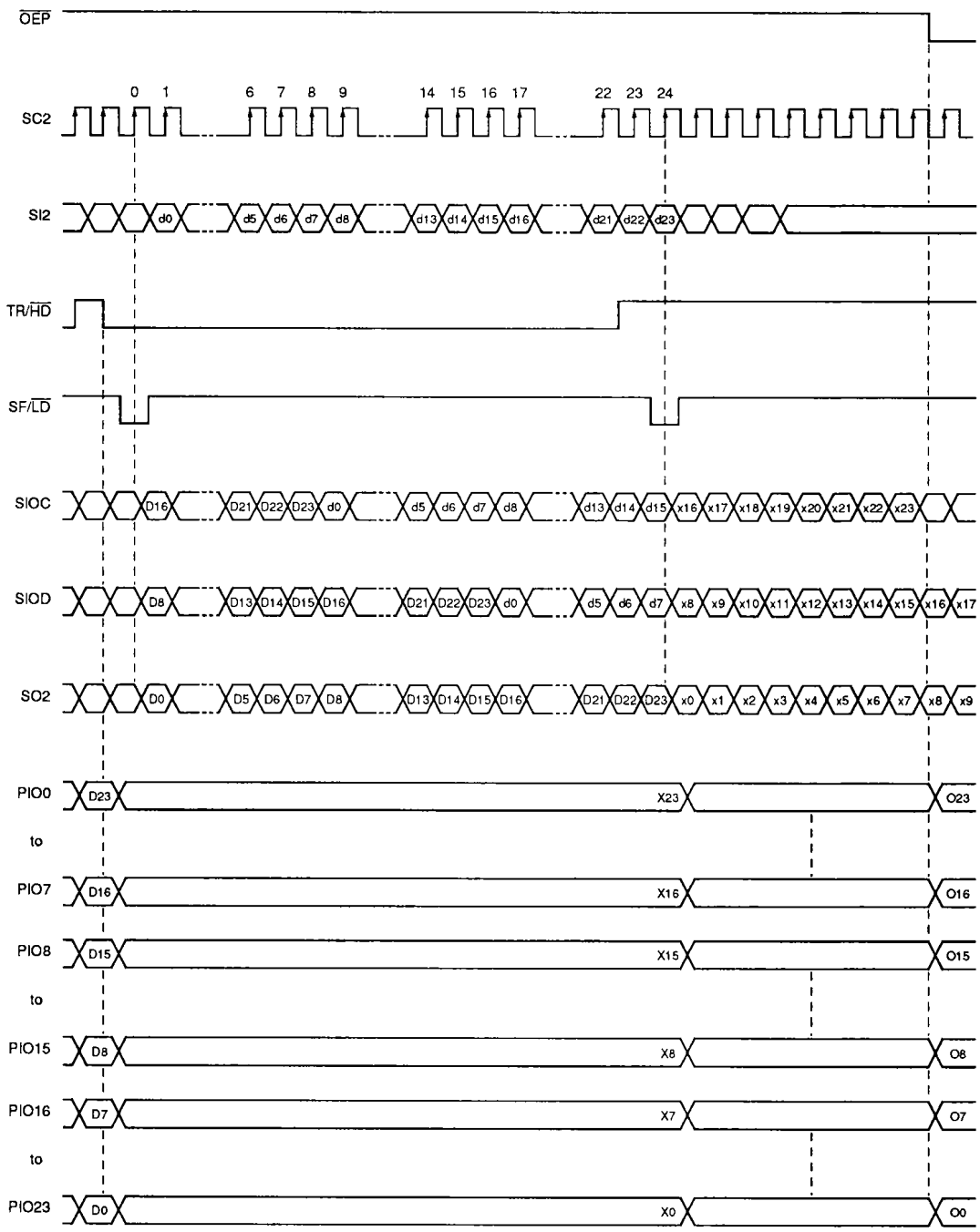


Figure 17. 24-bit PISO ($\overline{\text{OEAC}}$ = LOW, $\overline{\text{OEBD}}$ = LOW)

FUNCTIONAL DESCRIPTION

Serial-to-parallel Converter Mode ($\overline{OEP}$ = LOW)

In this mode, the levels on $\overline{OEAC}$ and $\overline{OEBD}$ define a further four sub-modes. These sub-modes determine the configuration of three 8-bit shift registers making up the serial-to-parallel converter.

Mode name	$\overline{OEAC}$	$\overline{OEBD}$	Function
SPM1	LOW	LOW	1 × (24-bit serial → 24-bit parallel)
SPM2	LOW	HIGH	1 × (16-bit serial → 16-bit parallel) AND 1 × (8-bit serial → 8-bit parallel)
SPM3	HIGH	LOW	1 × (8-bit serial → 8-bit parallel) AND 1 × (16-bit serial → 16-bit parallel)
SPM4	HIGH	HIGH	3 × (8-bit serial → 8-bit parallel)

The mode selected determines which input(s) of SI1, SIOA and SIOB will function as a serial data input. Data is shifted on the rising edge of SC1.

The shift register (SIPO) output data from each SIPO is latched into general-purpose registers in 8-bit units on the falling edge of the data latch clock, $\overline{LC1}$.

Data is output on consecutive outputs from PIO0 up to PIO23, depending on the mode selected.

Parallel-to-serial Converter Mode ($\overline{OEP}$ = HIGH)

In this mode, the levels on $\overline{OEAC}$ and $\overline{OEBD}$ define a further four sub-modes. These sub-modes determine the configuration of three 8-bit shift registers making up the parallel-to-serial converter.

Mode name	$\overline{OEAC}$	$\overline{OEBD}$	Function
PSM1	LOW	LOW	1 × (24-bit parallel → 24-bit serial) OR 3 × (8-bit parallel → 8-bit serial)
PSM2	LOW	HIGH	2 × (8-bit parallel → 8-bit serial)
PSM3	HIGH	LOW	1 × 16-bit parallel → 16-bit serial) OR 2 × (8-bit parallel → 8-bit serial)
PSM4	HIGH	HIGH	1 × (8-bit parallel → 8-bit serial)

The parallel input data is input on consecutive inputs from PIO0 up to PIO23, depending on the mode selected.

Input parallel data is passed directly to the PISO shift registers when TR/$\overline{HD}$ is HIGH (transparent mode). The input data is latched when TR/$\overline{HD}$ goes LOW.

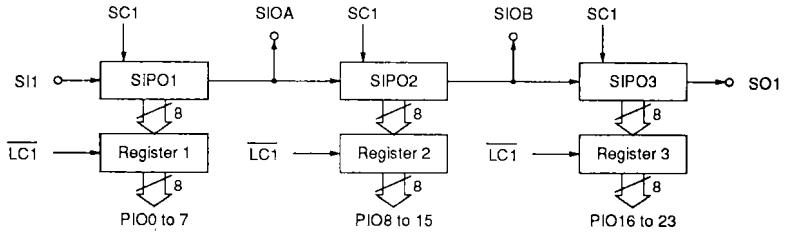
Data is loaded into the PISO registers when SF/$\overline{LD}$ goes LOW, and shifting is enabled when SF/$\overline{LD}$ goes HIGH. Data is shifted in three 8-bit units on the rising edge of the data shift clock, SC2.

The mode selected determines which output(s) of SO2, SIOC and SIOD will function as a serial output.

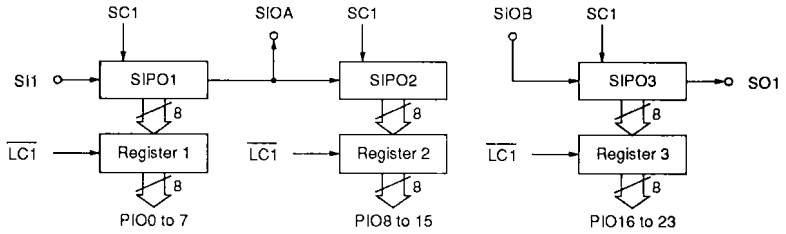
Mode Selection

Serial-to-parallel converter mode ($\overline{OEP}$ = LOW)

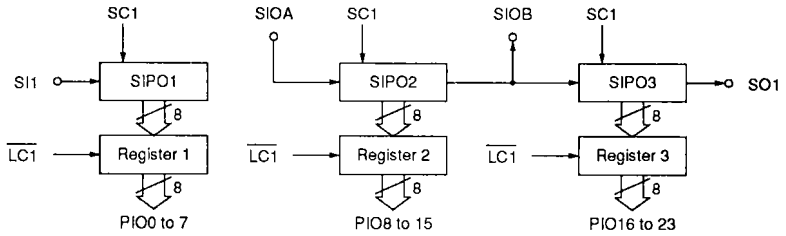
SPM1 ($\overline{OEAC}$ = LOW, $\overline{OEBD}$ = LOW)



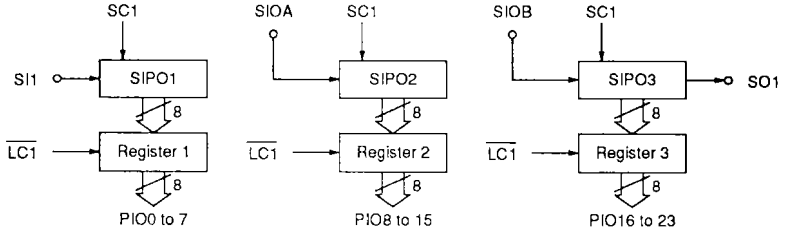
SPM2 ($\overline{OEAC}$ = LOW, $\overline{OEBD}$ = HIGH)



SPM3 ($\overline{OEAC}$ = HIGH, $\overline{OEBD}$ = LOW)

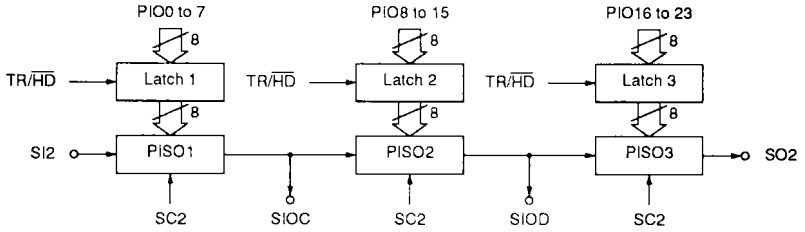


SPM4 ($\overline{OEAC}$ = HIGH, $\overline{OEBD}$ = HIGH)

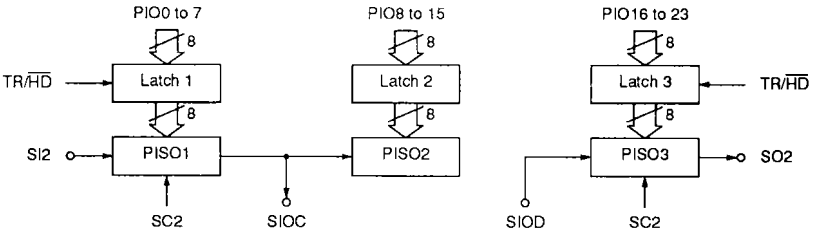


Parallel-to-serial converter mode ($\overline{OEP}$ = HIGH)

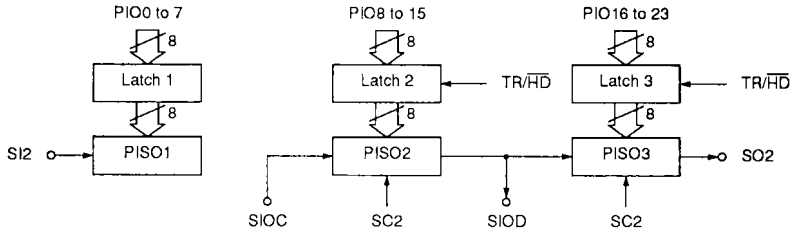
PSM1 ($\overline{OEAC}$ = LOW, $\overline{OEBD}$ = LOW)



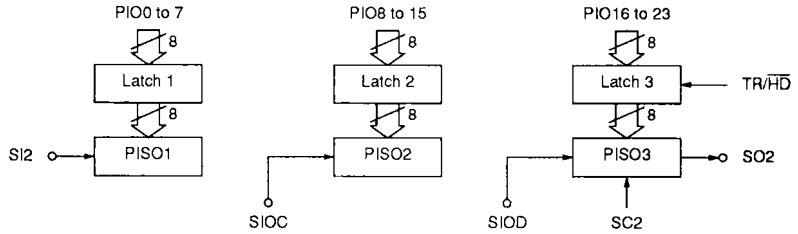
PSM2 ($\overline{OEAC}$ = LOW, $\overline{OEBD}$ = HIGH)



PSM3 ($\overline{OEAC}$ = HIGH, $\overline{OEBD}$ = LOW)

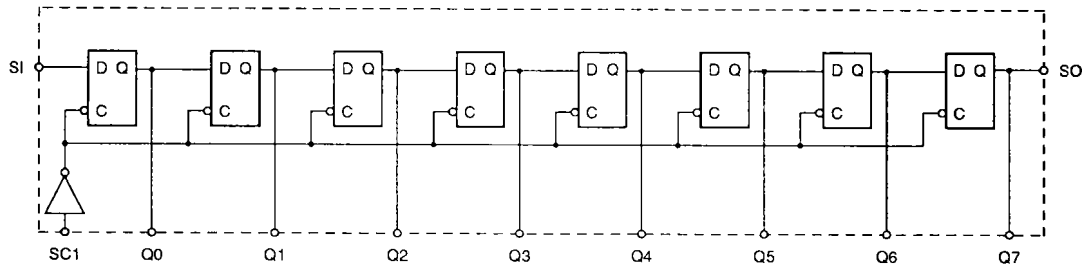


PSM4 ($\overline{OEAC}$ = HIGH, $\overline{OEBD}$ = HIGH)

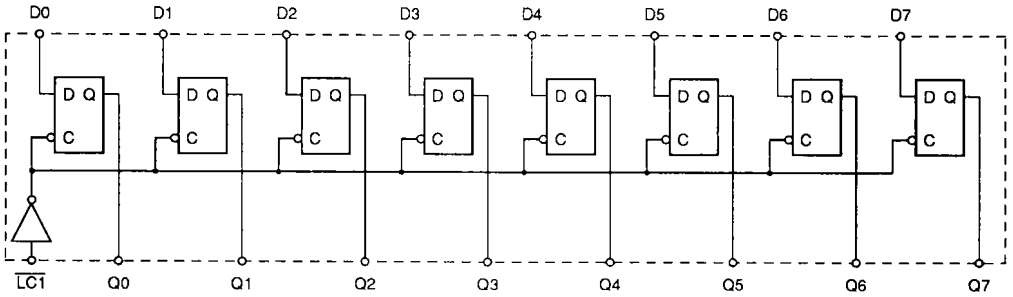


Equivalent Circuits

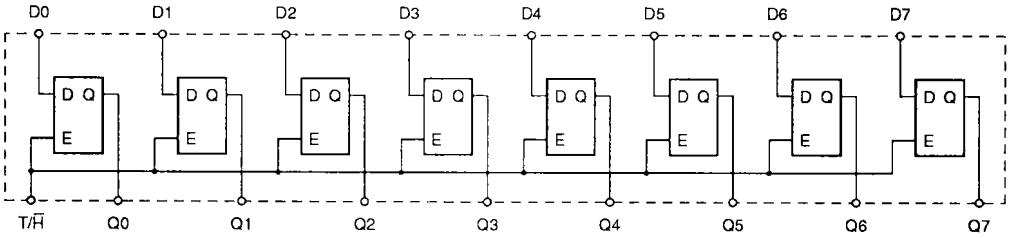
8-bit SIPO



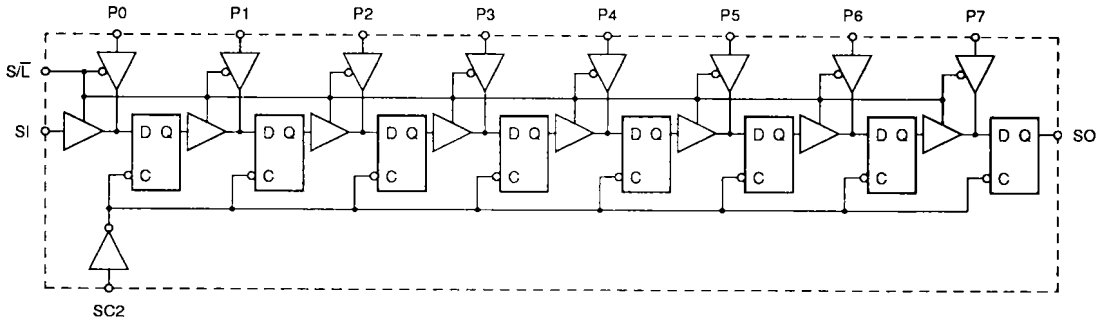
8-bit register



8-bit latch



8-bit PISO



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