OVERVIEW

The SM3320AGA is an image sensor IC with a built-in single picture element (pixel) photodiode of 1mm^2 and programmable signal conditioning circuit. The IC has an optical filter on chip with target condition 585nm±30nm, and it integrates all the elements required for optical sensor into an ultra-miniature package. The signal condition circuit has a programmable gain amplifier with dark current compensation circuit, so that it can operate in wider temperature range. With 3 addressing bits, up to 8 SM3320AGA can be paralleled.

FEATURES

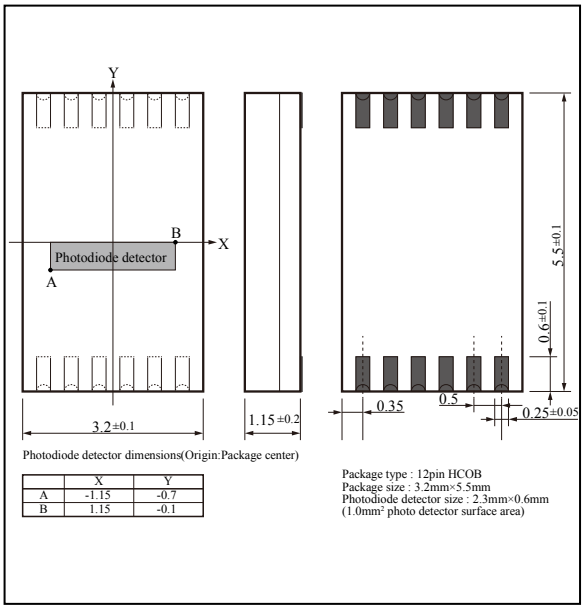
- Optical filter on chip with target condition: 585nm±30nm
- Dark current compensation circuit built-in for stable signal output
- Gain setting and output control function using serial interface (DATA, SE, CLK, OE)
- Connection up to 8 devices in parallel according to 3-bit address setting
- Transimpedance range: 500kΩ to 240MΩ
- Photodiode detector size: 2.3mm×0.6mm (1.0mm^2 photodetector surface area)
- Anti-reflection film coating with little sensitivity changing by wavelength
- Supply voltage range: 2.7 to 5.5V (single supply)
- Current consumption: 1.5mA (typ)@V_{DD}=5V, no load
- Operating temperature range: -40 to +85°C
- Package: 12 pin HCOB

ORDERING INFORMATION

Device	Package
SM3320AGA	12 pin HCOB

PACKAGE DIMENSIONS

(Unit: mm)

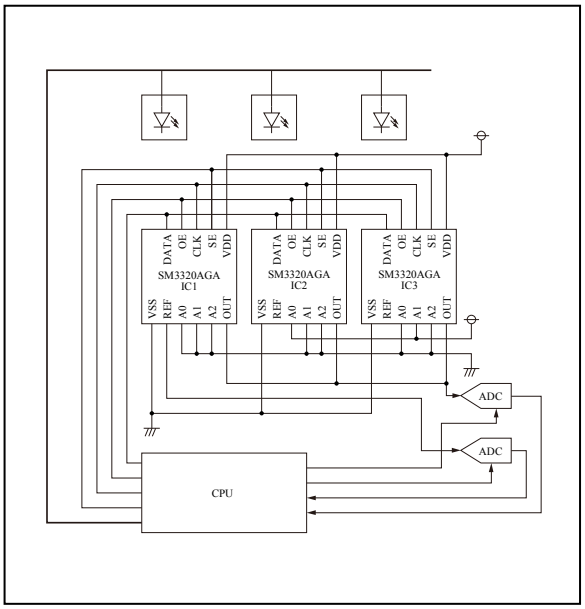


Photodiode detector dimensions(Origin:Package center)

	X	Y
A	-1.15	-0.7
B	1.15	-0.1

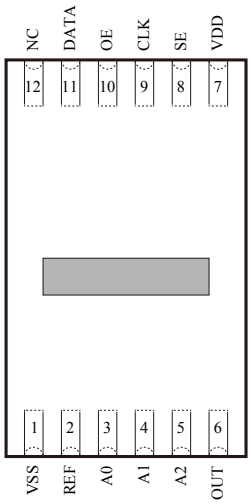
Package type : 12pin HCOB
Package size : 3.2mm×5.5mm
Photodiode detector size : 2.3mm×0.6mm
(1.0mm^2 photo detector surface area)

TYPICAL APPLICATION CIRCUIT



PINOUT

(Top view)

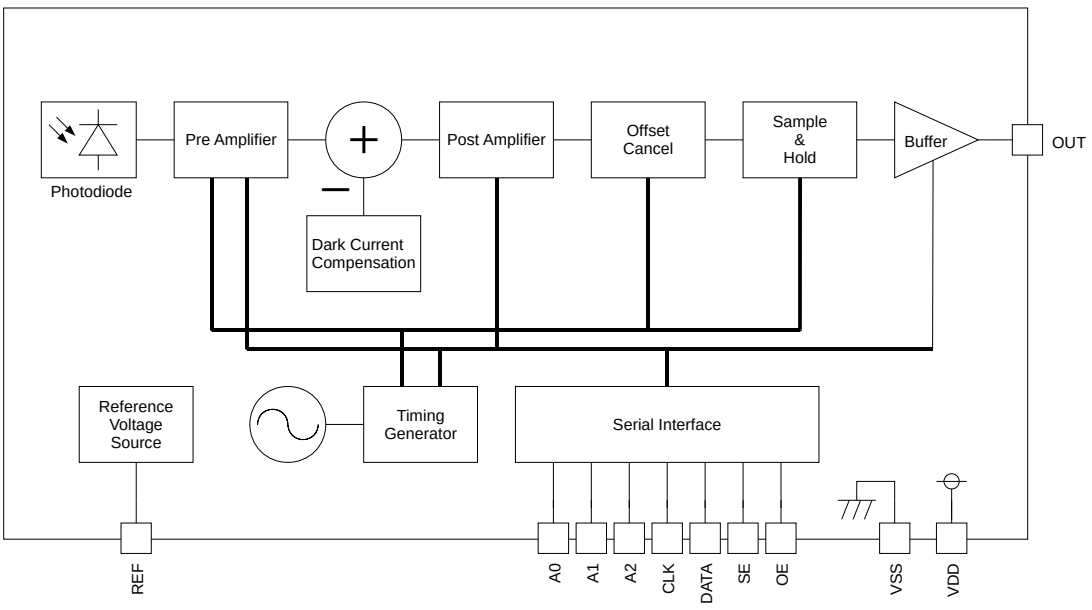


PIN DESCRIPTION

No.	Name	I/O	Description
1	VSS	S	Ground
2	REF	O	Reference voltage
3	A0	I	Address setting input 0
4	A1	I	Address setting input 1
5	A2	I	Address setting input 2
6	OUT	O	Analog output
7	VDD	S	Supply voltage
8	SE	I	Serial I/F enable input
9	CLK	I	Serial I/F clock input
10	OE	I	Output enable control
11	DATA	I/O	Serial I/F data input/output
12	NC	-	Leave open-circuit for normal use

*. I/O: Input/Output pin I: Input pin O: Output pin S: Supply pin

BLOCK DIAGRAM



SPECIFICATIONS

Absolute Maximum Ratings

V_{SS}=0V

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage*1	V_{DD}	VDD pin	-0.3 to +7.0	V
Input voltage*1*2	V_{IN}	DATA, CLK, SE, OE, A0, A1, A2 pins	-0.3 to V_{DD}+0.3	V
Output voltage*1*2	V_{OUT}	OUT, REF pins	-0.3 to V_{DD}+0.3	V
Storage temperature*3	T_{STG}		-55 to +90	°C

*1. These ratings must not be exceeded, not even momentarily. If a rating is exceeded, there is a risk of IC failure, deterioration in characteristics, and decrease in reliability.

*2. V_{DD} is a V_{DD} value of recommended operating conditions.

*3. When stored in nitrogen or vacuum atmosphere applied to IC itself only (excluding packaging materials).

Recommended Operating Conditions

The recommended operating conditions are the conditions for which the electrical characteristics are guaranteed.

VSS=0V

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V_{DD}		2.7	5.0	5.5	V
OUT output load*1			-	-	100	pF
REF output load*1			-	-	100	pF
Operating temperature	T_a		-40	-	85	°C

*1. The output load of the OUT and REF outputs presumes capacitive load only. For current load, an error in the output voltage occurs, so the outputs must be used under high-impedance conditions.

Note. Since it may influence the reliability if it is used out of range of recommended operating conditions, this product should be used within this range.

Electrical Characteristics
DC Characteristics

Recommended operating conditions using reference circuit, unless otherwise noted

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Current consumption	I_{DD}	OE=0V, No output load		-	1.5	3.0	mA
Logic input voltage 1	V_{IH1}	DATA,CLK,SE,A0,A1,A2 pins		$0.8V_{DD}$	-	-	V
	V_{IL1}			-	-	$0.2V_{DD}$	
Logic input voltage 2	V_{IH2}	OE pin		$0.8V_{DD}$	-	-	V
	V_{IL2}			-	-	$0.2V_{DD}$	
Logic input current 1	I_{IH1}	DATA,CLK,SE,	$V_{IH}=V_{DD}$	-	-	1	µA
	I_{IL1}	A0,A1,A2,pins	$V_{IL}=0V$	-1	-	-	
Logic input current 2	I_{IH2}	OE pin,	$V_{IH}=V_{DD}$	-	10	20	µA
	I_{IL2}	V_{DD}=5.0V	$V_{IL}=0V$	-20	-10	-	
Logic output impedance	Z_{DATA}	DATA pin, read mode		-	-	400	Ω
REF output voltage	V_{REF}	Load capacitance < 100pF*1		$0.08V_{DD}$	$0.10V_{DD}$	$0.12V_{DD}$	V
OUT maximum output voltage	$V_{OUT}H$			$0.65V_{DD}$	$0.70V_{DD}$	-	V
Output impedance	Z_O	OUT pin*2		-	400	1000	Ω

*1. If a large load capacitance is connected to REF, the REF voltage may begin to oscillate. Accordingly, the load capacitance connected to the REF output should be 100pF or lower.

*2. The output impedance Z_O is given by the following equation, where V10 is the output voltage for 10kΩ load resistance and V0 is the output voltage with no load.

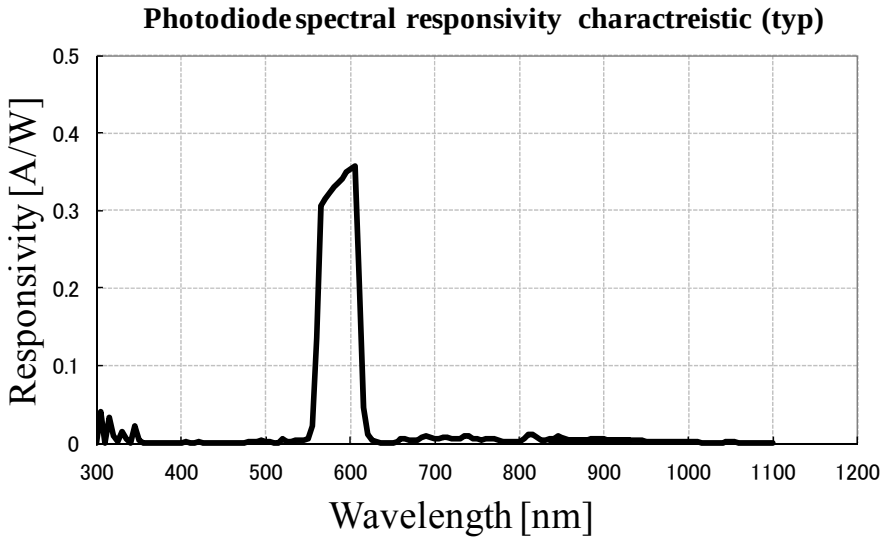
$$Z_O = (V0/V10 - 1)*10 \quad [k\Omega]$$

Photodiode Characteristics

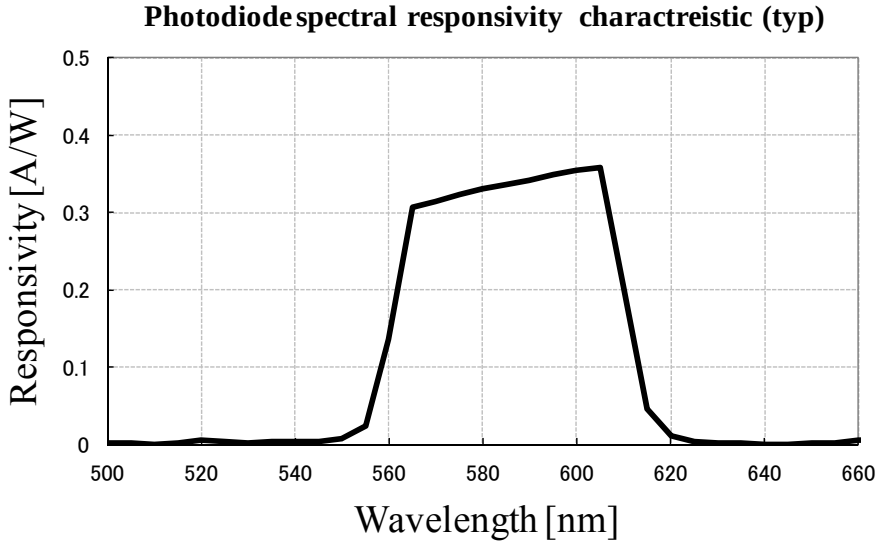
Recommended operating conditions using reference circuit, unless otherwise noted.

Parameter*1	Symbol	Conditions	MIN	TYP	MAX	Unit
Photodetector sensitivity 1*1	S1/S4	470nm	-	-	20	%
Photodetector sensitivity 2*1	S2/S4	525nm	-	-	30	%
Photodetector sensitivity 3*1	S3/S4	545nm	-	-	60	%
Photodetector sensitivity 4*1	S4	590nm	0.23	0.33	-	A/W
Photodetector sensitivity 5*1	S5/S4	630nm	-	-	60	%
Photodetector sensitivity 6*1	S6/S4	870nm	-	-	30	%

*1. Typical characteristics determined on standalone device.



Photodiode spectral responsivity



Photodiode spectral responsivity (500nm~680nm)

Analog Electrical Characteristics

Recommended operating conditions using reference circuit, unless otherwise noted.

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Preamplifier transimpedance*1		CS[00]	TS[00]	-	0.5	-	MΩ
		CS[01]		-	1.0	-	MΩ
		CS[10]		-	2.0	-	MΩ
		CS[11]		-	4.0	-	MΩ
		CS[00]	TS[01]	-	1.5	-	MΩ
		CS[01]			3.0	-	MΩ
		CS[10]		-	6.0	-	MΩ
		CS[11]		-	12.0	-	MΩ
		CS[00]	TS[10]	-	3.5	-	MΩ
		CS[01]		-	7.0	-	MΩ
		CS[10]		-	14.0	-	MΩ
		CS[11]		-	28.0	-	MΩ
		CS[00]	TS[11]	-	7.5	-	MΩ
		CS[01]		-	15.0	-	MΩ
		CS[10]		-	30.0	-	MΩ
		CS[11]		-	60.0	-	MΩ
Preamplifier conversion time		TS[00]		-	20	30	μs
		TS[01]		-	40	60	μs
		TS[10]		-	80	120	μs
		TS[11]		-	160	240	μs
Postamplifier gain error				-	-	±1	dB
Dark voltage		REF reference, [01111111] below		-40	-	40	mV
		REF reference, [11111111] below		-40	-	40	mV

*1. Design value: Preamplifier transimpedance is determined by specifying the preamplifier feedback capacitance (CS[1:0]) and preamplifier conversion time (TS[1:0]). This is a virtual impedance called the preamplifier transimpedance. The preamplifier transimpedance (Rti) is calculated using the following equation.

$$Rti = \frac{(\text{Preamplifier conversion time} - 10\mu\text{sec})}{\text{Preamplifier feedback capacitance}}$$

The sample and hold circuit is synchronized to the preamplifier conversion time. To determine the output voltage, the sample and hold circuit must complete one full cycle after photoirradiation. The photoirradiation time should be set to a value equal to or greater than the detection time (double the maximum preamplifier conversion time) + analog output capture time. If photoirradiation ends before analog output capture, the output voltage may drop or fall to zero. Photoirradiation should be continuous until analog output capture is completed.

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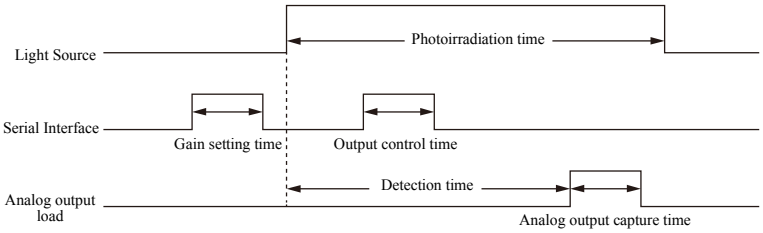


Preamplifier conversion time	TS[00]	TS[01]	TS[10]	TS[11]
Detection time	≥60μs	≥120μs	≥240μs	≥480μs

Output voltage = V_{REF} + (Rti × Photodiode photocurrent × Postamplifier gain)

AC Characteristics

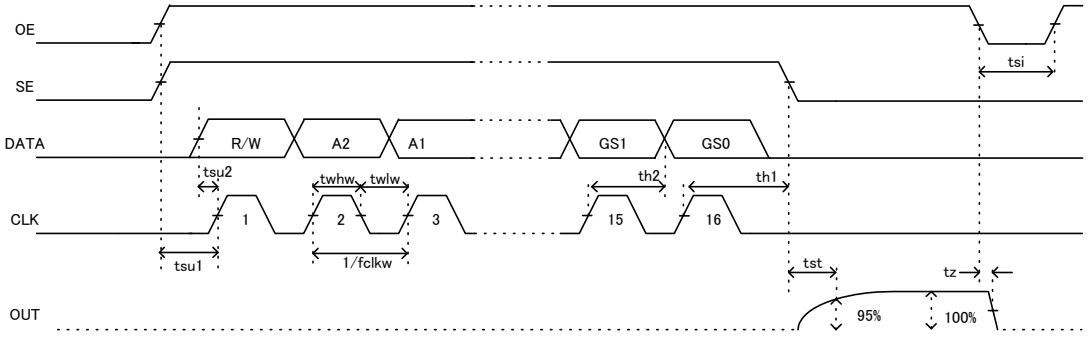
Data Write Mode

Recommended operating conditions using reference circuit, unless otherwise noted.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Write clock LOW-level pulse width	twlw	CLK pin	40	-	-	ns
Write clock HIGH-level pulse width	twhw	CLK pin	40	-	-	ns
Data setup time 1	tsu1	Between SE-CLK	40	-	-	ns
Data setup time 2	tsu2	Between DATA-CLK	40	-	-	ns
Data hold time 1	th1	Between SE-CLK	140	-	-	ns
Data hold time 2	th2	Between DATA-CLK	40	-	-	ns
Write clock frequency	fclkw		-	-	10	MHz
Settling time	tst	OUT pin, 100pF load, 1V output amplitude variation, time to reach 95% level	-	-	2	µs
Output disable time*1	tz	OUT pin	-	0.1	-	µs
Input capacitance*2	C_I	SE,OE,CLK,DATA pins	-	5	-	pF
Output capacitance*2	C_O	OUT pin	-	5	-	pF
Interface wait time	tsi		100	-	-	ns

*1. Design value: Provided as a measure for the output control time.
*2. Design value: Indicates the terminal capacitance per pin. Provided as a guide for when designing the circuit board.

LOW/HIGH-level switch timing measured with respect to $0.5V_{DD}$ reference level, unless otherwise noted.

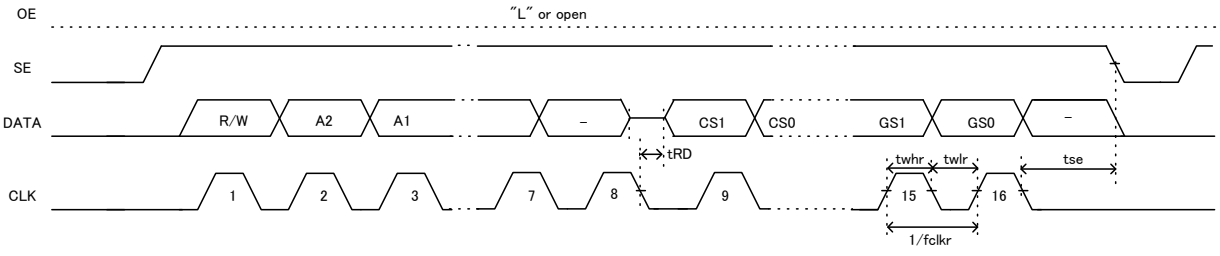


Data Read Mode

Recommended operating conditions using reference circuit, unless otherwise noted.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Read clock LOW-level pulse width	twlr	CLK pin	500	-	-	ns
Read clock HIGH-level pulse width	twhr	CLK pin	500	-	-	ns
Read clock frequency	fclkr		-	-	1	MHz
SE hold time	tse	Between SE-CLK	500	-	-	ns
Read-out data delay time	tRD	DATA pin, load capacitance=100pF	-	-	400	ns

LOW/HIGH-level switch timing measured with respect to $0.5V_{DD}$ reference level, unless otherwise noted.



FUNCTIONAL DESCRIPTION

Basic Function

The SM3320AGA detects the current generated from a photodiode and outputs a voltage signal.

The transimpedance of the preamplifier can be adjusted for coarse adjustment of the responsivity. The transimpedance adjustment range is 0.5 to 60MΩ, set using 4 adjustment bits. Also, a dark current compensation circuit is used to compensate photodiode output under dark lighting conditions for output voltage stability with low temperature variation.

The gain of the postamplifier can be adjusted for fine adjustment of the responsivity. The gain adjustment range is 1 to 4 times, set using 4 adjustment bits. Also, a built-in offset cancel circuit is used to provide low offset voltage at the output.

The output voltage when there is no photoirradiation, called the dark voltage, is $0.1V_{DD}$. The maximum output voltage with photoirradiation is $0.7V_{DD}$.

The device can be addressed using address pin control. This function allows the transimpedance and gain settings to be adjusted for each device independently when multiple devices are connected in parallel. An output enable control (OE) is used for output control.

[Address and A[2:0] setting]

Address	A2 setting	A1 setting	A0 setting
[000]	VSS	VSS	VSS
[001]	VSS	VSS	VDD
[010]	VSS	VDD	VSS
[011]	VSS	VDD	VDD
[100]	VDD	VSS	VSS
[101]	VDD	VSS	VDD
[110]	VDD	VDD	VSS
[111]	VDD	VDD	VDD

Serial Interface

The SM3320AGA use a 3-wire serial interface (SE, CLK, DATA) to access the device and to set an internal register to control device operation. Note that extraneous signal input on the serial interface pins must be avoided when not reading/writing data to the device to prevent incorrect operation.

Internal Register Structure

The device read/write mode, address, operating mode, preamplifier transimpedance, and postamplifier gain are set in an internal register.

The device can be accessed for writing data to or reading data from the register when the A[2:0] address write data bits match the setting of the address control inputs (A2 to A0).

Note that register data must be configured before using the device.

	Address			Data											
RW	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R/W	address			Don't care				Preamplifier transimpedance				Postamplifier gain			
								Feedback capacitance		Conversion time					
				-	-	-	-	CS1	CS0	TS1	TS0	GS3	GS2	GS1	GS0

(1) RW

Read/Write mode set bit. Set to "1" for read mode, and to "0" for write mode.

(2) Address A[2:0] (A2 to A0)

Address bits.

(3) Preamplifier transimpedance CS[1:0] (D7 to D6) and TS[1:0] (D5 to D4)

Preamplifier transimpedance setting bits

(4) Postamplifier gain GS[3:0] (D3 to D0)

Postamplifier gain setting bits

[Adjustment bit assignment]

	Preamplifier feedback capacitance		Capacitance (pF)
CS[1:0]	CS1	CS0	
	0	0	20.0
	0	1	10.0
	1	0	5.0
	1	1	2.5

	Preamplifier conversion time		Time (µs)
TS[1:0]	TS1	TS0	
	0	0	20
	0	1	40
	1	0	80
	1	1	160

	Postamplifier gain				Gain (times)
	GS3	GS2	GS1	GS0	
GS[3:0]	0	0	0	0	1.00
	0	0	0	1	1.08
	0	0	1	0	1.17
	0	0	1	1	1.27
	0	1	0	0	1.38
	0	1	0	1	1.50
	0	1	1	0	1.63
	0	1	1	1	1.78
	1	0	0	0	1.94
	1	0	0	1	2.13
	1	0	1	0	2.33
	1	0	1	1	2.57
	1	1	0	0	2.85
	1	1	0	1	3.17
	1	1	1	0	3.55
	1	1	1	1	4.00

OUT pin Control

The OUT pin is controlled by the level of the OE control pin.

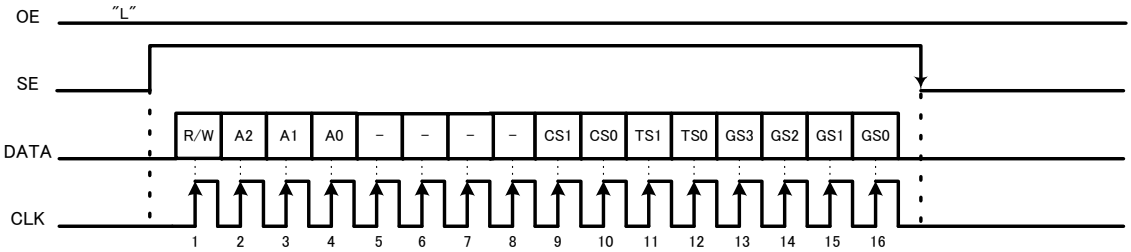
OE pin	OUT pin	Conditions
$\geq 0.8V_{DD}$	Output enable	Normal operation output when A[2:0] write data matches the setting of the address control inputs.
Open	Output enable	Normal operation output
$\leq 0.2V_{DD}$	Output disable	

Gain Setting (register write mode, OE = LOW or open-circuit)

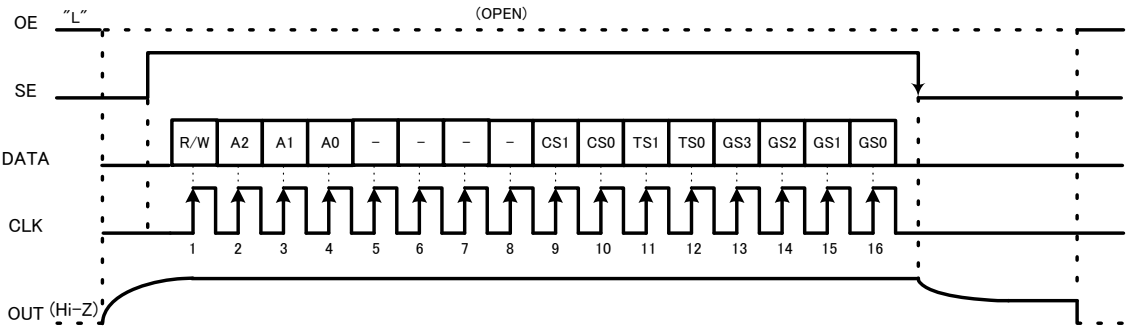
If OE is LOW or open circuit, serial interface operation starts when SE goes HIGH.

Write data comprises 1 read/write mode bit (write mode = 0), 3 address bits, and 12 write data bits transferred in sequence. If the address data bits match the address control pin settings (meaning the device is addressed), the write data is loaded into the register, and the write data becomes valid and serial interface operation ends when SE goes LOW. Note that data will be corrupted if there are less than or more than 16 clock pulses received during serial data transfer.

Register write (when OE is LOW)



Register write (when OE is open-circuit)



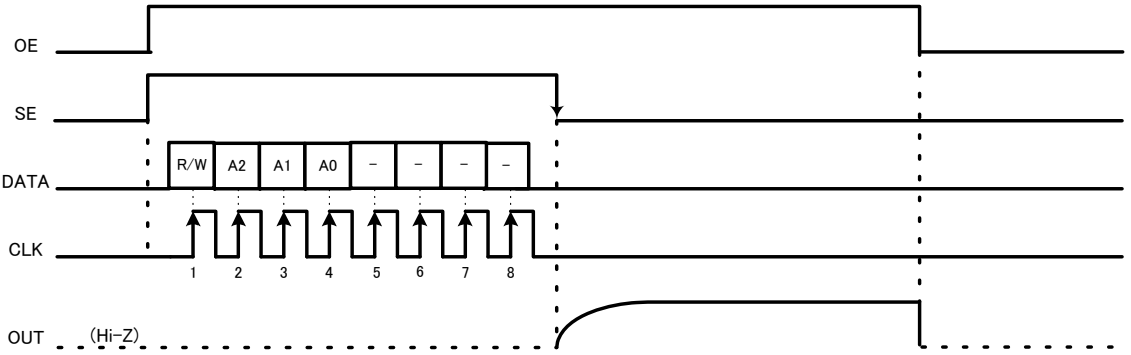
Analog Output Control (register write mode, OE = HIGH)

If OE is HIGH, serial interface operation starts when SE goes HIGH.

Write data comprises 1 read/write mode bit (write mode = 0), 3 address bits, and 4 dummy data bits transferred in sequence. The address data becomes valid and serial interface operation ends when SE goes LOW. If the address data bits match the address control pin settings (meaning the device is addressed), the output is enabled. If the output was already enabled and the address data does not match the address pin settings, the output is disabled. Note that if there are less than or more than 8 clock pulses received during serial data transfer, an address mismatch occurs and the output is disabled.

In addition, sequential write cycles to the register are permitted while OE is HIGH.

Register write (when OE is HIGH)

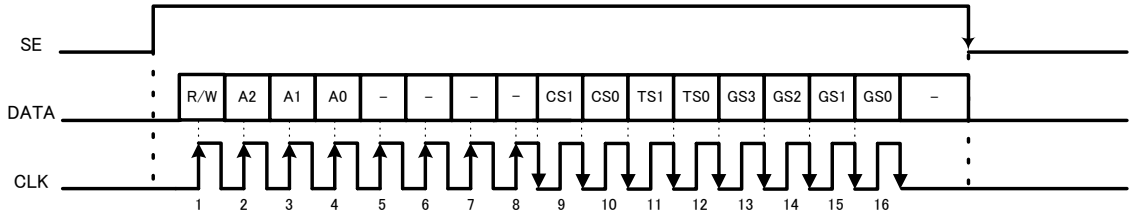


Reading Data from the Register (OE = LOW or open-circuit)

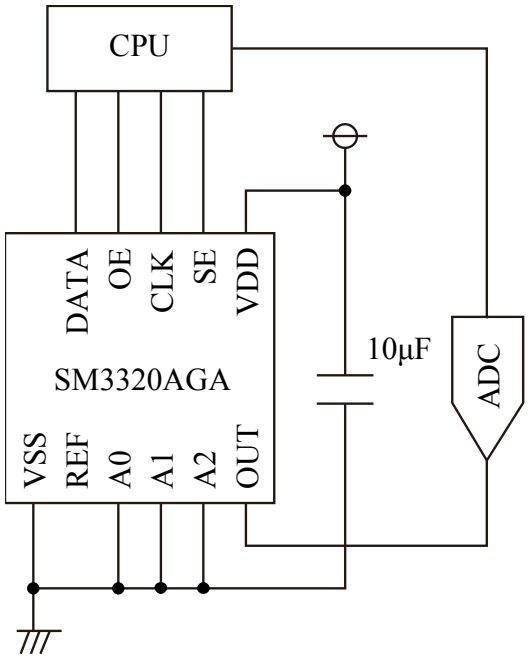
Serial interface operation starts when SE goes HIGH.

Read data comprises 1 read/write mode bit (read mode = 1), 3 address bits, and 4 dummy data bits transferred in sequence when OE is open-circuit or goes LOW. The address control pin setting is compared with the address register setting on the falling edge of the 8th CLK pulse. If the settings match (meaning the device is addressed), the data in the 8-bit analog adjustment code register is read out in sequence. On the serial interface, the GS0 data bit is transferred on the 15th falling edge of CLK, and then any data bits transferred between the 16th falling edge of CLK and the falling edge on SE are undefined data. Serial interface operation ends when SE goes LOW, and the DATA terminal reverts to an input. Make sure there are not less than nor more than 16 input pulses on the CLK clock. If the number of clock pulses is incorrect, incorrect data may be written to the register or read from the register.

Register read



REFERENCE CIRCUIT



Device with [000] address setting

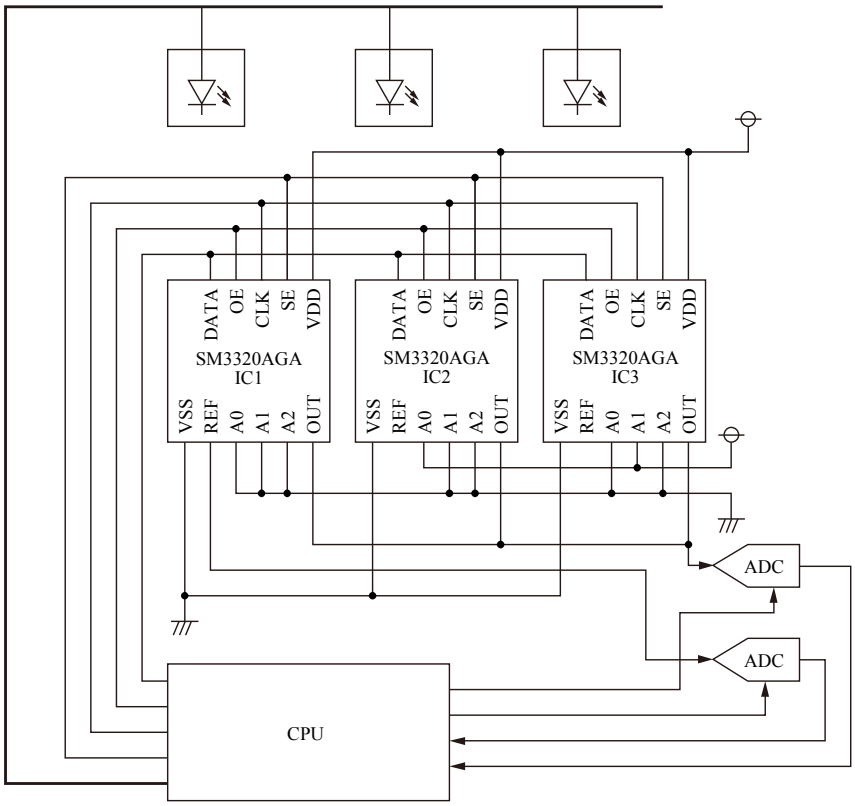
Connect a laminated ceramic capacitor of 10µF or larger as close as possible to the supply voltage terminals.

The nominal value rating for each electrical characteristics parameter is measured using the reference circuit.

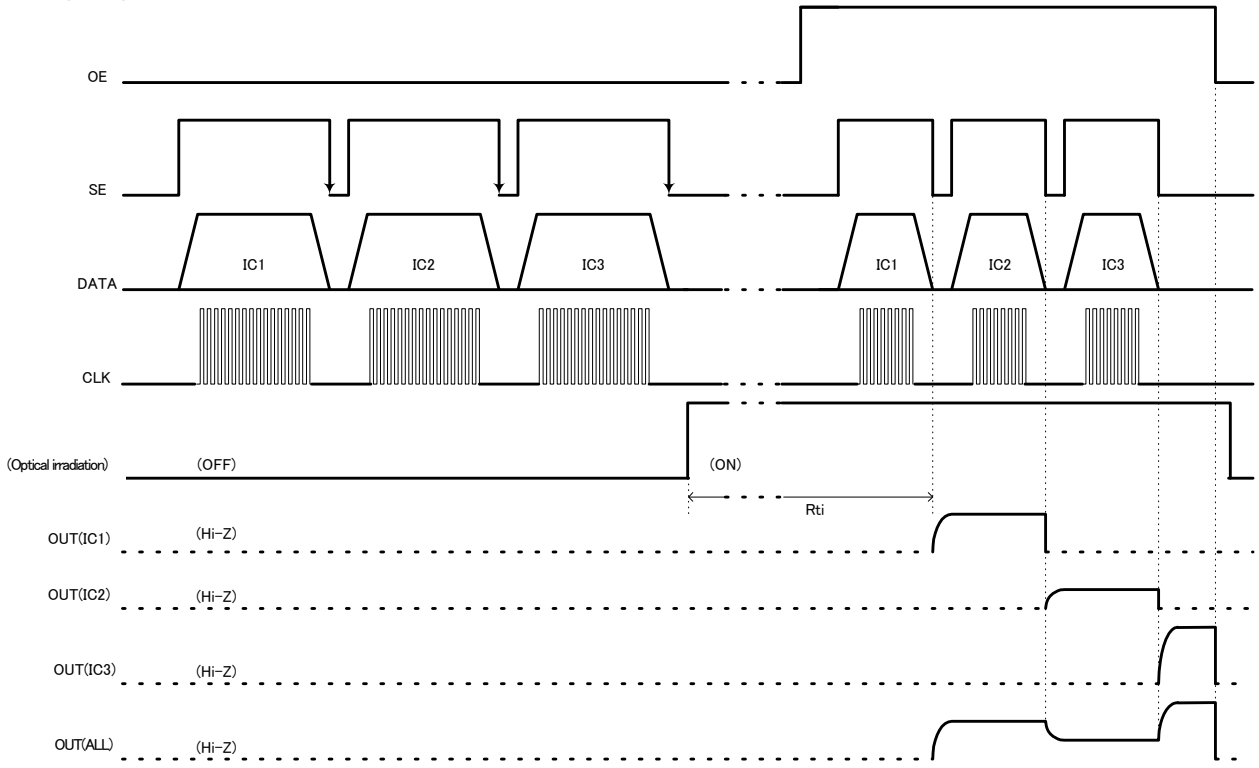
TYPICAL APPLICATION CIRCUITS

The typical application circuits are provided for reference only, and do not represent a guarantee of circuit operation. We accept no liability for any damage resulting from the use of these circuits. Always use devices after sufficient evaluation under actual operating conditions.

Circuit 1

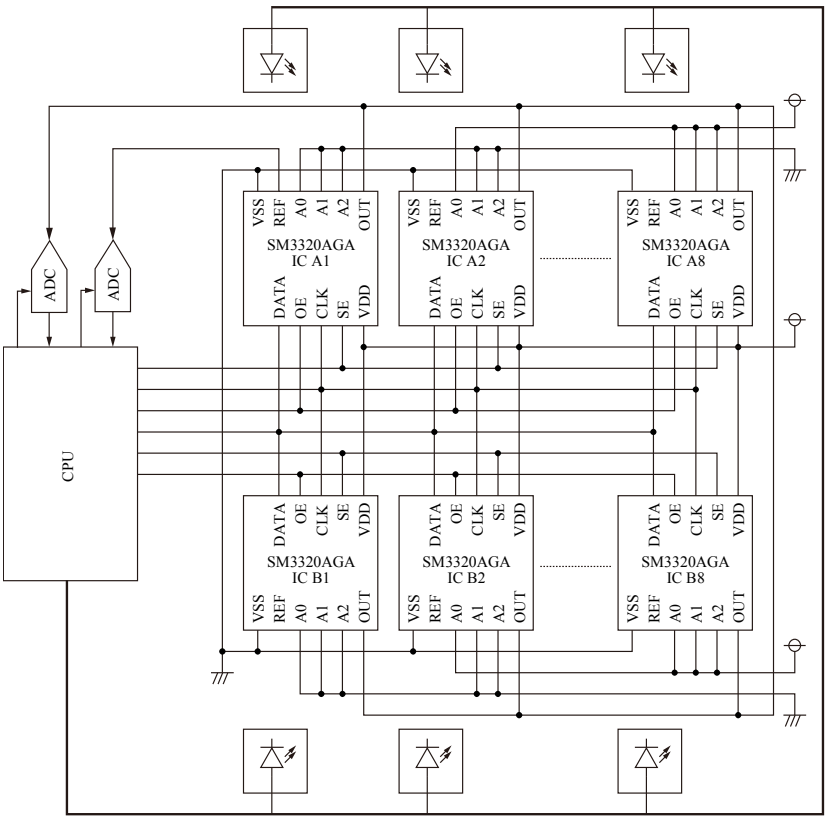


Timing Diagram

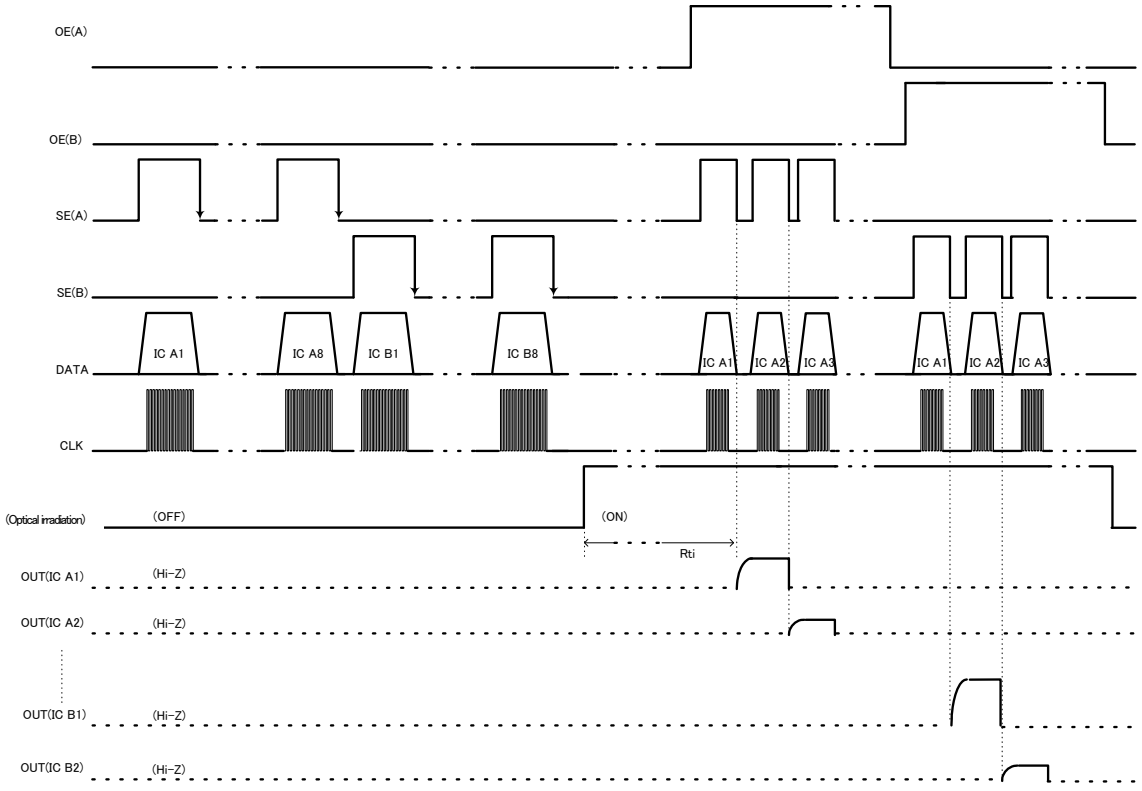


Circuit 2

Example with 9 or more devices connected in parallel



Timing Diagram



Please pay your attention to the following points at time of using the products shown in this document.

1. The products shown in this document (hereinafter ”Products”) are designed and manufactured to the generally accepted standards of reliability as expected for use in general electronic and electrical equipment, such as personal equipment, machine tools and measurement equipment. The Products are not designed and manufactured to be used in any other special equipment requiring extremely high level of reliability and safety, such as aerospace equipment, nuclear power control equipment, medical equipment, transportation equipment, disaster prevention equipment, security equipment. The Products are not designed and manufactured to be used for the apparatus that exerts harmful influence on the human lives due to the defects, failure or malfunction of the Products.
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