



## General Description

Silego SLG7NT4375 is a low power and small form device. The SoC is housed in a 1.6 x 1.6 mm STQFN package which is optimal for using with small devices.

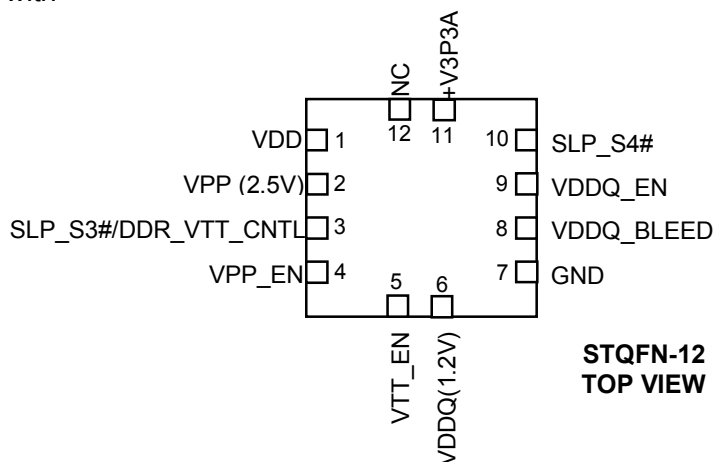
## Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-12 Package
- MSL “1”

## Output Summary

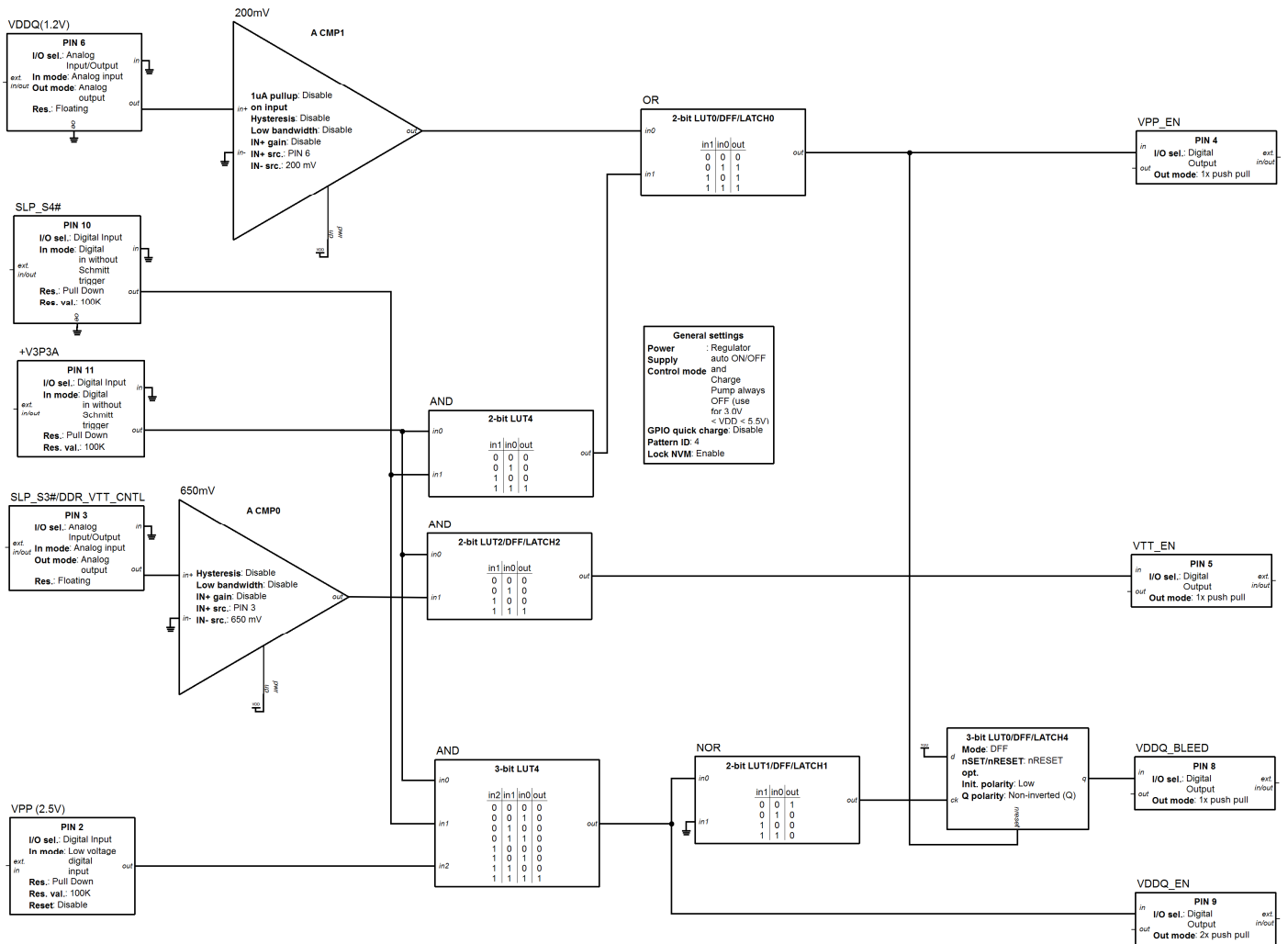
- 3 Outputs — Push Pull 1X
- 1 Output — Push Pull 2X

## Pin Configuration





### Block Diagram





### Pin Configuration

| Pin # | Pin Name             | Type                | Pin Description                       |
|-------|----------------------|---------------------|---------------------------------------|
| 1     | VDD                  | PWR                 | Supply Voltage                        |
| 2     | VPP (2.5V)           | Digital Input       | Low Voltage Digital input             |
| 3     | SLP_S3#/DDR_VTT_CNTL | Analog Input/Output | Analog Input/Output                   |
| 4     | VPP_EN               | Digital Output      | Push Pull 1X                          |
| 5     | VTT_EN               | Digital Output      | Push Pull 1X                          |
| 6     | VDDQ(1.2V)           | Analog Input/Output | Analog Input/Output                   |
| 7     | GND                  | GND                 | Ground                                |
| 8     | VDDQ_BLEED           | Digital Output      | Push Pull 1X                          |
| 9     | VDDQ_EN              | Digital Output      | Push Pull 2X                          |
| 10    | SLP_S4#              | Digital Input       | Digital Input without Schmitt trigger |
| 11    | +V3P3A               | Digital Input       | Digital Input without Schmitt trigger |
| 12    | NC                   | --                  | Keep Floating or Connect to GND       |

### Ordering Information

| Part Number   | Package Type                        |
|---------------|-------------------------------------|
| SLG7NT4375V   | V=STQFN-12                          |
| SLG7NT4375VTR | STQFN-12 – Tape and Reel (3k units) |



### Absolute Maximum Conditions

| Parameter                 | Min. | Max. | Unit |
|---------------------------|------|------|------|
| V <sub>HIGH</sub> to GND  | -0.3 | 7    | V    |
| Voltage at input pins     | -0.3 | 7    | V    |
| Current at input pin      | -1.0 | 1.0  | mA   |
| Storage temperature range | -65  | 150  | °C   |
| Junction temperature      | --   | 150  | °C   |

### Electrical Characteristics

(@ 25°C, unless otherwise stated)

| Symbol             | Parameter                                                  | Condition/Note                                                                      | Min.  | Typ.  | Max. | Unit |
|--------------------|------------------------------------------------------------|-------------------------------------------------------------------------------------|-------|-------|------|------|
| V <sub>DD</sub>    | Supply Voltage                                             |                                                                                     | 3     | 3.3   | 3.6  | V    |
| T <sub>A</sub>     | Operating Temperature                                      |                                                                                     | -40   | 25    | 85   | °C   |
| I <sub>Q</sub>     | Quiescent Current                                          | Static inputs and outputs                                                           | --    | 70    | --   | μA   |
| V <sub>O</sub>     | Maximal Voltage Applied to any PIN in High-Impedance State |                                                                                     | --    | --    | VDD  | V    |
| I <sub>O</sub>     | Maximal Average or DC Current                              | Per Each Chip Side                                                                  | --    | --    | 90   | mA   |
| V <sub>IH</sub>    | HIGH-Level Input Voltage                                   | Logic Input, at VDD=3.3V                                                            | 1.4   | --    | VDD  | V    |
|                    |                                                            | Low-Level Logic Input, at VDD=3.3V                                                  | 0.91  | --    | VDD  |      |
| V <sub>IL</sub>    | LOW-Level Input Voltage                                    | Logic Input, at VDD=3.3V                                                            | --    | --    | 1.65 | V    |
|                    |                                                            | Low-Level Logic Input, at VDD=3.3V                                                  | --    | --    | 0.95 |      |
| I <sub>IH</sub>    | HIGH-Level Input Current                                   | Logic Input PINs; V <sub>IN</sub> = VDD                                             | -1.0  | --    | 1.0  | μA   |
| I <sub>IL</sub>    | LOW-Level Input Current                                    | Logic Input PINs; V <sub>IN</sub> = 0V                                              | -1.0  | --    | 1.0  | μA   |
| V <sub>OH</sub>    | HIGH-Level Output Voltage                                  | Push Pull, I <sub>OH</sub> = 3mA, 1X Driver, at VDD=3.3 V                           | 2.73  | 3.13  | --   | V    |
|                    |                                                            | Push Pull, I <sub>OH</sub> = 3mA, 2X Driver, at VDD=3.3 V                           | 2.87  | 3.22  | --   |      |
| V <sub>OL</sub>    | LOW-Level Output Voltage                                   | Push Pull, I <sub>OL</sub> = 3mA, 1X Driver, at VDD=3.3 V                           | --    | 0.15  | 0.28 | V    |
|                    |                                                            | Push Pull, I <sub>OL</sub> = 3mA, 2X Driver, at VDD=3.3 V                           | --    | 0.07  | 0.13 |      |
| I <sub>OH</sub>    | HIGH-Level Output Current                                  | Push Pull & PMOS OD, V <sub>OH</sub> = 2.4 V, 1X Driver, at VDD=3.3 V               | 6.01  | 12.07 | --   | mA   |
|                    |                                                            | Push Pull & PMOS OD, V <sub>OH</sub> = 2.4 V, 2X Driver, at VDD=3.3 V               | 12.01 | 24.13 | --   |      |
| I <sub>OL</sub>    | LOW-Level Output Current                                   | Push Pull, V <sub>OL</sub> = 0.4V, 1X Driver, at VDD=3.3 V                          | 4.06  | 6.92  | --   | mA   |
|                    |                                                            | Push Pull, V <sub>OL</sub> = 0.4V, 2X Driver, at VDD=3.3 V                          | 8.13  | 13.84 | --   |      |
| V <sub>ACMP0</sub> | Analog Comparator Threshold Voltage                        | ACMP0 threshold including input offset, reference voltage variation and hysteresis. | 620   | --    | 677  | mV   |
| V <sub>ACMP1</sub> | Analog Comparator Threshold Voltage                        | ACMP1 threshold including input offset, reference voltage variation and hysteresis. | 186   | --    | 214  | mV   |
| T <sub>SU</sub>    | Start up Time                                              | From VDD rising past 1.6V                                                           | --    | 1     | --   | ms   |



### Functionality Waveforms

Channel 1 (yellow/top line) – PIN#3 (SLP\_S3#/DDR\_VTT\_CNTL)

Channel 2 (light blue/2nd line) – PIN#6 (VDDQ(1.2V))

D0 – PIN#2 (VPP (2.5V))

D1 – PIN#11 (+V3P3A)

D2 – PIN#10 (SLP\_S4#)

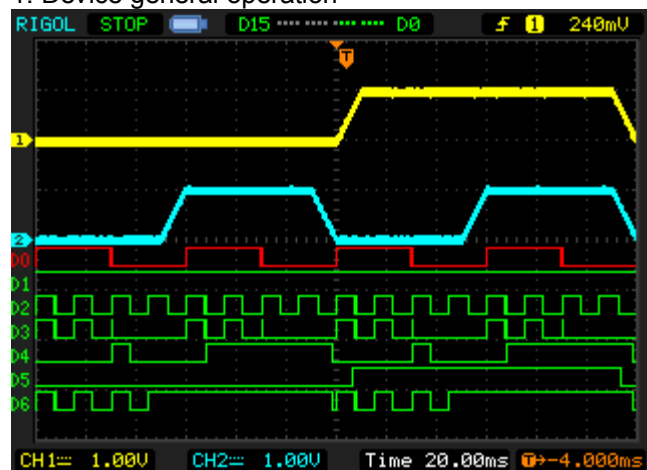
D3 – PIN#9 (VDDQ\_EN)

D4 – PIN#8 (VDDQ\_BLEED)

D5 – PIN#5 (VTT\_EN)

D6 – PIN#4 (VPP\_EN)

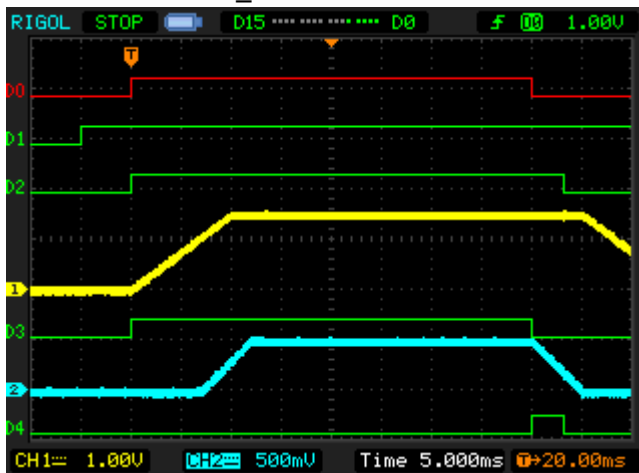
#### 1. Device general operation





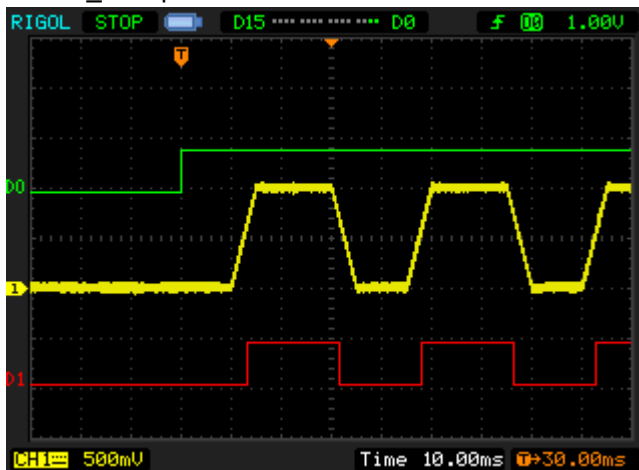
D0 – PIN#10 (SLP\_S4#)  
D1 – PIN#11 (+V3P3A)  
D2 – PIN#4 (VPP\_EN)  
Channel 1 (yellow/top line) – PIN#3 (SLP\_S3#/DDR\_VTT\_CNTL)  
D3 – PIN#9 (VDDQ\_EN)  
Channel 2 (light blue/2nd line) – PIN#6 (VDDQ(1.2V))  
D4 – PIN#8 (VDDQ\_BLEED)

### 2. Enable PIN: SLP\_S4#



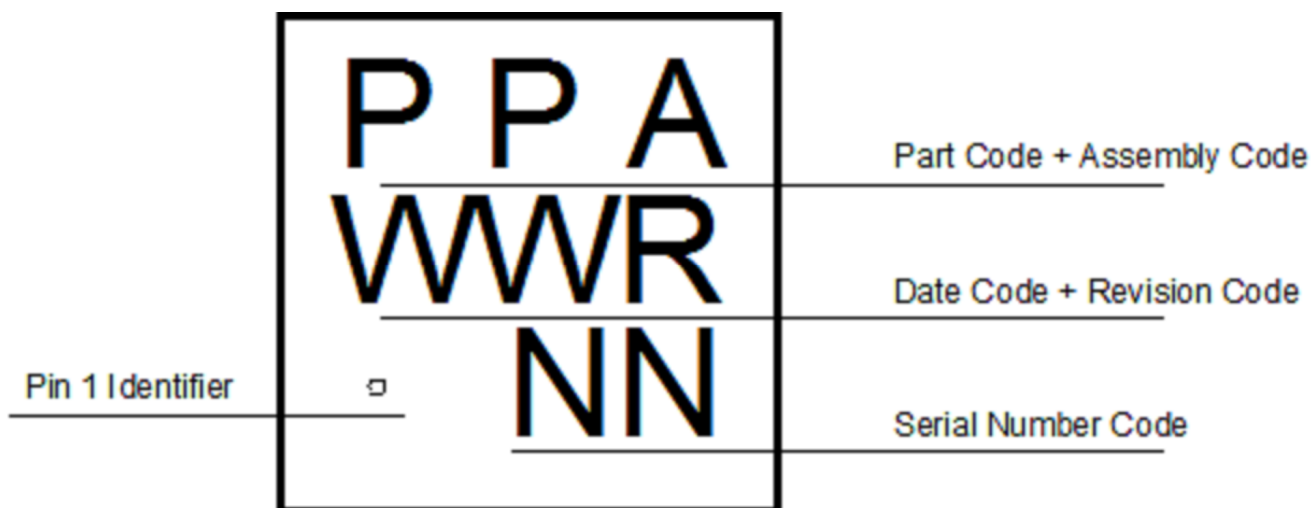
D0 – PIN#11 (+V3P3A)  
Channel 1 (yellow/top line) – PIN#3 (SLP\_S3#/DDR\_VTT\_CNTL)  
D1 – PIN#5 (VTT\_EN)

### 3. VTT\_EN operation





#### Package Top Marking



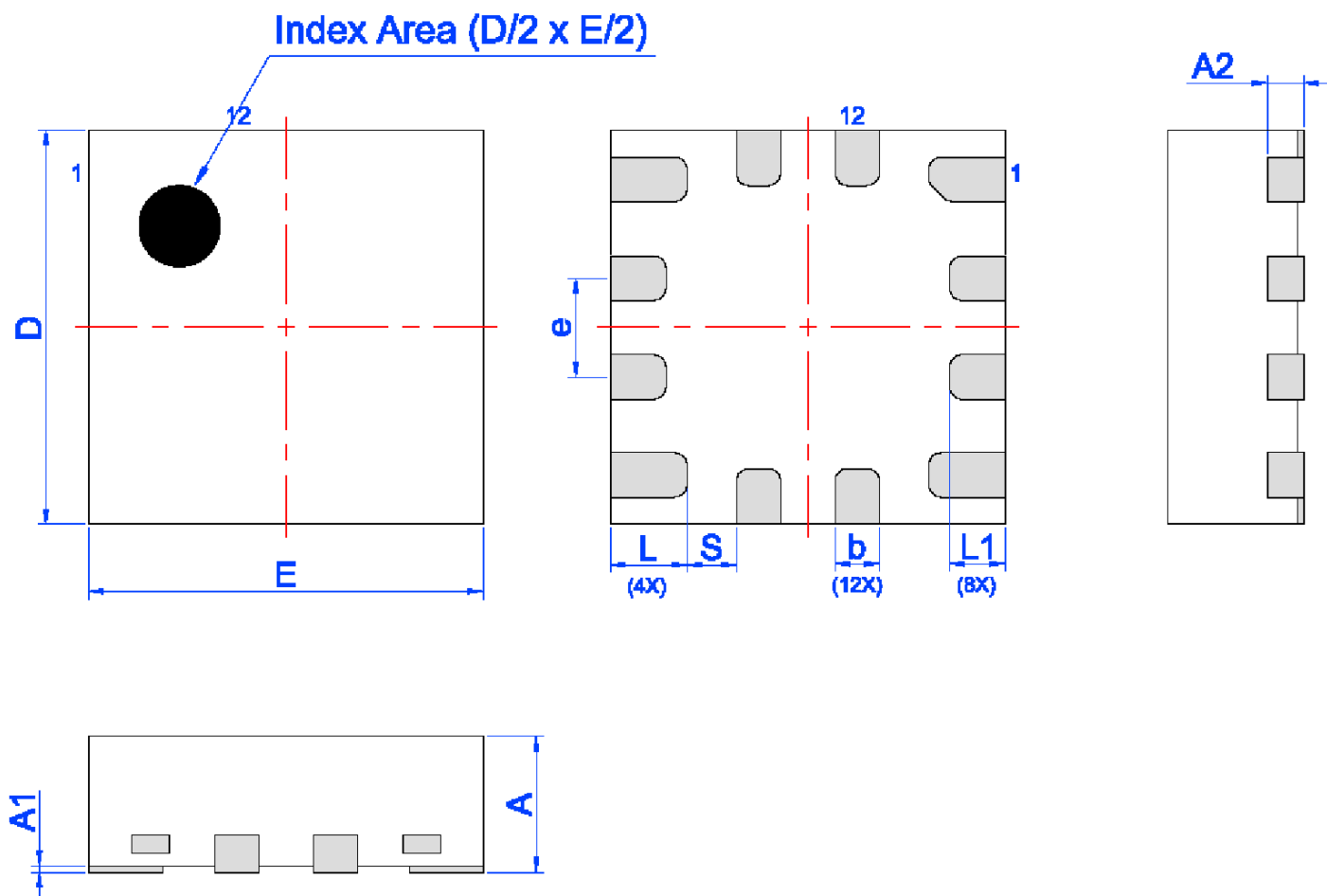
| Datasheet Revision | Programming Code Number | Locked Status | Part Code | Revision | Date       |
|--------------------|-------------------------|---------------|-----------|----------|------------|
| 1.01               | 004                     | L             | YV        | B        | 02/23/2015 |

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.



#### Package Drawing and Dimensions

##### 12 Lead STQFN Package JEDEC MO-220



Unit: mm

| Symbol | Min      | Nom. | Max   | Symbol | Min     | Nom.  | Max   |
|--------|----------|------|-------|--------|---------|-------|-------|
| A      | 0.50     | 0.55 | 0.60  | D      | 1.55    | 1.60  | 1.65  |
| A1     | 0.005    | -    | 0.060 | E      | 1.55    | 1.60  | 1.65  |
| A2     | 0.10     | 0.15 | 0.20  | L      | 0.26    | 0.31  | 0.36  |
| b      | 0.13     | 0.18 | 0.23  | L1     | 0.175   | 0.225 | 0.275 |
| e      | 0.40 BSC |      |       | S      | 0.2 REF |       |       |



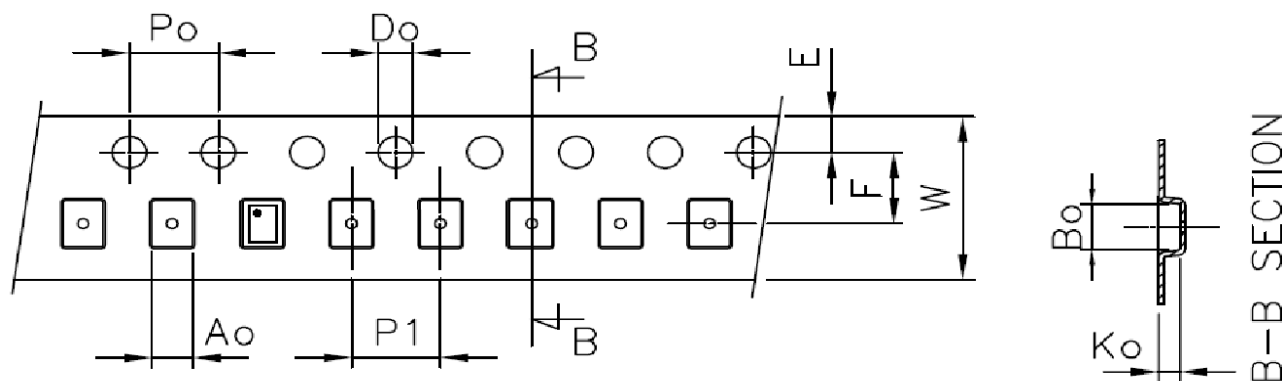
### Tape and Reel Specification

| Package Type                   | # of Pins | Nominal Package Size (mm) | Max Units |         | Reel & Hub Size (mm) | Trailer A |             | Leader B |             | Pocket (mm) |       |
|--------------------------------|-----------|---------------------------|-----------|---------|----------------------|-----------|-------------|----------|-------------|-------------|-------|
|                                |           |                           | per reel  | per box |                      | Pockets   | Length (mm) | Pockets  | Length (mm) | Width       | Pitch |
| STQFN 12L<br>FCA 0.4P<br>Green | 12        | 1.6x1.6x0.55              | 3000      | 3000    | 178/60               | 100       | 400         | 100      | 400         | 8           | 4     |

### Carrier Tape Drawing and Dimensions

| Package Type                   | Pocket BTM Length (mm) | Pocket BTM Width (mm) | Pocket Depth (mm) | Index Hole Pitch (mm) | Pocket Pitch (mm) | Index Hole Diameter (mm) | Index Hole to Tape Edge (mm) | Index Hole to Pocket Center (mm) | Tape Width (mm) |
|--------------------------------|------------------------|-----------------------|-------------------|-----------------------|-------------------|--------------------------|------------------------------|----------------------------------|-----------------|
|                                | A0                     | B0                    | K0                | P0                    | P1                | D0                       | E                            | F                                | W               |
| STQFN 12L<br>FCA 0.4P<br>Green | 1.9                    | 1.9                   | 0.8               | 4                     | 4                 | 1.5                      | 1.75                         | 3.5                              | 8               |

Refer to EIA-481 Specifications



### Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.408 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



### Datasheet Revision History

| Date       | Version | Change                                                              |
|------------|---------|---------------------------------------------------------------------|
| 03/27/2014 | 0.10    | New designSLG46120                                                  |
| 03/28/2014 | 0.11    | Corrected device functionality                                      |
| 04/02/2014 | 0.12    | Change PIN5 name VTT to VTT_EN, correctedElectrical Characteristics |
| 04/24/2014 | 0.13    | Removed LATCH from VPP_EN, ACMP1 Vref changed to 200mV              |
| 04/28/2014 | 0.14    | Added one more Functionality Waveform                               |
| 05/05/2014 | 0.15    | Added additional Functionality Waveforms                            |
| 05/23/2014 | 0.16    | Version update                                                      |
| 07/25/2014 | 0.17    | Updated Device Revision Table                                       |
| 08/25/2014 | 0.18    | Added MSL "1"<br>Renamed Package to FCA package                     |
| 09/03/2014 | 0.19    | Changed PIN11 name, updated functionality waveforms                 |
| 09/05/2014 | 0.20    | Removed one functionality waveform                                  |
| 09/25/2014 | 0.21    | Updated Device Revision Table                                       |
| 10/02/2014 | 0.22    | Changed Lock status                                                 |
| 10/03/2014 | 0.23    | Updated VIH, VIL logic levels                                       |
| 10/03/2014 | 0.24    | Updated Device Revision Table                                       |
| 11/06/2014 | 1.00    | Production Release                                                  |
| 02/23/2015 | 1.01    | Corrected VDDQ_EN output type                                       |



### Silego Website & Support

#### Silego Technology Website

Silego Technology provides online support via our website at <http://www.silego.com/>. This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

<http://greenpak.silego.com/>  
<http://greenpak2.silego.com/>  
<http://greenfet.silego.com/>  
<http://greenfet2.silego.com/>  
<http://greenclk.silego.com/>

Products are also available for purchase directly from Silego at the Silego Online Store at <http://store.silego.com/>.

### Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at [info@silego.com](mailto:info@silego.com).

For specific GreenPAK design or applications questions and support please send email requests to [GreenPAK@silego.com](mailto:GreenPAK@silego.com)

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#### Contact Your Local Sales Representative

Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to [info@silego.com](mailto:info@silego.com)

#### Contact Silego Directly

Silego can be contacted directly via e-mail at [info@silego.com](mailto:info@silego.com) or user submission form, located at the following URL: <http://support.silego.com/>

#### Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of worldwide Silego Technology offices and representatives are all available at <http://www.silego.com/>

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