



SILEGO

SLG7NT4249

**GreenPAK 3™
DISCHARGE, PGOOD MONITOR
AND LEVEL SHIFTER**

FOR INTERNAL USE ONLY

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OUTSIDE OF SILEGO AND INTEL.**

Internal Use Only



General Description

Silego SLG7NT4249 is a low power and small form device. The SoC is housed in a 2mm x 3mm TQFN package which is optimal for using with small devices.

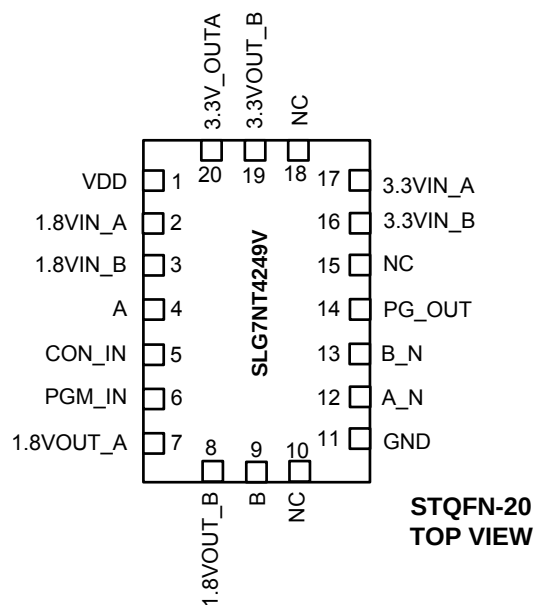
Features

- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary

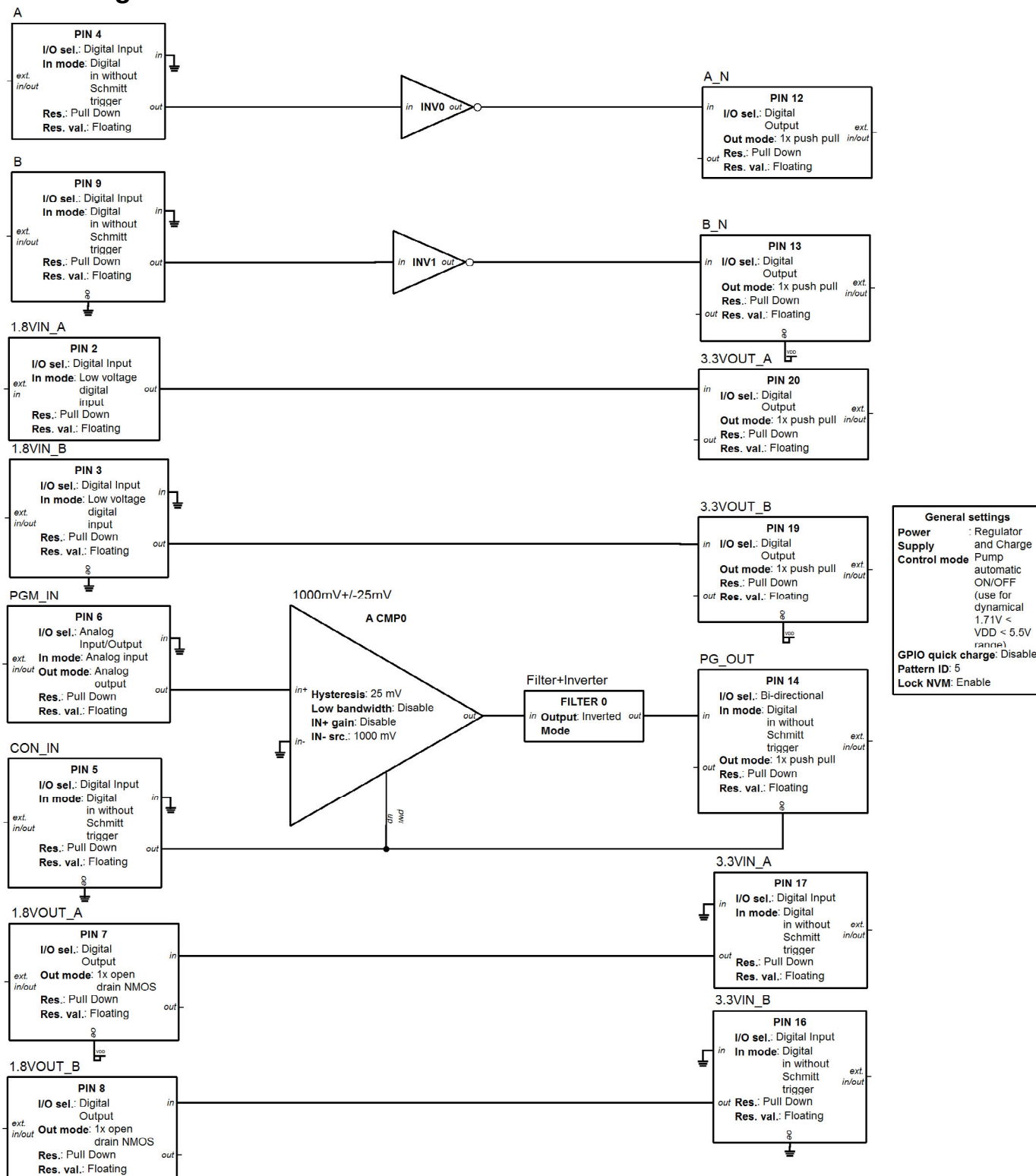
- 2 Outputs – Open Drain 1X
- 4 Outputs – Push Pull 1X
- 1 Output – Push Pull 1X / 3-State

Pin Configuration





Block Diagram





Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	1.8VIN_A	Input	Low Voltage Digital Input
3	1.8VIN_B	Input	Low Voltage Digital Input
4	A	Input	Digital Input
5	CON_IN	Input	Digital Input
6	PGM_IN	Input	Analog input
7	1.8VOUT_A	Output	Open Drain NMOS 1X
8	1.8VOUT_B	Output	Open Drain NMOS 1X
9	B	Input	Digital Input
10	NC	--	Keep Floating or Connect to GND
11	GND	GND	Ground
12	A_N	Output	Push Pull
13	B_N	Output	Push Pull
14	PG_OUT	Output	Push Pull / 3-State*
15	NC	--	Keep Floating or Connect to GND
16	3.3VIN_B	Input	Digital Input
17	3.3VIN_A	Input	Digital Input
18	NC	--	Keep Floating or Connect to GND
19	3.3VOUT_B	Output	Push Pull
20	3.3VOUT_A	Output	Push Pull

*OE = HIGH – PG_OUT is Push Pull; OE= LOW – PG_OUT is Hi-Z

Ordering Information

Part Number	Package Type
SLG7NT4249V	V=STQFN-20
SLG7NT4249VTR	STQFN-20 – Tape and Reel (3k units)



Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

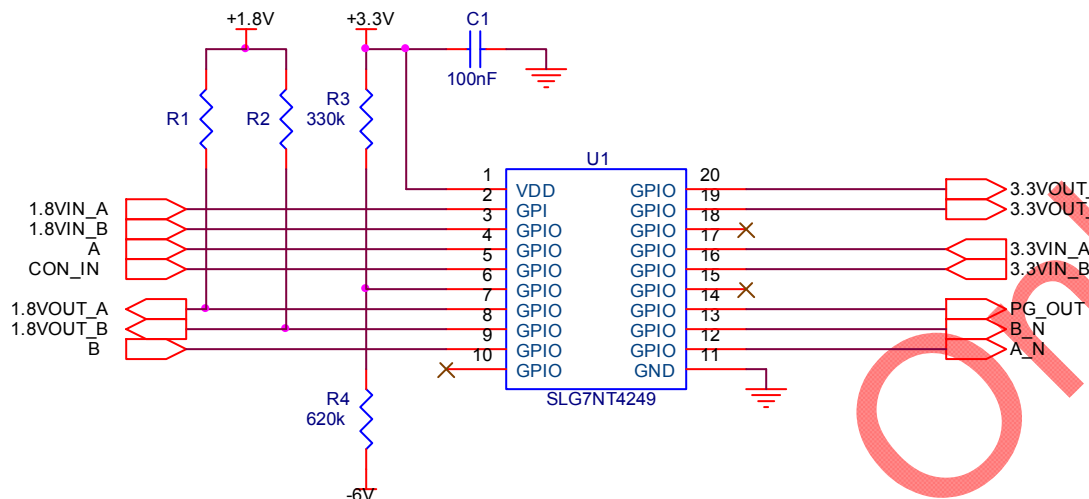
Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs, CON_IN=LOW	--	1	--	μA
		Static inputs and outputs, CON_IN=HIGH	--	90	--	μA
V_{IH}	HIGH-Level Input Voltage	Low Voltage Logic Input	1.07	--	--	V
		Logic Input	2.1	--	--	
V_{IL}	LOW-Level Input Voltage	Low Voltage Logic Input	--	--	0.76	V
		Logic Input	--	--	0.96	
I_{IH}	HIGH-Level Input Current	Logic Input Pins; $V_{IN} = 3.3V$	-1.0	--	1.0	μA
I_{IL}	LOW-Level Input Current	Logic Input Pins; $V_{IN} = 0V$	-1.0	--	1.0	μA
V_{OH}	HIGH-Level Output Voltage	Push Pull, $I_{OH} = 3\text{ mA}$, 1X Driver	2.735	3.120	--	V
V_{OL}	LOW-Level Output Voltage	Open Drain, $I_{OL} = 3\text{ mA}$, 1X Driver	--	0.080	0.15	V
		Push Pull (OE=HIGH), $I_{OL} = 3\text{ mA}$, 1X Driver	--	0.130	0.228	V
I_{OH}	HIGH-Level Output Current	Push Pull (OE=HIGH), $V_{OH} = 2.4\text{ V}$, 1X Driver	6.045	12.080	--	mA
I_{OL}	LOW-Level Output Current	Open Drain, $V_{OL} = 0.4\text{ V}$, 1X Driver	7.31	12.37	--	mA
		Push Pull (OE=HIGH), $V_{OL} = 0.4\text{ V}$, 1X Driver	4.875	8.244	--	mA
V_{ACMP0}	Analog Comparator Threshold Voltage	ACMP0 threshold including input offset, Vref variation and hysteresis	956	--	1040	mV
V_{HYST}	Analog Comparator Hysteresis	ACMP0	9.4	--	27.4	mV
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
T_{SU}	Start up Time		--	1	--	ms



Typical Application Circuit

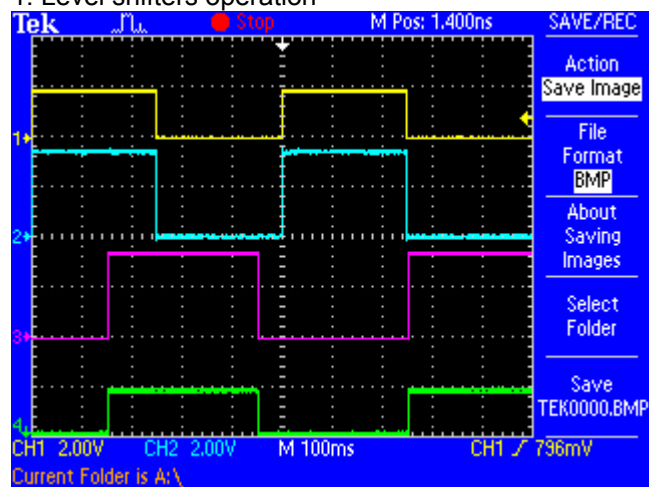




Functionality Waveforms

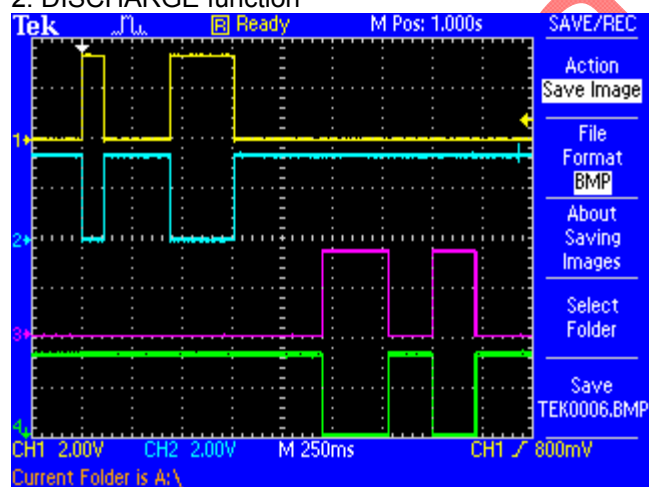
Channel1 (yellow/top line) – PIN2 (1.8VIN_A)
Channel2 (cyan/2nd line) – PIN20 (3.3VOUT_A)
Channel3 (magenta/3rd line) – PIN17 (3.3VIN_A)
Channel4 (green/bottom line) – PIN7 (1.8VOUT_A) with external 5kΩ pull up resistor

1. Level shifters operation



Channel1 (yellow/top line) – PIN4 (A)
Channel2 (light blue/2nd line) – PIN12 (A_N)
Channel3 (magenta/3rd line) – PIN9 (B)
Channel4 (magenta/3rd line) – PIN13 (B_N)

2. DISCHARGE function



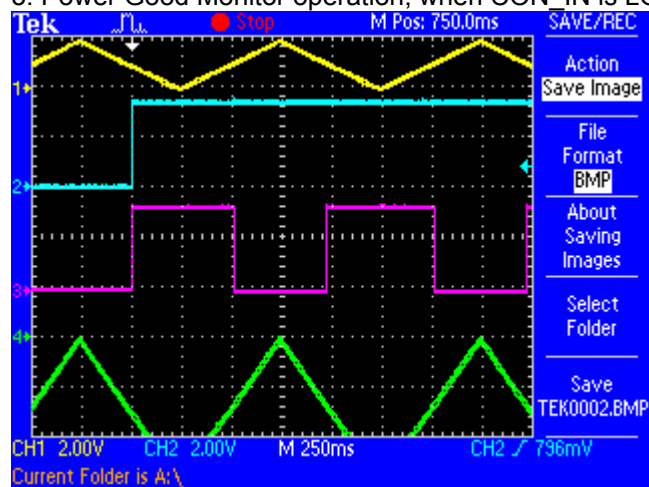


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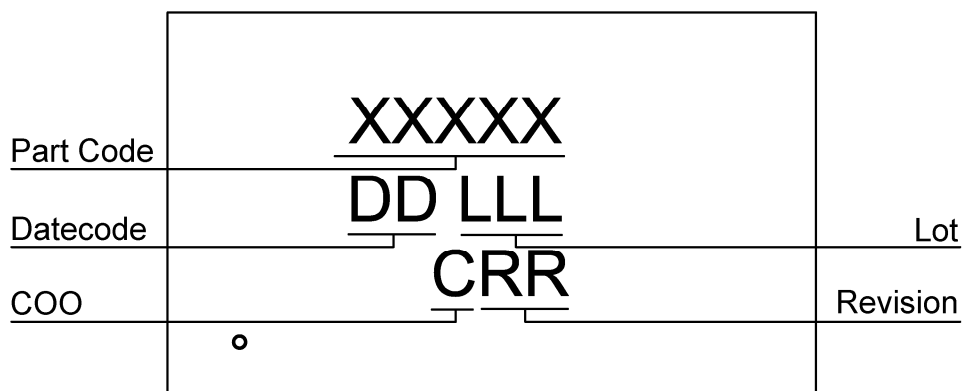
Channel1 (yellow/top line) – PIN6 (PGM_IN)
Channel2 (light blue/2nd line) – PIN5 (CON_IN)
Channel3 (magenta/3rd line) – PIN14 (PG_OUT)
Channel4 (blue/bottom line) – -6V line

3. Power Good Monitor operation, when CON_IN is LOW PG_OUT is in HI-Z state





Package Top Marking



XXXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
1.0	005	L	4249V	AB	04/15/2014

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking

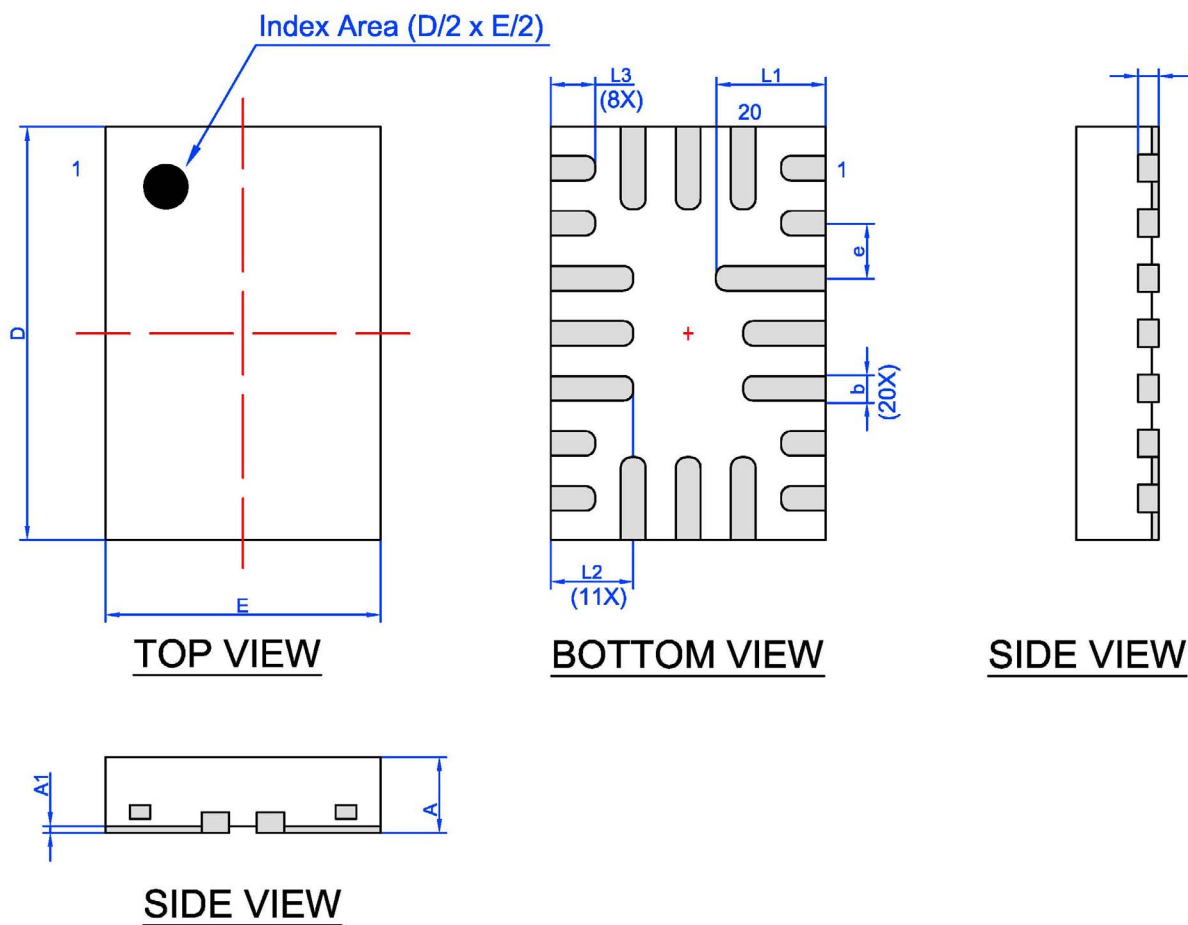


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Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE
IC Net Weight: 0.0118 g



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375



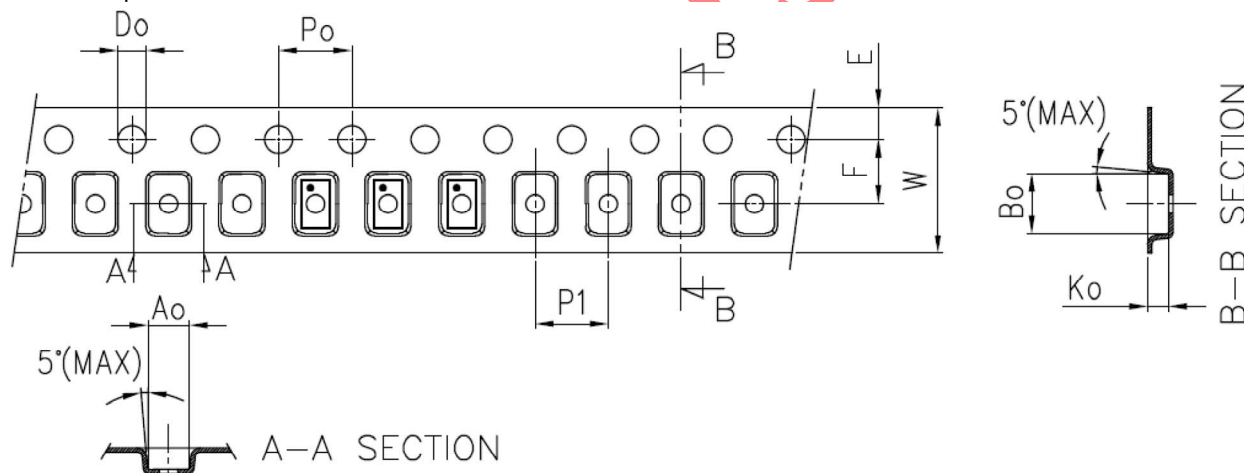
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm³ (nominal). More information can be found at www.jedec.org.



Datasheet Revision History

Date	Version	Change
09/27/2013	0.10	New design for SLG46721
10/01/2013	0.11	Inverted Discharge function
10/14/2013	0.12	Corrected 1.8VOUT_B operation
11/11/2013	0.13	Changed Discharged function
11/14/2013	0.14	Updated Device Revision Table
11/26/2013	0.15	Updated Package Outline Drawing Updated Tape and Reel Specifications Updated Carrier Tape Drawing and Dimensions Updated Recommended Reflow Soldering Profile
01/09/2014	0.16	Changed PIN12 and PIN13 to Push Pull
01/13/2014	0.17	Updated Device Revision Table
04/15/2014	1.0	Production Release



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Silego Technology provides online support via our website at <http://www.silego.com/>. This website is used as a means to make files and information easily available to customers.

For more information regarding Silego Green products, please visit:

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<http://greenfet2.silego.com/>
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Products are also available for purchase directly from Silego at the Silego Online Store at <http://store.silego.com/>.

Silego Technical Support

Datasheets and errata, application notes and example designs, user guides, and hardware support documents and the latest software releases are available at the Silego website or can be requested directly at info@silego.com.

For specific GreenPAK design or applications questions and support please send email requests to GreenPAK@silego.com

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Customers can contact their local sales representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. More information regarding your local representative is available at the Silego website or send a request to info@silego.com

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Other Information

The latest Silego Technology press releases, listing of seminars and events, listings of worldwide Silego Technology offices and representatives are all available at <http://www.silego.com/>

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