SLG6M6201V

CurrentPAK™ Ultra-small 3.8 mΩ, 10 A Power Switch with Current Sense

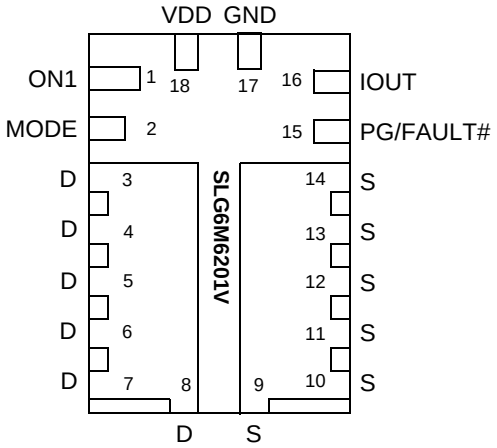
General Description

The SLG6M6201V is a 3.8 mΩ 10 A single-channel load switch that is able to switch 3.0 V to 3.6 V power rails. The product is packaged in an ultra-small 2 x 3 mm package.

Features

- 2 x 3 mm STQFN 18L FC package (6 fused pins for drain and 6 fused pins for source)
- Logic level ON pins capable of supporting 1.05 V CMOS Logic
- 3.8 mΩ RDS_{ON}while supporting 10 A
- Discharges load when off
- Two Over Current Protection Modes (Short Circuit/Active)
  - Short Circuit Current Limit
  - Active Current Limit
- Over Temperature Protection
- High / Low Current Select
- Automatic Switch from Low to High Current
- Current Sense Output:
  - Wide IDS current sensing range: 50 mA to 10 A
  - High Current Mode Accuracy
    - ±3% from 3A to 10A
    - ±6% from 1A to 2.9A
  - Low Current Mode Accuracy
    - ±10% from 0.1A to 1A
- Pb-Free / Halogen-Free / RoHS 6/6 compliant
- Operating Temperature: -10 °C to 70°C
- Operating Voltage
  - V_{DD}: 3.0 V to 3.6 V
  - V_D: 3.0 V to 3.6 V

Pin Configuration

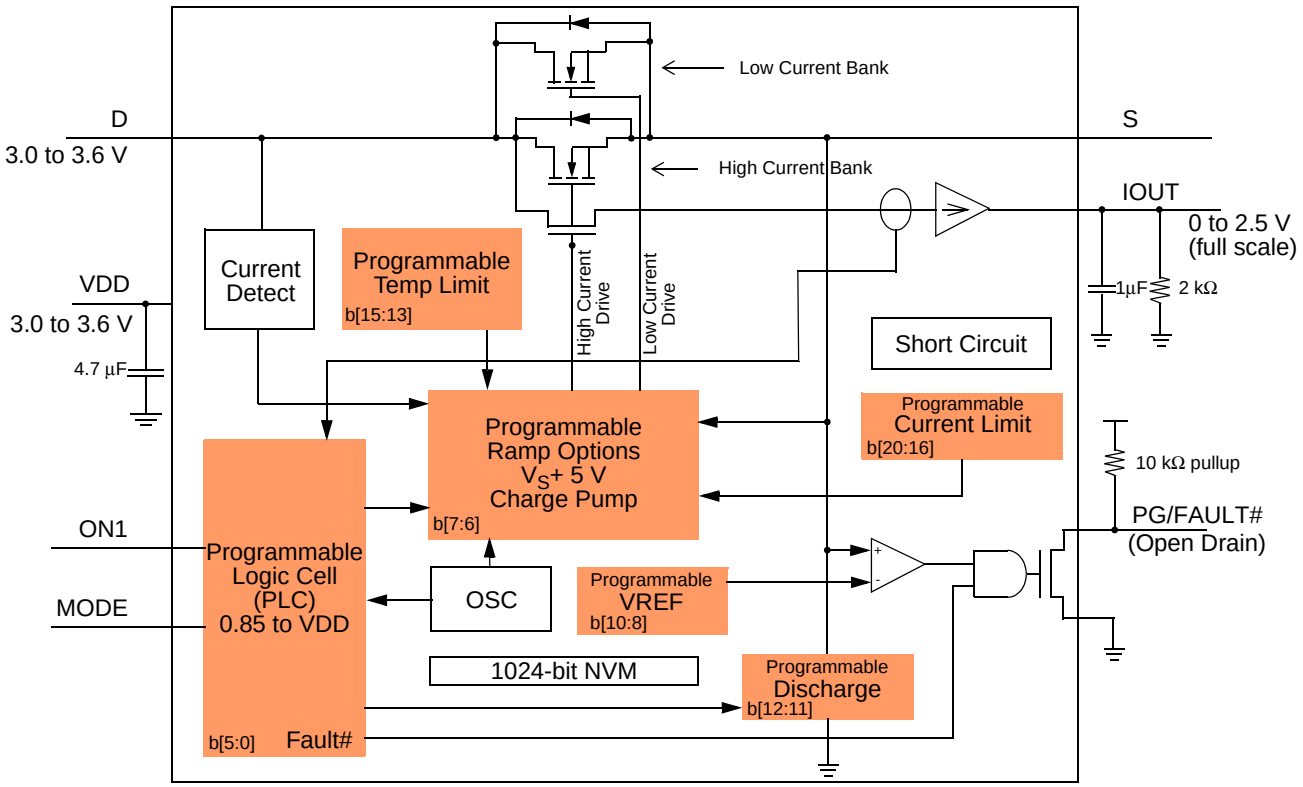


18-pin STQFN FC
(Top View)

Applications

- Notebook Power Rail Switching
- Tablet Power Rail Switching
- Server Power Rail Switching
- Telecommunications Equipment Power Rail Switching

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON1	Input	Programmable Logic (4 MΩ pull down resistor) CMOS input with V_{IL} < 0.3 V, V_{IH} > 0.85 V
2	MODE	Input	ON2 or Current Mode Selection Pin Current Mode L = High Current Mode, 10 A max (Power Up Default) H = Low Current Mode, 750 mA max
3	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
4	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
5	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
6	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
7	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
8	D	MOSFET	Drain of Power MOSFET (fused pin 3 through pin 8)
9	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
10	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
11	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
12	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
13	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
14	S	MOSFET	Source of Power MOSFET (fused pin 9 through pin 14)
15	PG/FAULT#	Output, Open Drain Only	Pin 15 is a multipurpose status output pin. 10 kΩ pull up resistor recommended. - When Pin 15 asserts high, it acts as a power good output signal. The device's VS voltage has reached 90% voltage level and the internal N-FET has fully turned on which allows max IDS current at lowest RDSON value. - When Pin 15 asserts low, it acts as a fault# notification signal. The fault condition is dependent on Pin 2's input level.
16	IOUT	Output	Current Output. 2 kΩ external resistor and 1 nF external capacitor recommended.
17	GND	GND	Ground
18	VDD	PWR	VDD power for load switch control (3.0 V to 3.6 V)

PG/FAULT# Status Table

Pin 2 (MODE)	Pin 15 (Fault#)	Device Status
L (High Current Mode)	Low	VS dropped below 90% of power rail voltage.
H (Low Current Mode)	Low	Device failed to enter low current mode. See State diagram for more details.

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	7	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
W_{DIS}	Package Power Dissipation		--	--	2.5	W
MOSFET IDS	Current from Drain to Source	Continuous	--	--	12	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	16	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature

Parameter	Description	Min.	Max.	Unit
T_O	Operating Temperature	-10	70	°C

Electrical Characteristics

Conditions: -10 °C to 70 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	-10 °C to 70 °C	3.0	--	3.6	V
I_{DD}	Power Supply Current	when OFF @ 25°C Leakage	--	1	4	µA
		when ON, no load, @ 25°C	--	340	400	µA
IDS	Drain to Source Current	High Current Mode	--	--	10	A
		Low Current Mode	--	--	750	mA

MOSFET Characteristics

Conditions: V_{DD} = 3.3 V, -10 °C to 70 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
RDS_{ON}	ON Resistance (High Current Mode)	T_A 25°C @ 100 mA	3.5	3.6	4.0	mΩ
		T_A 85°C @ 100 mA	4.2	4.4	4.7	mΩ
	ON Resistance (Low Current Mode)	T_A 25°C @ 100 mA	24.7	25.1	27.0	mΩ
		T_A 85°C @ 100 mA	29	30	32	mΩ
V_S	Source Voltage		--	0	V_D	V
V_D	Drain Voltage		3.0	--	3.6	V

ON/OFF Characteristics

Conditions: -10 °C to 70 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{INIT_DELAY}	Power up initiation delay*	See Timing Diagram	--	--	1	ms
T_{ON_DELAY}	ON Logic Delay*	See Timing Diagram	--	--	500	µs
T_{PROG_DELAY}	Programmable Delay		--	0.	--	ms
T_{SLEW}	Programmable Slew Rate	10% to 90% V_S, C_L = 10 µF, R_L = 20 Ω	--	1.6	--	V/ms
T_{TOTAL_ON}	Total on Delay	50% ON1 to V_S 90%, C_L = 10 µF, R_L = 20 Ω	1.4	--	3	ms
T_{OFF_DELAY}	Off Delay	50% ON1 to V_S Fall, No C_L, R_L = 20 Ω	11	16	25	µs
T_{PG_DELAY}	PG/FAULT# Driver Assertion Delay*	Logic trigger to PG/FAULT# asserted	--	--	100	µs
$T_{SWITCH\_DLY\_LH}$	Low Current mode to High Current Mode switch delay	50% Pin 2 to High Current Mode	--	--	5	ms
$T_{SWITCH\_DLY\_HL}$	High Current mode to Low Current Mode switch delay	50% Pin 2 to Low Current Mode	--	--	500	µs
V_{IH}	High Input Voltage	Pin 1 & Pin 2	0.85	--	V_{DD}	V
V_{IL}	Low Input Voltage	Pin 1 & Pin 2	-0.3	--	0.3	V
V_{OL_PG}	PG/FAULT# Low Output Voltage	I_{OL} = 1 mA, Pull Up Resistor = 10 kΩ, Pin 15	--	--	0.5	V
$V_{REF\_PG\_RISE}$	Power Good Rising VREF comparator voltage	V_D = 3.3 V	--	2.97	--	V
$V_{REF\_PG\_FALL}$	Power Good Falling VREF comparator voltage	V_D = 3.3 V	--	2.80	--	V
I_{LIMIT}	Active Current Limit (High Mode)	I_{LIMIT}. V_S > 500 mV, Pin 2 = Assert Low (High Current Mode)	11.5	12.5	14.0	A
	Active Current Limit (Low Mode)	I_{LIMIT}. V_S > 500 mV, Pin 2 = Assert High (Low Current Mode)	--	1.25	--	A
	Short Circuit Current Limit	V_S < 500 mV	--	2.0	--	A
I_{LIMIT_ACC}	Current Limit Accuracy*	Current Limit Accuracy	--	--	±20	%
$THERM_{OFF}$	Thermal Protection Shutoff*	automatic shutoff temperature	--	125	--	°C
$THERM_{OFF\_ACC}$	Thermal Sensor Accuracy*		--	--	±10	%
$THERM_{ON}$	Thermal Protection turn on*	automatic Turn on temperature	85	--	--	°C
$THERM_{TIME}$	Thermal shutoff reaction time*		--	--	1.0	ms
$I_{AS\_TRIGGER}$	IDS Current Automatic Low Current to High Current Trigger Level		0.8	1.0	1.2	A
$I_{BLK\_HL\_TRANS}$	IDS Current level to block illegal High current to Low Current transition		--	--	750	mA
R_{DIS}	Equivalent discharge resistance	V_S discharge resistor	280	300	350	Ω
CapSource	Source Cap	Source to GND	10	100	--	µf

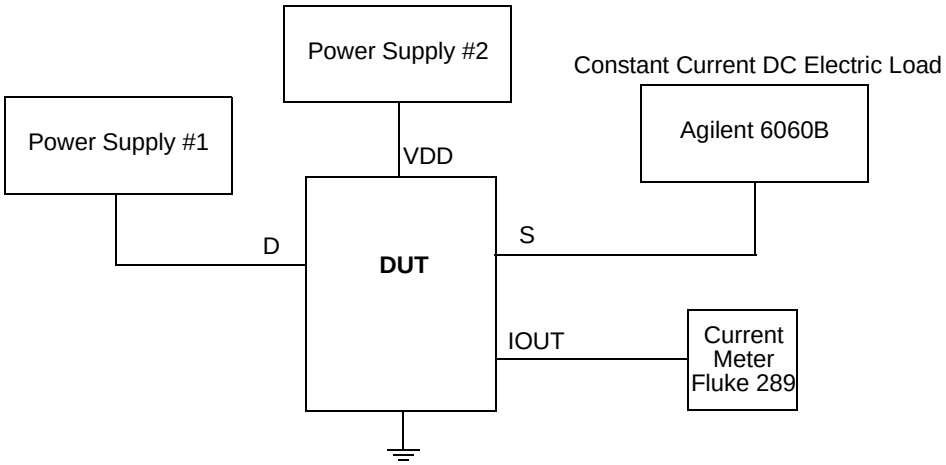
* Not 100% tested

Current Output Characteristics

Conditions: -10 °C to 70 °C (unless otherwise noted)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{SENSE}	IOUT (Pin 16) Output Current, FET Array High Current Mode 10 A Max	IDS = 10 A, Pin 2 (Mode) = L	--	1000	--	µA
		IDS = 1 A, Pin 2 (Mode) = L	--	100	--	µA
		IDS = 0.5 A, Pin 2 (Mode) = L	--	50	--	µA
	IOUT (Pin 16) Output Current, FET Array Low Mode 750 mA Max	IDS = 0.75 A, Pin 2 (Mode) = H	--	600	--	µA
		IDS = 0.1 A, Pin 2 (Mode) = H	--	80	--	µA
		IDS = 0.05 A, Pin 2 (Mode) = H	--	40	--	µA
I_{SENSE_ACC}	IOUT (Pin 16) Output Current Accuracy, FET Array High Current Mode 10 A Max	IDS = 3 A to 10 A, Pin 2 (Mode) = L	--	±3	--	%
		IDS = 1 A to 2.9 A, Pin 2 (Mode) = L	--	±6	--	%
	IOUT (Pin 16) Output Current Accuracy, FET Array Low Mode 750 mA Max	IDS = 0.1 to 1 A, Pin 2 (Mode) = H	--	±10	--	%

IOUT Accuracy Test Setup



SLG6M6201V Turn ON

The normal power on sequence is first VDD, with VD only being applied after VDD is > 1 V, and then ON after VD is at least 90% of final value. The normal power off sequence is the power on sequence in reverse.

If VDD and VD are turned on at the same time, then it is possible that a voltage glitch will appear on VS before VDD achieves 1V, which is the VT of the main MOSFET. The size of the glitch is dependent on source and drain capacitance loading and the ramp rate of VDD & VD.

SLG6M6201V Turn ON

The VS ramp follows a linear path, not an RC limitation provided the ramp is slow enough to not be current limited by load capacitance.

SLG6M6201V Current Limiting

The SLG6M6201V has two forms of current limiting.

12 A Standard Current Limiting Mode (Programmable Level)

Current is measured by mirroring the current through the main MOSFET. This response is a closed loop response and is therefore very fast and current limits in less than a few micro-seconds. There is no difference between peak or constant current limit

Temperature Cutoff

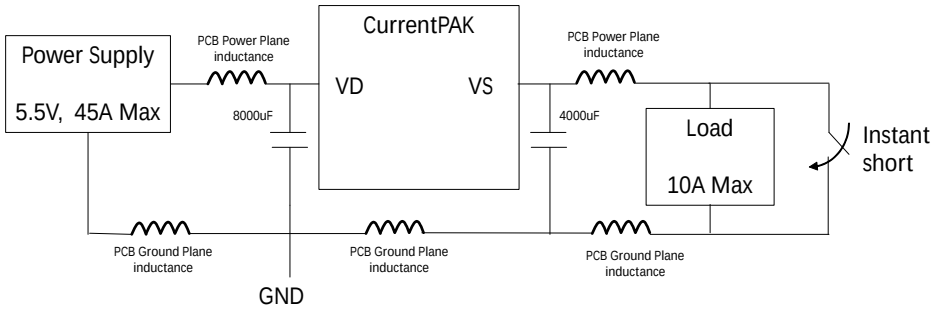
As the V(g) drops the Rds(ON) of the main MOSFET will increase, thus limiting the current, but also increasing the power dissipation of the IC. The IC is very small and cannot dissipate much power. Therefore, if a current limit condition is sustained the IC will heat up. If the junction temperature exceeds approximately 125°C (Default, Programmable), then V(g) will be brought low completely shutting off the main MOSFET. As the die cools the MOSFET will be turned back on at 100°C (Default, Programmable hysteresis).

If the current limiting condition has not been mitigated then the die will again heat up to 125°C (Default, Programmable) and the process will repeat.

Short Circuit Current Limiting Mode

When V(S) < 500 mV, the current is limited to approximately 3 A to 1.5 A. The short circuit current limit is a NVM programmable setting. This current limit is accomplished in the same manner as the Standard Current Limiting Mode with the exception that the current mirror is 15x greater. Because the current mirror is so much larger, a 15x smaller main MOSFET current is required to generate the same V(i). If V(S) rises above approximately 500 mV, then this mode is automatically switched out.

The short circuit current limiting mode does not protect the device from a sudden short after ON. In the event of a sudden short after ON, the VS pin of the CurrentPAK will switch from 10A @ 5V to ground within few nanoseconds. During this transition, the device will incur irreversible damage due to a high voltage spike created on VD or VS pins. To prevent this damage, it is recommended to add decoupling capacitors at the VD and VS pins of the CurrentPAK, as shown below, to suppress the voltage spike on the VS and VD pins. For example, assume the power supply max output feeding into the CurrentPAK is 45A max, it is recommended to use an 8000 µF capacitor from VD to GND and a 4000 µF capacitor from VS to GND. The decoupling capacitors should be placed as close to the CurrentPAK as possible. In addition to using the large size decoupling capacitors, minimizing the inductance on PCB power and ground plane is also important to minimize the voltage spike.



Short Circuit Current Limiting Mode

When V(S) < 500 mV, which is the case if there is a solder bridge during the manufacturing process or a hard short on the power rail, then the current is limited to approximately 3 A to 1.5 A. The short circuit current limit is a NVM programmable setting. This current limit is accomplished in the same manner as the Standard. Current Limiting Mode with the exception that the current mirror is 15x greater. Because the current mirror is so much larger, a 15x smaller main MOSFET current is required to generate the same V(i). If V(S) rises above approximately 500 mV, then this mode is automatically switched out.

High Current Mode vs. Low Current Mode Selection

The device powers up in high current mode as default setting. In high current mode, the max IDS is 10 A. When Pin 2 is driven from low to high, the internal power FET array shuts down 7 out of 8 banks and keeps 1 out 8 banks active.

Best system practice: The purpose of low current mode is to allow the system to get a more precise current sense reading when instantaneous IDS is between 50 mA to 750 mA. In low current mode, the IOUT (pin 16) output scales up by 8 times to produce a higher current level reading. If the system does not need precise current reading at low IDS, it is recommended to stay in high current mode at all times by tying MODE (pin 2) to GND.

The load switch can only switch to low current mode when instantaneous IDS is less than $I_{BLK\_HL\_TRANS}$ (750 mA). If the device attempts to switch to low current mode while the instantaneous IDS is higher than $I_{BLK\_HL\_TRANS}$ (750 mA), the device's internal control logic will block this operation. The device keeps the FET array in high current mode to prevent any system failures. The device also asserts FAULT# (Pin 15) low to notify the system that the attempt to switch to low current mode has failed.

If the IDS current increases above $I_{AS\_TRIGGER}$ (1.0 A typ), the device automatically switches back to high current mode by turning on all eight banks of the FET array. The auto switch delay time is $T_{SWITCH\_DLY\_LH}$ (5 ms max).

Programmable NVM Settings

ON1 and ON2 Pin Configuration

ON1 and ON2 pins are inputs to a small NVM programmable logic cell “PLC”.

Bits [2:0]	ON Logic Functions
000	Pin1 = ON1 Pin2 = H/L Select, No Delay

Bits [5:3]	Turn ON Delay Functions
000	0 ms Delay ON1

Note: Delay table not applicable to turn device off.

Power On Ramp Options

The Power On Ramp Options are NVM programmable via the followings bits.

Bits [7:6]	Ramp Options (V_D of 3.3V)	Tolerance	
		Typ	Max
00	2 ms linear ramp from output of programmable logic cell “PLC” to 90% of V_D assuming < 500 µs delay from PLC out to start of ramp	1.6 V/ms	2.0 V/ms

Power Good Reference Settings

The Power Good feature is NVM programmable via the followings bits.

Bits [10:8]	V_D [V]	Under Voltage Detect Level		Tolerance	
		PG rising on rising input	PG falling on falling input	Typical @ 25 °C	Max over PVT @ -20 to 70 °C
001	3.3	2.97	2.805	±3%	±5%

Power Good turns on ~ 100 µs after power condition is met.

Discharge Settings

The discharge options are NVM programmable via the followings bits.

Bits [12:11]	Resistance [Ω]		
	Min	Typ	Max
01	280	300	350

Temperature Shutdown Settings

The temperature shutdown limit is NVM programmable via the followings bits.

Bits [15:13]	Temperature [°C]	Hysteresis [°C]	Tolerance
000	125	25	±10 °C

Active Current Limit Settings

The Active Current Limit is NVM programmable via the followings bits.

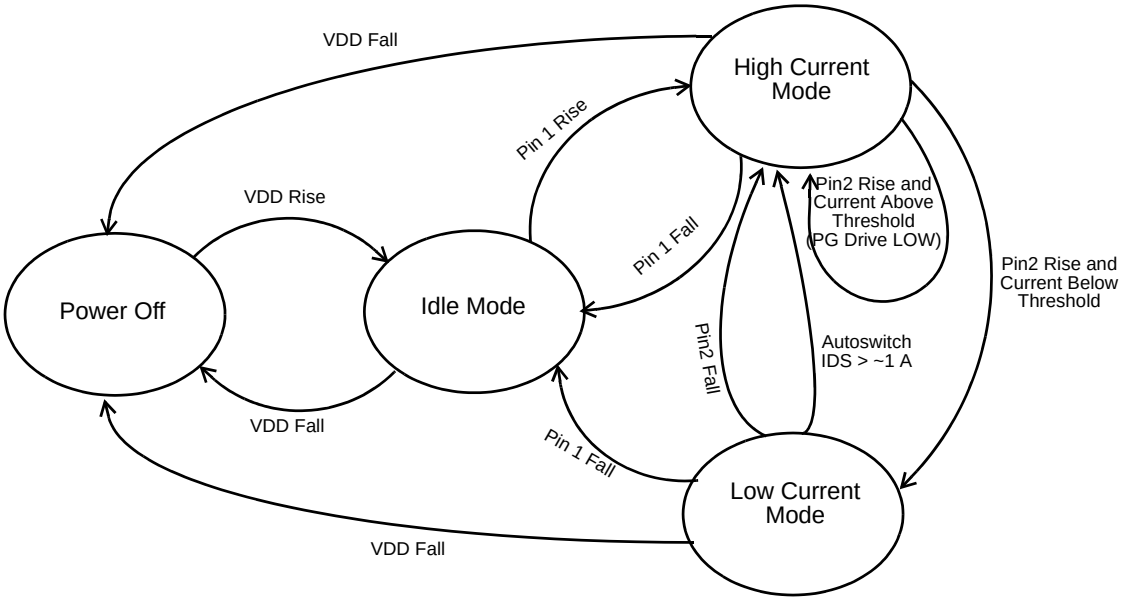
Bits [17:16]	Current Limit [A] (High Current Mode)	Current Limit [A] (Low Current Mode)	Voltage Level of V_S	Tolerance
00	12 (default)	1.5 (default)	> 500 mV	±20%

Short Circuit Current Limit Level

Bits [20:18]	Current Limit [A], VS < 500 mV	Short Circuit Current Limit Tolerance
011	2.0	±50%

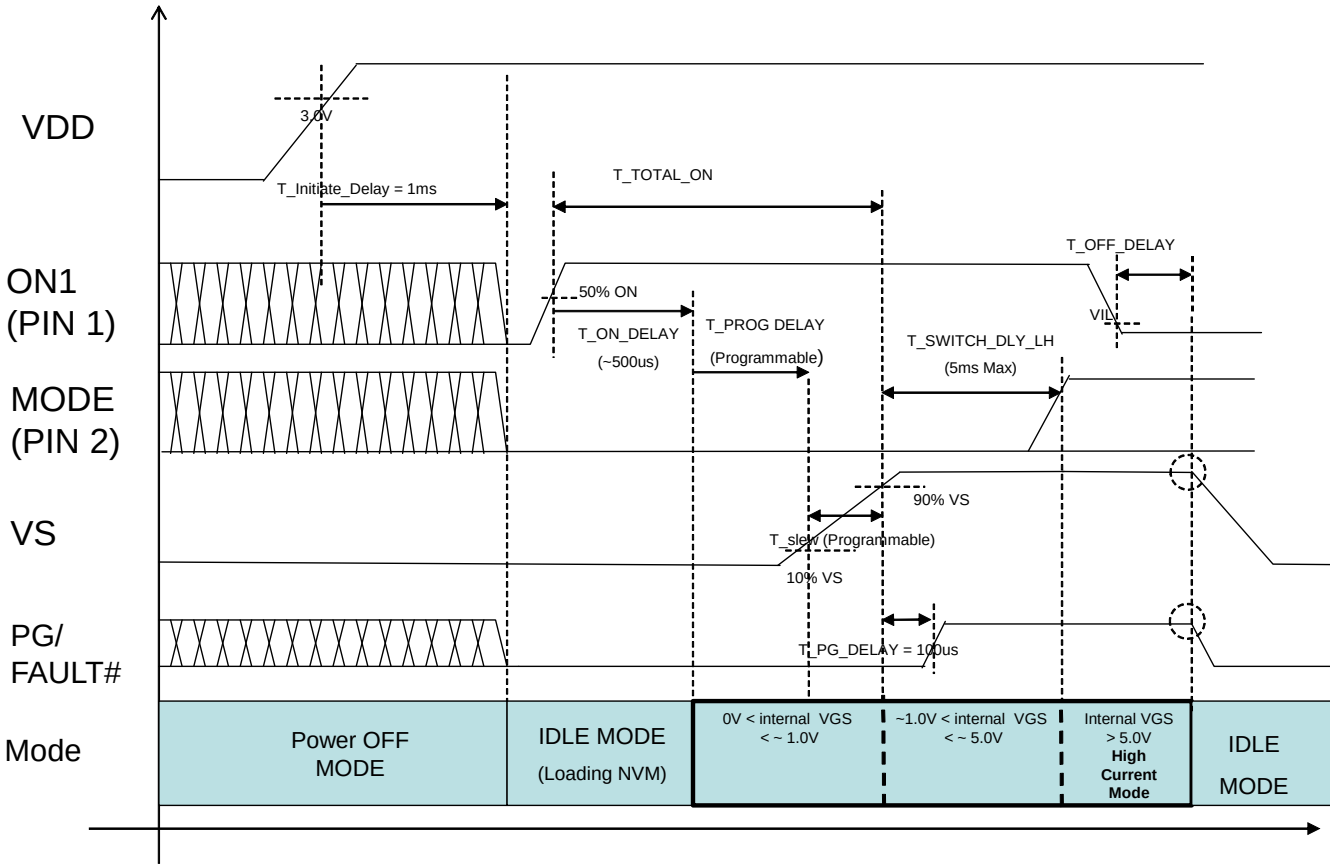
Bits [1023:21] are reserved.

State Diagram



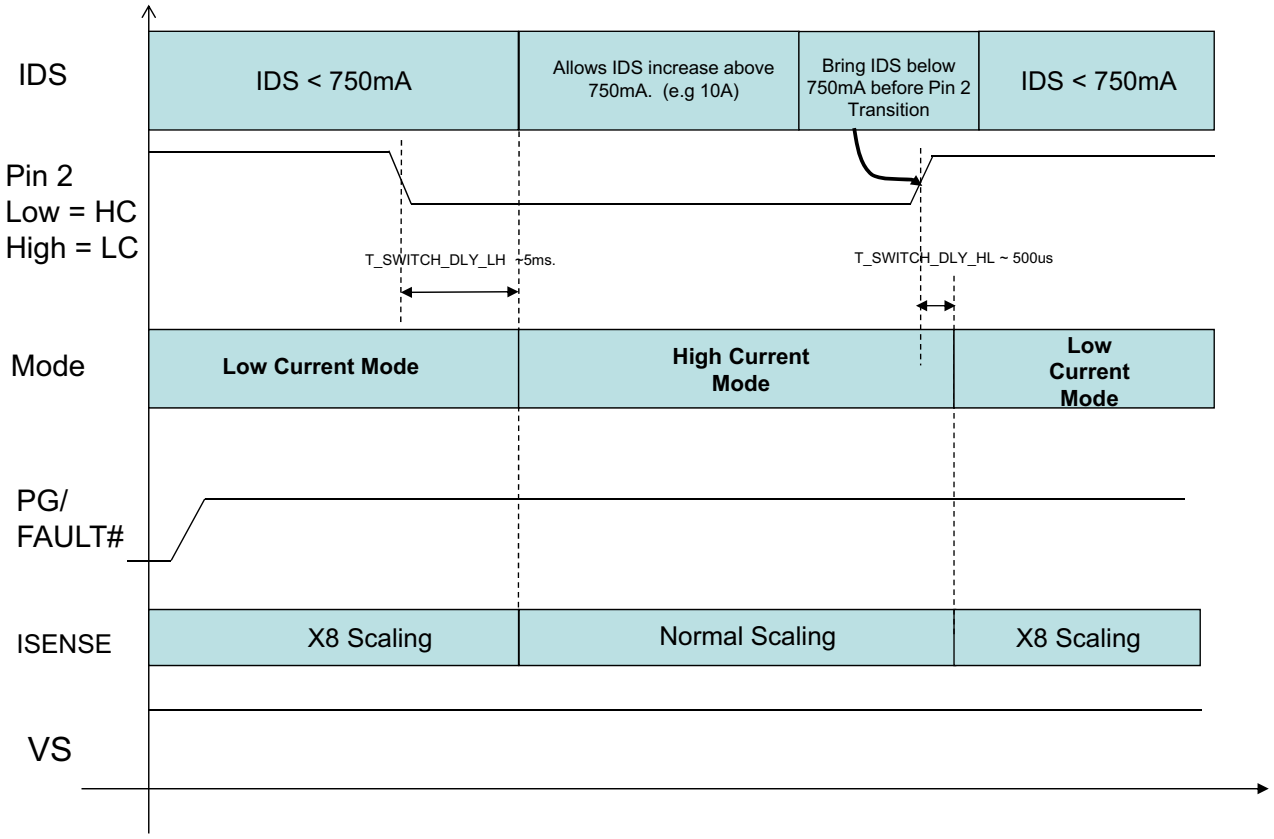
Note: Pin 2 (MODE) must stay LOW during initial power up. After the device enters High Current Mode, the system can select Low Current Mode by driving Pin 2 to HIGH level

Initialization Timing Diagram

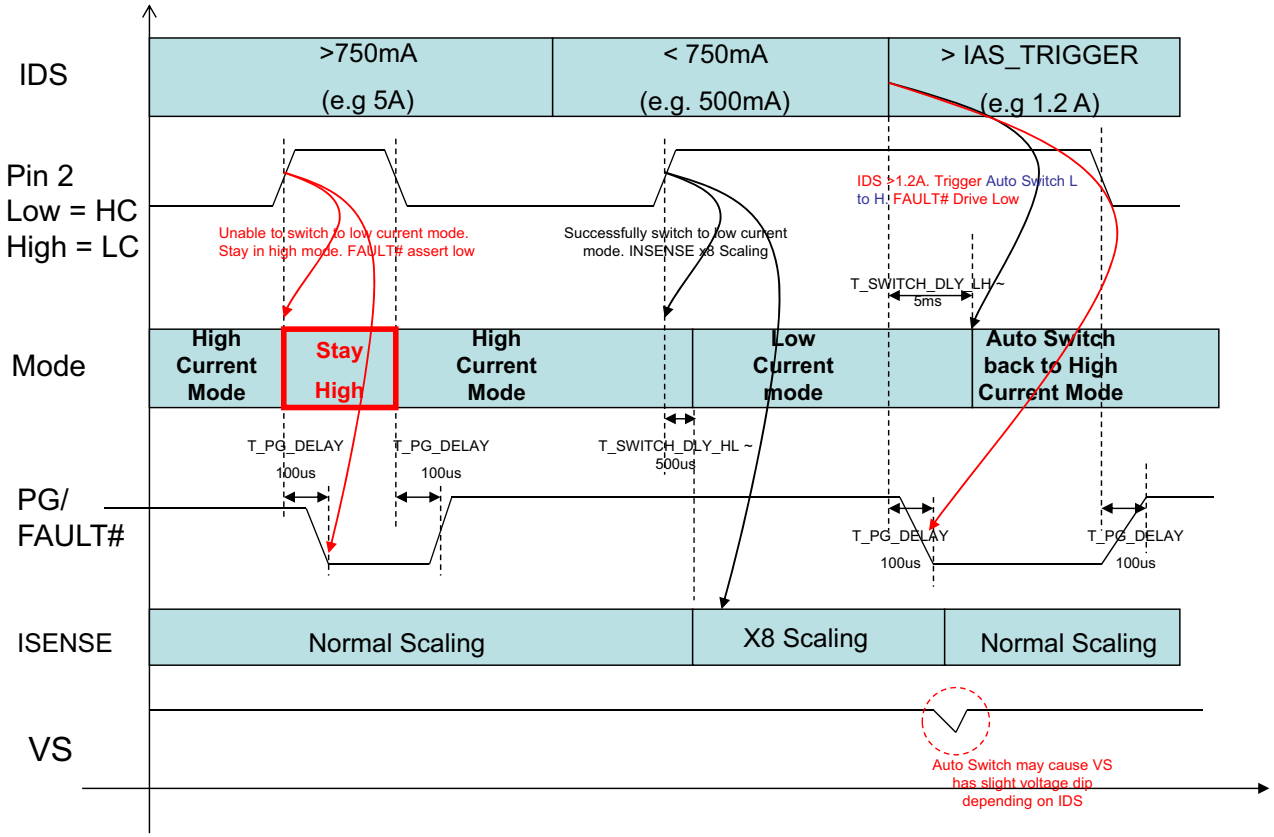


Note: Pin 2 must stay LOW before the rising edge of Pin 1. Pin 2 can go HIGH only after V_S goes above 90%

H->L & L->H Transition Timing Diagram



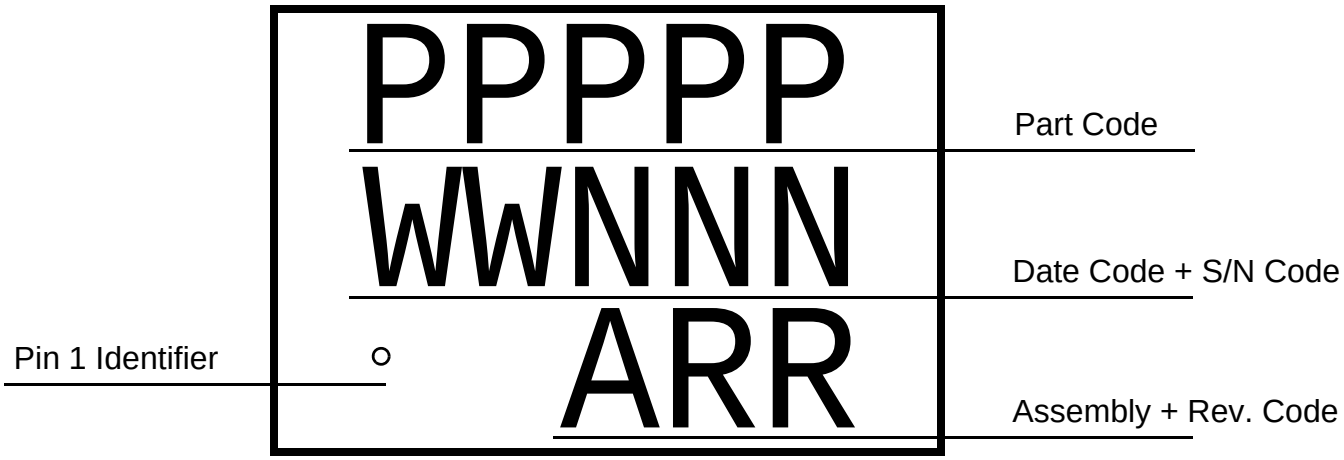
Illegal & Auto Mode Transition Timing Diagram



Ordering Information

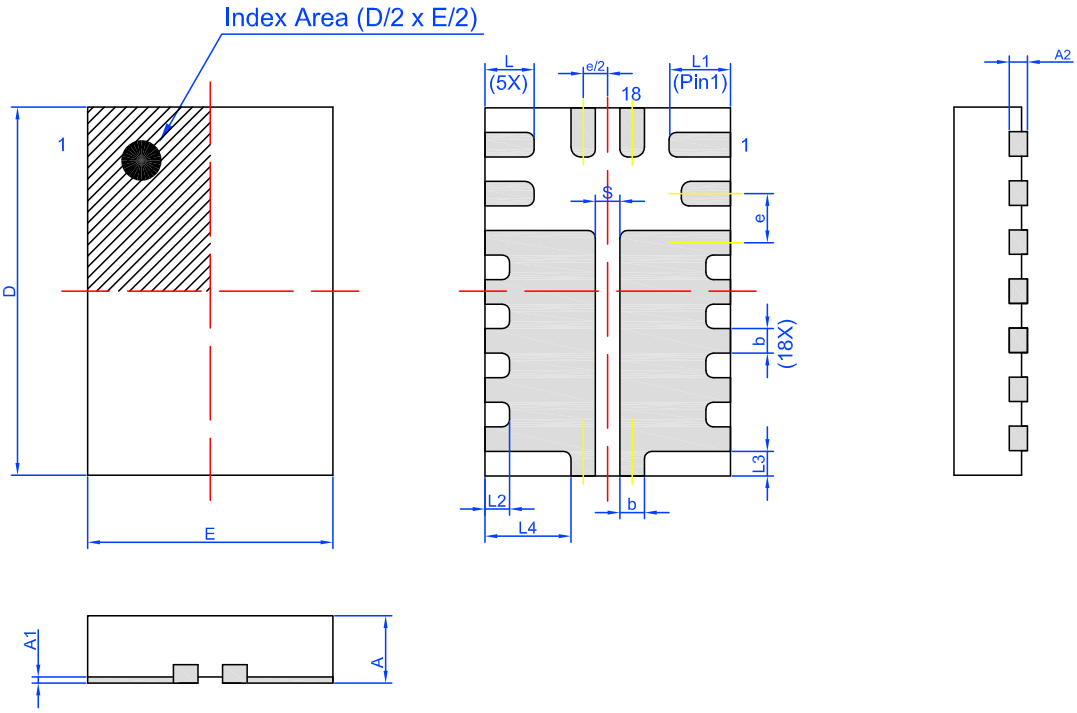
Part Number	Type	Production Flow
SLG6M6201V	STQFN 18L FC	Commercial, -10 °C to 70 °C
SLG6M6201VTR	STQFN 18L FC (Tape and Reel)	Commercial, -10 °C to 70 °C

Package Top Marking System Definition



Package Drawing and Dimensions

18 Lead TQFN Package 2 x 3 mm (Fused Lead)
JEDEC MO-220, Variation WCEE



Unit: mm

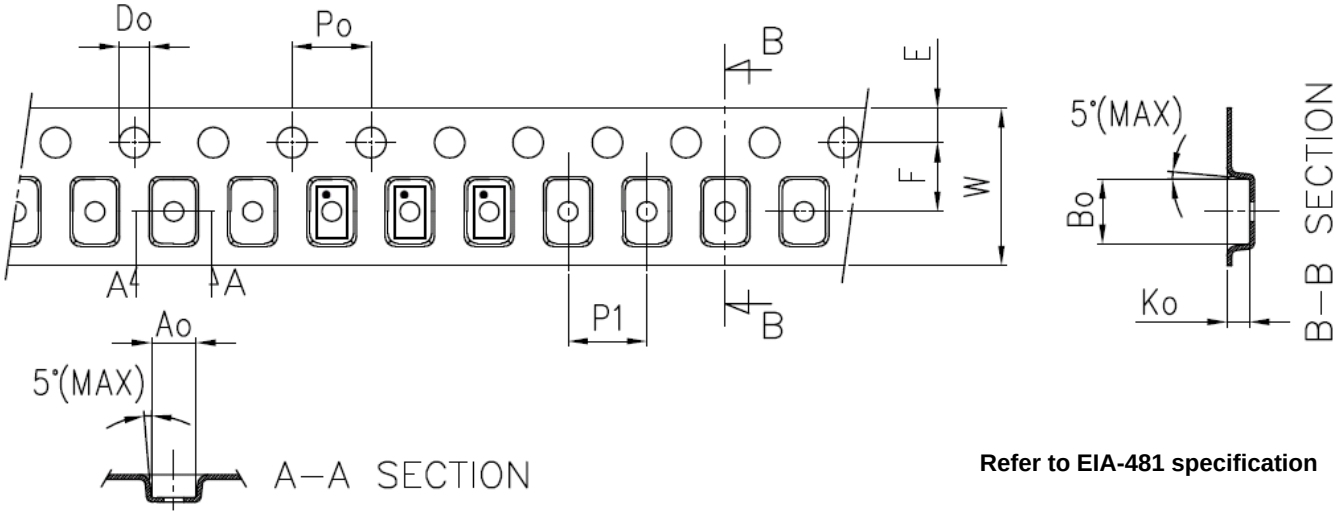
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.060	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	L1	0.45	0.50	0.55
e	0.40 BSC			L2	0.2 REF		
S	0.2 REF			L3	0.2 REF		
				L4	0.7 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 18L FC Green	18	2 x 3 x 0.55	3,000	3,000	178 / 60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 18L FC Green	2.25	3.3	1.1	4	4	1.55	1.75	3.5	8



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.