



# SILEGO

# SLG59M1649V

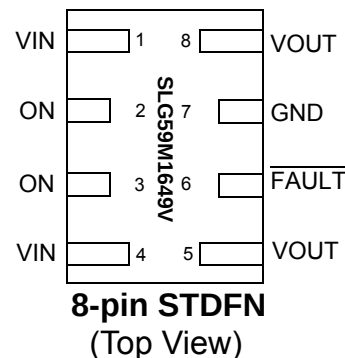
## An Ultra-small, Low-power 23 m $\Omega$ /4 A P-Channel Integrated Power Switch with Reverse-Current Blocking

### General Description

The SLG59M1649V is a self-powered, high-performance, 23 m $\Omega$  pFET integrated power switch designed for 1.5 to 5 V power rail applications up to 4 A. When enabled, internal reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a  $V_{OUT} + 50\text{mV} > V_{IN}$  condition opens the switch). Upon the detection of a reverse condition, an open-drain  $\overline{\text{FAULT}}$  output is asserted. In the event the  $V_{IN}$  voltage is too low, the power switch also contains an internal UVLO threshold monitor to keep or to turn the switch OFF.

Designed to operate over a  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  range, the SLG59M1649V is available in a RoHS-compliant, ultra-small 1.0 x 1.6 mm STDFN package.

### Pin Configuration



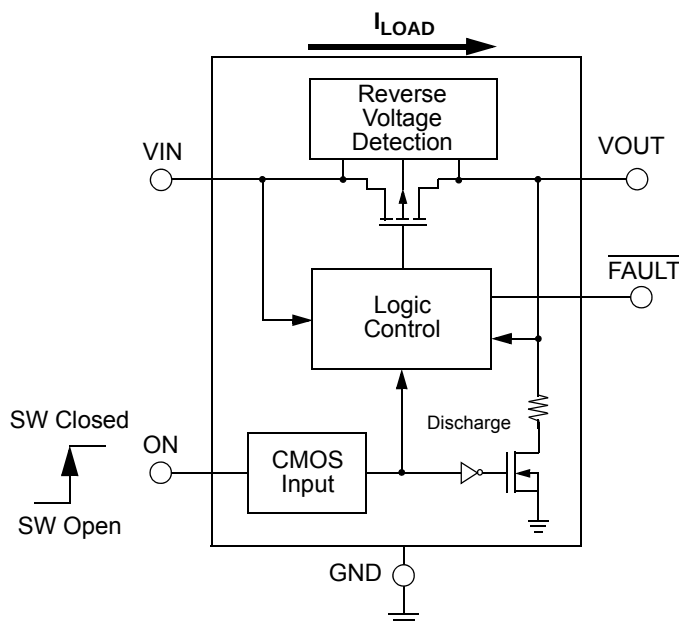
### Features

- Steady-state Operating Current: Up to 4 A
- Low Typical  $\text{RDS}_{\text{ON}}$ :
  - 23 m $\Omega$  at  $V_{\text{IN}} = 5\text{ V}$
  - 31 m $\Omega$  at  $V_{\text{IN}} = 2.5\text{ V}$
  - 42 m $\Omega$  at  $V_{\text{IN}} = 1.5\text{ V}$
- Operating Voltage: 1.5 V to 5.5 V
- Reverse-voltage Detection ON or OFF
- Internal Gate Drive and  $V_{\text{OUT}}$  Discharge
- Open-drain  $\overline{\text{FAULT}}$  Signaling
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Low  $\theta_{\text{JA}}$ , 8-pin 1.0 mm x 1.6 mm STDFN Packaging
  - Pb-Free / Halogen-Free / RoHS compliant packaging

### Applications

- Power-Rail Switching:
  - Notebook/Laptop/Tablet PCs
  - Smartphones/Wireless Handsets
  - High-definition Digital Cameras
  - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

### Block Diagram





### Pin Description

| Pin # | Pin Name                  | Type        | Pin Description                                                                                                                                                                                                                                                                                                                                                                                                                  |
|-------|---------------------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 4  | VIN                       | Power/Input | With an internal 1.2V UVLO threshold, VIN supplies the power for the operation of the power switch, the internal control circuitry, and the source terminal of pFET. Bypass the VIN pin to GND with a 2.2 $\mu$ F (or larger), low-ESR capacitor.                                                                                                                                                                                |
| 2, 3  | ON                        | Input       | A low-to-high transition on this pin initiates the operation of the power switch. ON is an asserted-HIGH, level-sensitive CMOS input with $V_{IL} < 0.3$ V and $V_{IH} > 1$ V. As the ON input circuitry does not have an internal pull-down resistor, connect the ON pin directly to a GPIO controller – do not allow this pin to be open circuited.                                                                            |
| 5, 8  | VOUT                      | Output      | Output and drain terminal of MOSFET.                                                                                                                                                                                                                                                                                                                                                                                             |
| 6     | $\overline{\text{FAULT}}$ | Output      | An open drain output, $\overline{\text{FAULT}}$ is asserted within $T_{\text{FAULT\_LOW}}$ when a ( $V_{\text{OUT}} + V_{\text{REVERSE}} > V_{\text{IN}}$ ) condition is detected. The $\overline{\text{FAULT}}$ output is deasserted within $T_{\text{FAULT\_HIGH}}$ when the fault condition is removed. Connect an external 10-k $\Omega$ resistor from the $\overline{\text{FAULT}}$ pin to the system's local logic supply. |
| 7     | GND                       | GND         | Ground connection. Connect this pin to system analog or power ground plane.                                                                                                                                                                                                                                                                                                                                                      |

### Ordering Information

| Part Number   | Type                  | Production Flow             |
|---------------|-----------------------|-----------------------------|
| SLG59M1649V   | STDFN                 | Industrial, -40 °C to 85 °C |
| SLG59M1649VTR | STDFN (Tape and Reel) | Industrial, -40 °C to 85 °C |



### Absolute Maximum Ratings

| Parameter                     | Description                         | Conditions                                                       | Min. | Typ. | Max. | Unit |
|-------------------------------|-------------------------------------|------------------------------------------------------------------|------|------|------|------|
| $V_{IN}$                      | Power Switch Input Voltage          |                                                                  | -0.3 | --   | 6    | V    |
| $T_S$                         | Storage Temperature                 |                                                                  | -65  | --   | 150  | °C   |
| ESD <sub>HBM</sub>            | ESD Protection                      | Human Body Model                                                 | 2000 | --   | --   | V    |
| ESD <sub>CDM</sub>            | ESD Protection                      | Charged Device Model                                             | 1000 | --   | --   | V    |
| MSL                           | Moisture Sensitivity Level          |                                                                  | 1    |      |      |      |
| $\Theta_{JA}$                 | Thermal Resistance                  | 1.0 x 1.6 mm 8L STDFN                                            | --   | 82   | --   | °C/W |
| $T_{J,MAX}$                   | Maximum Junction Temperature        |                                                                  | --   | 150  | --   | °C   |
| MOSFET<br>IDS <sub>CONT</sub> | Continuous Current from VIN to VOUT | Each channel, $T_J < 150^\circ\text{C}$                          | --   | --   | 2    | A    |
| MOSFET IDS <sub>PK</sub>      | Peak Current from Drain to Source   | Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle | --   | --   | 2.5  | A    |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Electrical Characteristics

$1.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ;  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted.

Typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise stated)

| Parameter         | Description                                                 | Conditions                                                                       | Min. | Typ. | Max.     | Unit          |
|-------------------|-------------------------------------------------------------|----------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{IN}$          | Power Switch Input Voltage                                  |                                                                                  | 1.5  | --   | 5.5      | V             |
| $V_{IN(UVLO)}$    | $V_{IN}$ Undervoltage Lockout Threshold                     | $V_{IN} \uparrow$ , $V_{ON} = 0\text{V}$ , $I_{OUT} = -100\text{ mA}$            | --   | --   | 1.2      | V             |
|                   |                                                             | $V_{IN} \downarrow$ , $V_{ON} = 0\text{V}$ , $R_{LOAD} = 10\Omega$               | 0.5  | --   | --       | V             |
| $I_{IN}$          | Quiescent Power Switch Current                              | $V_{IN} = 5.25\text{V}$ , $V_{ON} = \text{HIGH}$ , $I_{OUT} = 0\text{ mA}$       | --   | 6.6  | 11       | $\mu\text{A}$ |
|                   |                                                             | $V_{IN} = 1.5\text{ V}$ , $V_{ON} = \text{HIGH}$ , $I_{OUT} = 0\text{ mA}$       | --   | 5    | 8        | $\mu\text{A}$ |
| $I_{IN(OFF)}$     | OFF Mode Power Switch Current                               | $V_{IN} = 5.25\text{ V}$ , $V_{ON} = \text{LOW}$ , $R_{LOAD} = 1\text{ M}\Omega$ | --   | 2    | 3        | $\mu\text{A}$ |
|                   |                                                             | $V_{IN} = 1.5\text{ V}$ , $V_{ON} = \text{LOW}$ , $R_{LOAD} = 1\text{ M}\Omega$  | --   | 0.8  | 2        | $\mu\text{A}$ |
| RDS <sub>ON</sub> | Static Drain to Source ON Resistance                        | $T_A = 25^\circ\text{C}$ , $V_{IN} = 5.0\text{ V}$ , $I_{LOAD} = -200\text{ mA}$ | --   | 23   | 28       | m $\Omega$    |
|                   |                                                             | $T_A = 25^\circ\text{C}$ , $V_{IN} = 2.5\text{ V}$ , $I_{LOAD} = -200\text{ mA}$ | --   | 31   | 38       | m $\Omega$    |
|                   |                                                             | $T_A = 25^\circ\text{C}$ , $V_{IN} = 1.5\text{ V}$ , $I_{LOAD} = -200\text{ mA}$ | --   | 42   | 50       | m $\Omega$    |
| $V_{REVERSE}$     | Reverse-current Voltage Threshold                           |                                                                                  | --   | 50   | --       | mV            |
| $I_{REVERSE}$     | Reverse-current Leakage Current after Reverse Current Event | $V_{OUT} - V_{IN} > V_{REVERSE}$ ; $T_A = 25^\circ\text{C}$ ; ON = GND           | --   | 1    | --       | $\mu\text{A}$ |
| $V_{ON}$          | ON Pin Voltage Range                                        |                                                                                  | 0    |      | $V_{IN}$ | V             |
| $I_{ON(Leakage)}$ | ON Pin Leakage Current                                      | $1.4\text{ V} \leq V_{ON} \leq V_{IN}$ or $V_{ON} = \text{GND}$                  | --   | --   | 1        | $\mu\text{A}$ |
| ON_ $V_{IH}$      | ON Pin Input High Voltage                                   |                                                                                  | 1    | --   | $V_{DD}$ | V             |
| ON_ $V_{IL}$      | ON Pin Input Low Voltage                                    |                                                                                  | -0.3 | 0    | 0.3      | V             |
| ON <sub>HYS</sub> | ON Hysteresis                                               |                                                                                  | --   | 60   | --       | mV            |



### Electrical Characteristics (continued)

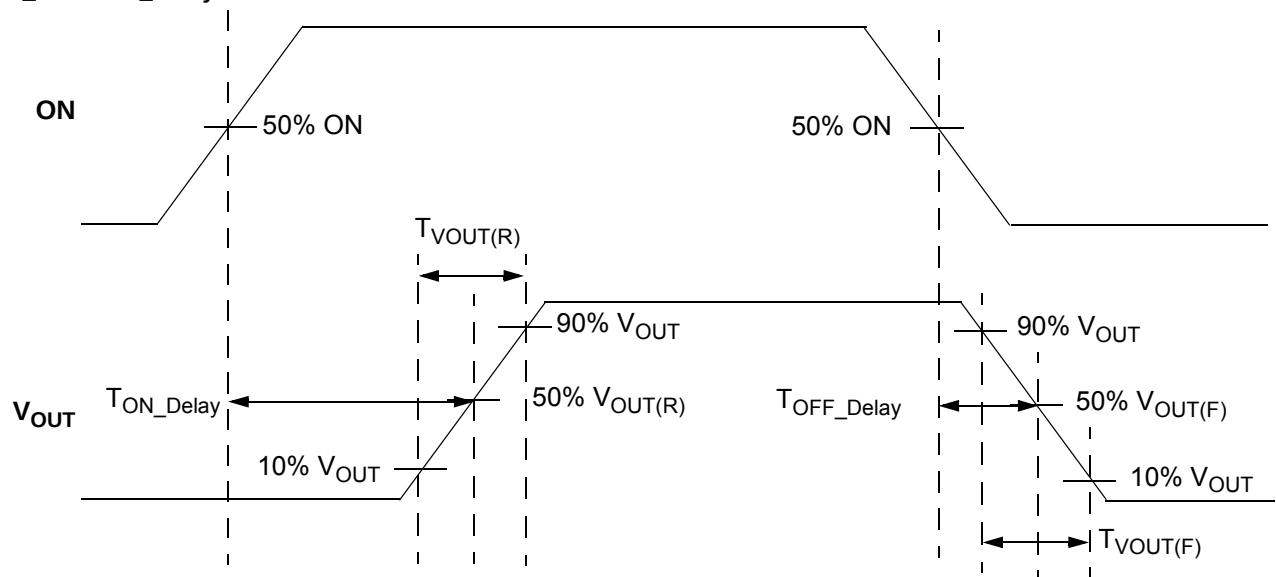
$1.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ ;  $C_{IN} = 2.2\text{ }\mu\text{F}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $85\text{ }^\circ\text{C}$ , unless otherwise noted.

Typical values are at  $T_A = 25\text{ }^\circ\text{C}$  (unless otherwise stated)

| Parameter                    | Description                           | Conditions                                                                                                                                                                    | Min. | Typ. | Max. | Unit          |
|------------------------------|---------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $R_{DSCHRG}$                 | Output Discharge Resistance           | $V_{IN} = 5\text{ V}$ ; $V_{OUT} < 0.4\text{ V}$                                                                                                                              | 50   | 80   | 120  | $\Omega$      |
| $T_{REV}$                    | Reverse-current Detect Response Delay | $V_{IN} = 5\text{ V}$                                                                                                                                                         | --   | 10   | --   | $\mu\text{s}$ |
| $T_{REARM}$                  | Reverse Detect Rearm Time             |                                                                                                                                                                               | --   | 1.5  | --   | ms            |
| $T_{ON\_Delay}$              | ON Delay Time                         | 50% ON to 50% $V_{OUT}$ $\uparrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$     | --   | 180  | 235  | $\mu\text{s}$ |
|                              |                                       | 50% ON to 50% $V_{OUT}$ $\uparrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 1.5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$   | --   | 110  | 145  | $\mu\text{s}$ |
| $T_{VOUT(R)}$                | $V_{OUT}$ Rise Time                   | 10% to 90% $V_{OUT}$ $\uparrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$        | --   | 130  | 170  | $\mu\text{s}$ |
|                              |                                       | 10% to 90% $V_{OUT}$ $\uparrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 1.5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$      | --   | 66   | 86   | $\mu\text{s}$ |
| $T_{VOUT(F)}$                | $V_{OUT}$ Fall Time                   | 90% to 10% $V_{OUT}$ $\downarrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$      | --   | 2.2  | 3.6  | $\mu\text{s}$ |
|                              |                                       | 90% to 10% $V_{OUT}$ $\downarrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 1.5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$    | --   | 2.2  | 3.6  | $\mu\text{s}$ |
| $T_{OFF\_Delay}$             | OFF Delay Time                        | 50% ON to 50% $V_{OUT}$ $\downarrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$   | --   | 3.5  | 5    | $\mu\text{s}$ |
|                              |                                       | 50% ON to 50% $V_{OUT}$ $\downarrow$ ;<br>$T_A = 25\text{ }^\circ\text{C}$ , $V_{IN} = 1.5\text{ V}$ ;<br>$R_{LOAD} = 10\text{ }\Omega$ , $C_{LOAD} = 0.1\text{ }\mu\text{F}$ | --   | 5    | 7    | $\mu\text{s}$ |
| $\overline{T_{FAULT\_LOW}}$  | FAULT Assertion Time                  | Reverse-voltage Detection to $\overline{FAULT}$ $\downarrow$ ; $1.5\text{ V} \leq V_{IN} \leq 5\text{ V}$ ; ON = Low                                                          | --   | 2    | --   | $\mu\text{s}$ |
|                              |                                       | $1.5\text{ V} \leq V_{IN} \leq 5\text{ V}$ ; ON = High                                                                                                                        | --   | 0.5  | --   | $\mu\text{s}$ |
| $\overline{T_{FAULT\_HIGH}}$ | FAULT De-assertion Time               | Delay to $\overline{FAULT}$ $\uparrow$ after fault condition is removed;<br>$1.5\text{ V} \leq V_{IN} \leq 5\text{ V}$ ; ON = Low                                             | --   | 7    | --   | ms            |
|                              |                                       | $1.5\text{ V} \leq V_{IN} \leq 5\text{ V}$ ; ON = High                                                                                                                        | --   | 2    | --   | ms            |
| $\overline{FAULT\_VOL}$      | FAULT Output Low Voltage              | $I_{\overline{FAULT}} = 1\text{ mA}$                                                                                                                                          | --   | --   | 0.2  | V             |

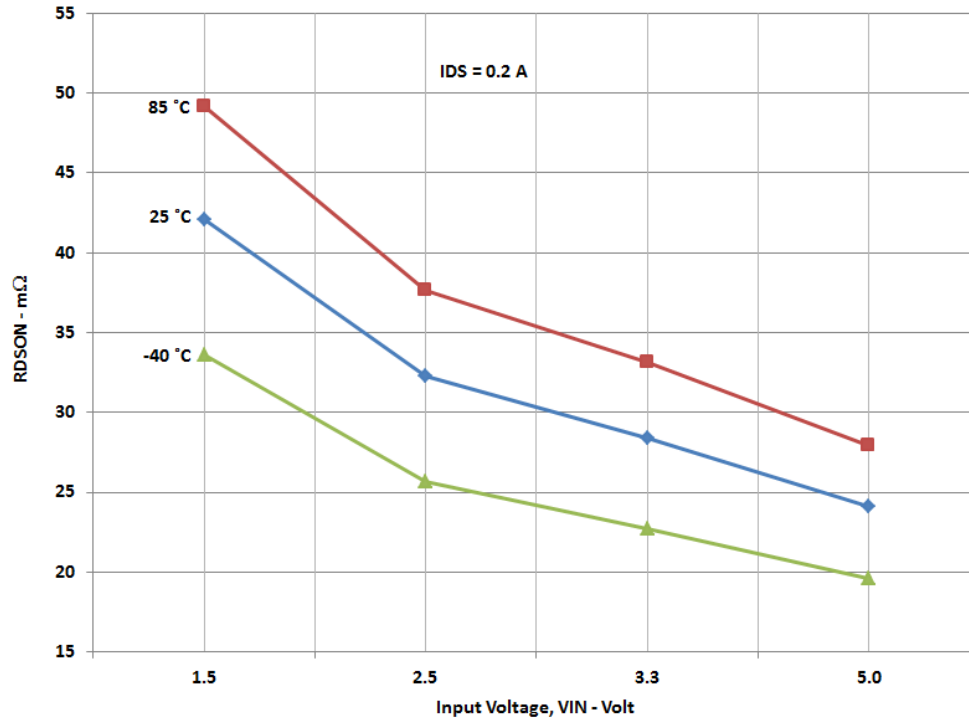


### $T_{\text{Total\_ON}}$ , $T_{\text{ON\_Delay}}$ and Slew Rate Measurement

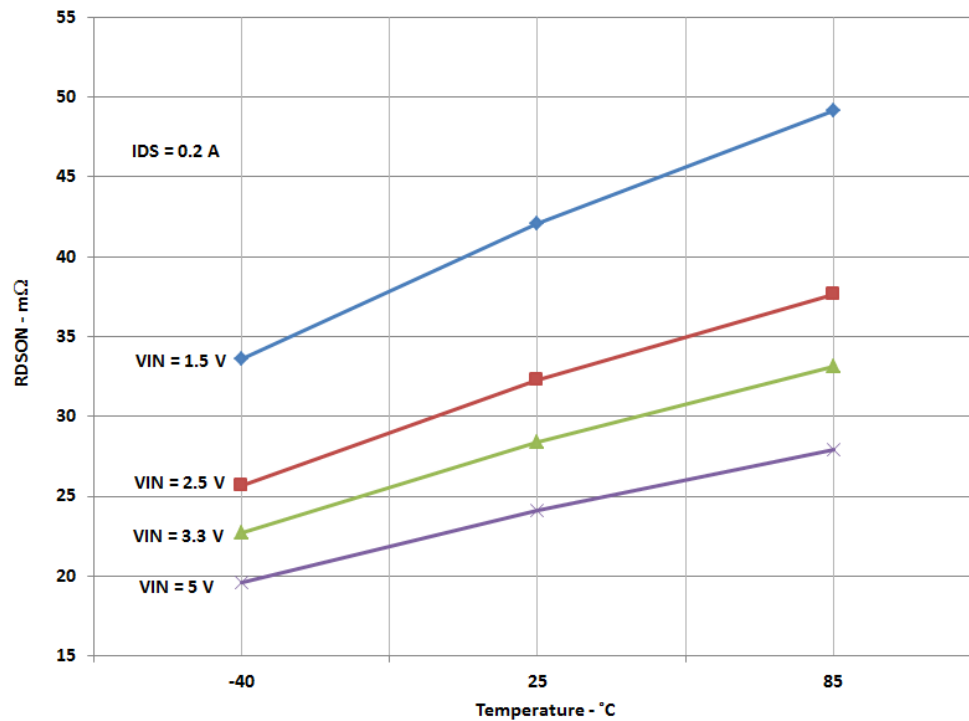




### $R_{DS(on)}$ vs. $V_{IN}$ and Temperature



### $R_{DS(on)}$ vs. Temperature and $V_{IN}$





### V<sub>IN</sub> Inrush Current Details

When the SLG59M1649V is enabled with ON ↑, the power switch closes to charge the V<sub>OUT</sub> output capacitor to V<sub>IN</sub>. The charging current drawn from V<sub>IN</sub> is commonly referred to as “V<sub>IN</sub> inrush current” and can cause the input power source to collapse if the V<sub>IN</sub> inrush current is too high.

Since the V<sub>OUT</sub> rise time of the SLG59M1649V is fixed, V<sub>IN</sub> inrush current is then a function of the output capacitance at V<sub>OUT</sub>. The expression relating V<sub>IN</sub> inrush current, the SLG59M1649V V<sub>OUT</sub> rise time, and C<sub>LOAD</sub> is:

$$V_{IN} \text{ Inrush Current} = C_{LOAD} \times \frac{\Delta V_{OUT}}{V_{OUT} \text{ Rise Time}}$$

where in this expression ΔV<sub>OUT</sub> is equivalent to V<sub>IN</sub> if the initial SLG59M1649V's output voltages are zero.

In the table below are examples of V<sub>IN</sub> inrush currents assuming zero initial charge on C<sub>LOAD</sub> as a function of V<sub>IN</sub>.

| V <sub>IN</sub> | V <sub>OUT</sub> Rise Time | C <sub>LOAD</sub> | Inrush Current |
|-----------------|----------------------------|-------------------|----------------|
| 1.5 V           | 66 μs                      | 0.1 μF            | 2.3 mA         |
| 5 V             | 130 μs                     | 0.1 μF            | 3.8 mA         |

Since the relationship is linear and if C<sub>LOAD</sub> were increased to 1 μF, then the V<sub>IN</sub> inrush currents would be 10x higher in either example. If a large C<sub>LOAD</sub> capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the C<sub>IN</sub>-to-C<sub>LOAD</sub> ratio to minimize V<sub>IN</sub> droop during turn-on.

For other V<sub>OUT</sub> rise time options, please contact Silego for additional information.

### Power Dissipation

The junction temperature of the SLG59M1649V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the R<sub>DS(ON)</sub>-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1649V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = R_{DS(ON)} \times I_{DS}^2$$

where:

PD<sub>TOTAL</sub> = Total package power dissipation, in Watts (W)

R<sub>DS(ON)</sub> = Power MOSFET ON resistance, in Ohms (Ω)

I<sub>DS</sub> = Output current, in Amps (A)

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T<sub>J</sub> = Die junction temperature, in Celsius degrees (°C)

θ<sub>JA</sub> = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T<sub>A</sub> = Ambient temperature, in Celsius degrees (°C)



### Power Dissipation (continued)

In nominal operating mode, the SLG59M1649V's power dissipation can also be calculated by taking into account the voltage drop across each switch ( $V_{IN}-V_{OUT}$ ) and the magnitude of that channel's output current ( $I_{OUT}$ ):

$$PD_{TOTAL} = (V_{IN}-V_{OUT}) \times I_{DS} \text{ or}$$

$$PD_{TOTAL} = (V_{IN} - (R_{LOAD} \times I_{DS})) \times I_{DS}$$

where:

$PD_{TOTAL}$  = Total package power dissipation, in Watts (W)

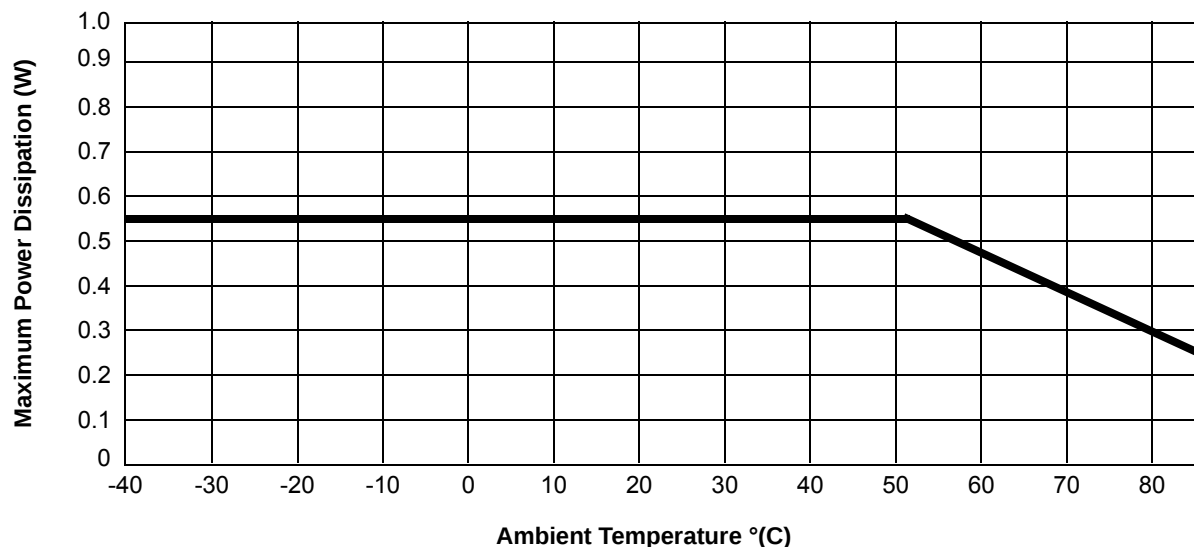
$V_{IN}$  = Input Voltage, in Volts (V)

$R_{LOAD}$  = Output Load Resistance, in Ohms ( $\Omega$ )

$I_{DS}$  = Output current, in Amps (A)

$V_{OUT}$  = Output voltage, or  $R_{LOAD} \times I_{DS}$

### Power Dissipation Derating Curve

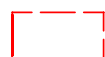


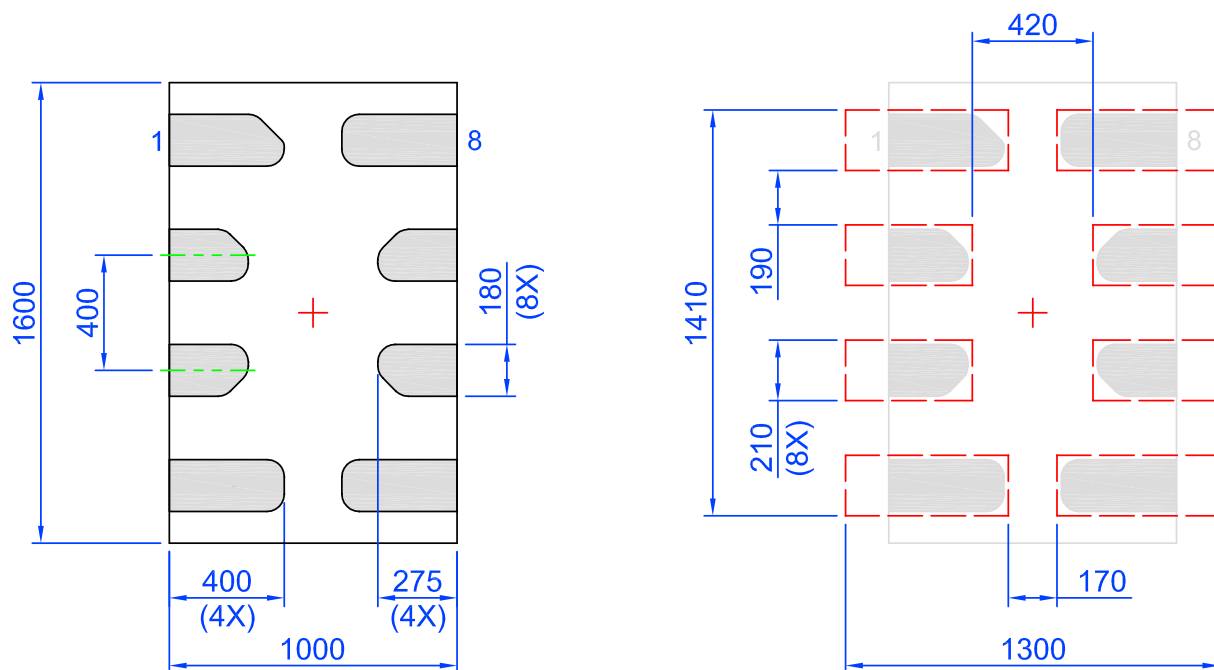
Note: Each  $V_{IN}$ ,  $V_{OUT}$  = 1 in<sup>2</sup> 1.2 oz. copper on FR4



### SLG59M1649V Layout Suggestion

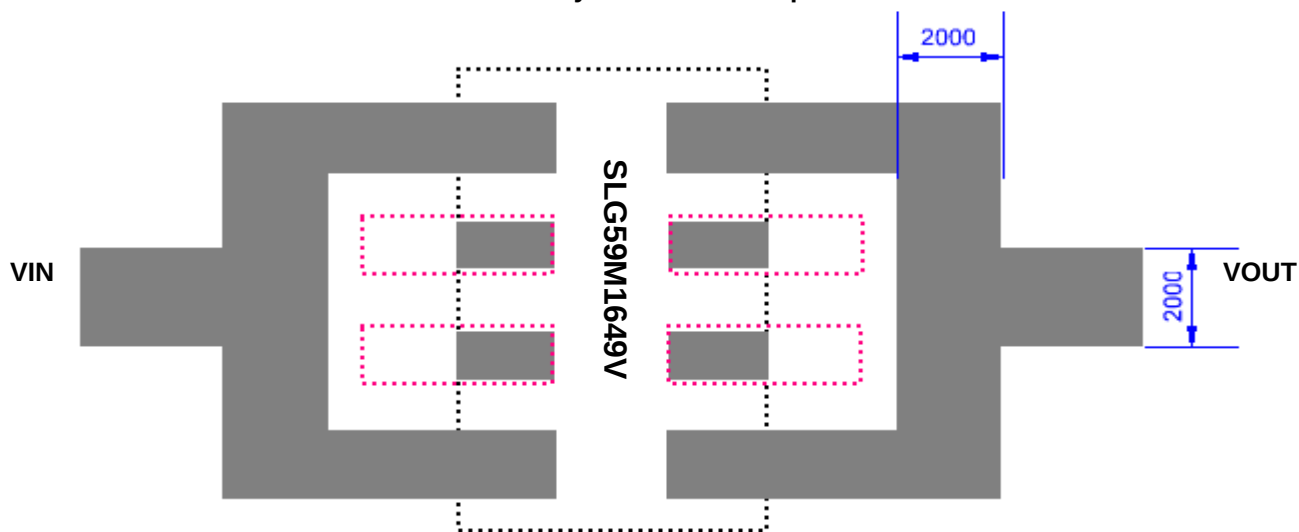
 Exposed Pad  
(PKG face down)

 Recommended Land Pattern  
(PKG face down)



Note: All dimensions shown in micrometers ( $\mu\text{m}$ )

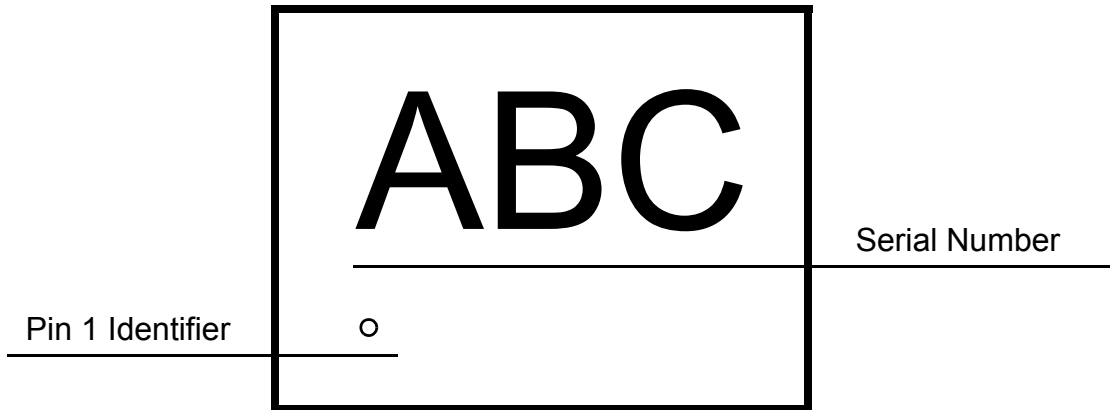
### Recommended PCB Layout for external power traces



Note: All dimensions shown in  $\mu\text{m}$  (micrometers)



### Package Top Marking System Definition

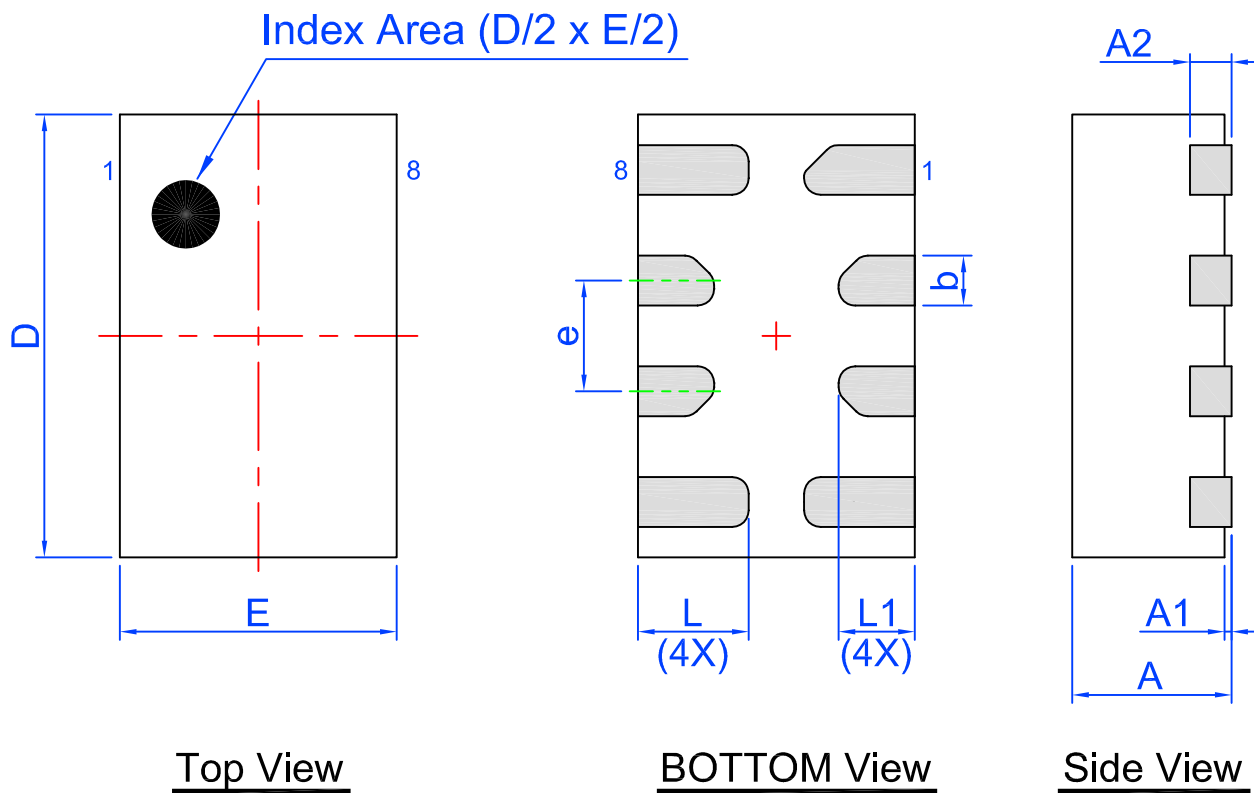


ABC - 3 alphanumeric Part Serial Number  
where A, B, or C can be A-Z and 0-9



### Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

| Symbol | Min      | Nom. | Max   | Symbol | Min   | Nom.  | Max   |
|--------|----------|------|-------|--------|-------|-------|-------|
| A      | 0.50     | 0.55 | 0.60  | D      | 1.55  | 1.60  | 1.65  |
| A1     | 0.005    | -    | 0.050 | E      | 0.95  | 1.00  | 1.05  |
| A2     | 0.10     | 0.15 | 0.20  | L      | 0.35  | 0.40  | 0.45  |
| b      | 0.13     | 0.18 | 0.23  | L1     | 0.225 | 0.275 | 0.325 |
| e      | 0.40 BSC |      |       |        |       |       |       |

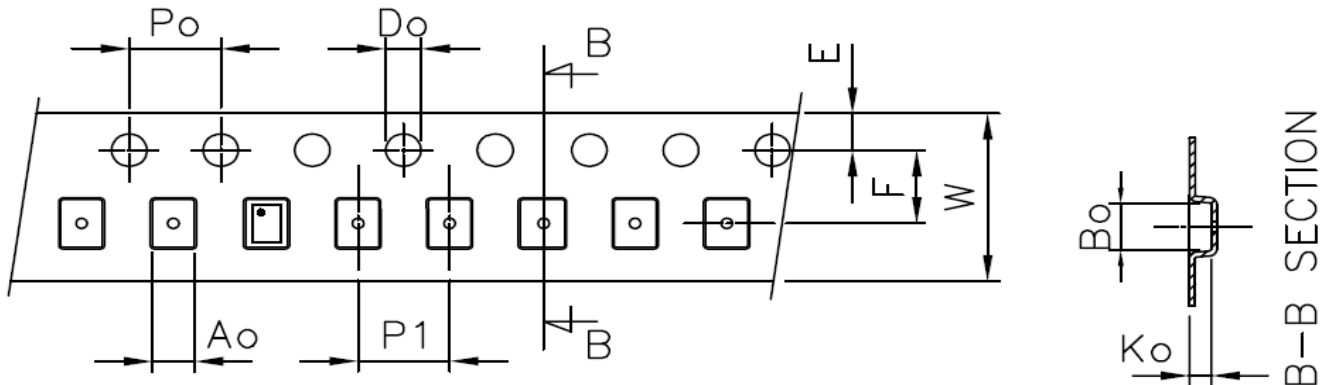


### Tape and Reel Specifications

| Package Type                             | # of Pins | Nominal Package Size [mm] | Max Units |         | Reel & Hub Size [mm] | Leader (min) |             | Trailer (min) |             | Tape Width [mm] | Part Pitch [mm] |
|------------------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
|                                          |           |                           | per Reel  | per Box |                      | Pockets      | Length [mm] | Pockets       | Length [mm] |                 |                 |
| STDFN 8L<br>1x1.6mm<br>0.4P FCD<br>Green | 8         | 1.0 x 1.6 x 0.55          | 3,000     | 3,000   | 178 / 60             | 100          | 400         | 100           | 400         | 8               | 4               |

### Carrier Tape Drawing and Dimensions

| Package Type                             | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
|                                          | A0                | B0               | K0           | P0               | P1           | D0                  | E                       | F                           | W          |
| STDFN 8L<br>1x1.6mm<br>0.4P FCD<br>Green | 1.12              | 1.72             | 0.7          | 4                | 4            | 1.55                | 1.75                    | 3.5                         | 8          |



### Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).



# SILEGO

## SLG59M1649V

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### Revision History

| Date      | Version | Change             |
|-----------|---------|--------------------|
| 2/23/2017 | 1.00    | Production Release |