

OSFP Low-Speed Host Controller

Pin Configuration

General Description

Dialog SLG4AX42396 is a low power and small formfactor bidirectional interface device for host-side lowspeed OSFP standard interfaces based on a Dialog GreenPAK configurable mixed-signal IC. The device is available in a 1.6mm x 2.0mm STQFN package.

Features

- OSFP module specification V1.2 compliant lowspeed host side interface support
- Integrated INT/RSTn and HPW/PRSn detection and generation
- Low Power Consumption
- Pb Free / RoHS Compliant
- Halogen Free
- STQFN 14 Package

14-pin STQFN (Top View)

Table 1: Other Dialog OSFP Compatible Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
SLG4AX42397	OSFP Low-Speed Module Controller

Table 2: Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	H_RSTn	9	HPW_PRS
3	H_INTn_invert	10	INT_RSTn
4	H_RSTn_invert	11	HPW
5	H_PRSn_invert	12	H_LPW
6	HPW_invert	13	H_PRSn
7	RST_L	14	H_INTn



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Table 3: Ordering Information

Part Number	Package Type
SLG4AX42396V	14-pin STQFN
SLG4AX42396VTR	14-pin STQFN - Tape and Reel (3k units)

Block Diagram







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Table 4: Pin Configuration

Pin #	Pin Name	Туре	Pin Description	Polarity
1	VDD	PWR	Supply Voltage	
2	H_RSTn	Digital Input	Host control to GPAK to assert Module Reset	Active Low
3	H_INTn_invert	Digital Input	Input to invert H_INTn default polarity	N/A
4	H_RSTn_invert	Digital Input	Input to invert H_RSTn default polarity	N/A
5	H_PRSn_invert	Digital Input	Input to invert H_PRSn default polarity	N/A
6	HPW_invert	Digital Input	Input to invert HPW default polarity	N/A
7	RST_L	Digital Output	Output to drive INT_RSTn line to reset the Module	Active Low
8	GND	GND	Ground	
9	HPW_PRS	Analog Input/Output	OSFP slow speed signal	
10	INT_RSTn	Analog Input/Output	OSFP slow speed signal	
11	HPW	Digital Output	Output to drive HPW_PRSn line to High Power Mode	Active High
12	H_LPW	Digital Input	Host control to GPAK to assert Module Low Power Mode	Active High
13	H_PRSn	Digital Output	Signal to Host that Module is Present	Active Low
14	H_INTn	Digital Output	Signal to Host that Module sent Interrupt	Active Low



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Table 5: Absolute Maximum Conditions

Symbol	Parameter	Min.	Max.	Unit
V _{DD}	Supply voltage to GND	-0.3	7	V
Vi	Voltage at Input Pin	-0.3	7	V
IMAX	Maximum Average or DC Current (Through VDD or GND pin)		Min. Max. -0.3 7 -0.3 7 90 1.0 -65 150 150 -40 +85 ±2000 ±1300	
l _{ikg}	Input leakage Current (Absolute Value)		1.0	μΑ
TSTRG	Storage Temperature Range	-65	150	°C
TJ	Junction Temperature		150	°C
Тамв	Ambient operating temperature	-40	+85	°C
ESD	ESD Protection (Human Body Model)	±2000		V
	ESD Protection (Charged Device Model)	±1300		V
MSL	Moisture Sensitivity Level		1	

Table 6: Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Тур.	Max.	Unit
Vdd	Supply Voltage		3	3.3	3.6	V
CIN	Input Capacitance			4		pF
la	Quiescent Current	Static inputs and floating outputs		57		μA
VIH	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	0.7*V _{DD}		V _{DD} +0.3	V
VIL	LOW-Level Input Voltage	Logic Input at VDD=3.3V GND- 0.3 0		0.3*V _{DD}	V	
Vон	HIGH-Level Output Voltage	Push-Pull 1X, IOH=3mA at VDD=3.3V	2.7			V
Vol	LOW-Level Output Voltage	Push-Pull 1X, $I_{OL}=3mA$, at0.16 $V_{DD}=3.3V$ 0.16		0.16	V	
Іон	HIGH-Level Output Current (Note 1)	VDD=3.3V Push-Pull 1X, VOH=2.4V at 5.29 VDD=3.3V			mA	
lol	LOW-Level Output Current (Note 1)	Push-Pull 1X, V _{OL} =0.4V, at V _{DD} =3.3V	4.68			mA
		Open Drain NMOS 1X, VoL=0.4V, at VoD=3.3V	12.07			mA
Rpull_up	Internal Pull Up Resistance	Pull up on PINs 12	6		14	kΩ
R _{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PIN 2	6		14	kΩ
VACMP	Analog Comparator 2 and 3 Threshold Voltage	Low to High transition, at temperature -40 +85°C (Note 3)		2496		mV



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Symbol	Parameter	Condition/Note	Min.	Тур.	Max.	Unit
Ts∪	Startup Time	From VDD rising past PONTHR		1	2	ms
PONTHR	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
POFF _{THR}	Power Off Threshold	V _{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

Note:

1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

2. The GreenPAK's power rails are divided in two sides.

3. Guaranteed by Design.



Description

The SLG4AX42396 OSFP Low-Speed Host Controller device contains one pair of INT_RSTn and HPW_PRS signals transceivers.

INT_RSTn is a bi-directional dual function signal that allows the module to raise an interrupt to the host and allows the host to reset the module. The link uses multi-level signaling to provide direct signal control in both directions. The host signals a RESET to the module when M_RSTn is asserted low. The module (SLG4AX42397) signals an interrupt to the host when M_INT_L is asserted low.

HPW_PRS is another bi-directional dual function signal that allows the host to signal Low Power mode and the module (SLG4AX42397) to indicate Module Present using multi-level signaling to provide direct signal control in both directions. The host signals the module to enter the low power state when M_RSTn is asserted low.

For ease of system use, four invert input pins have been added to invert the default polarity of output signals. Refer to Table 7.

Invert Pin Name	Status	Output Polarity		
H_INTn_invert	Low	Active Low		
	High	Active High		
H_RSTn_invert	Low	Active Low		
	High	Active High		
H_PRSn_invert	Low	Active Low		
	High	Active High		
HPW_invert	Low	Active High		
	High	Active Low		

Table 7: Output Polarity Control

Table 8: Other Dialog OSFP Compatible Parts

Part Number	Description
SLG4AC42401	Dual OSFP Low-Speed Host Controller
SLG4AX42396	OSFP Low-Speed Host Controller
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Typical Application Circuit



Figure 2: SLG4AX42396 Typical Application Circuit



Package Top Marking



Figure 3. Package Top Marking

Table 9: Part Information

Datasheet Revision	Programming Code Number	Locked Status	Checksum	Part Code	Revision	Date
0.11	004	U	0xAF238603			07/25/2018

Lock coverage for this part is indicated by $\sqrt{}$, from one of the following options:

Table 10: Lock Status

Lock Status	
Х	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.



Package Drawing and Dimensions



Figure 4. SLG4AX42396 Package Drawing and Dimensions



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Table 11: Tape and Reel Specification

Package Nominal Max Units		Units	Reel & Hub Size	Leader (min)		Trailer (min)		Tape Pa Width Pi	Part Pitch	
	Size [mm]	per Reel	per Box	[mm]	Pockets	Length [mm]	Pockets	Length [mm]	[mm]	[mm]
STQFN 14L 1.6x2mm 0.4P FC Green	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Table 12: Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	К0	P0	P1	D0	E	F	w
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8





Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm³ (nominal) for STQFN 14L Package. More information can be found at <u>www.jedec.org.</u>



Recommended Land Pattern



Unit: um

Figure 6. SLG4AX42396 Recommended Land Pattern



Table 13: Datasheet Revision History

Date	Version	Change
03/30/2018	0.10	New design for SLG46855 chip
07/25/2018	0.11	Updated DS formatting



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Contacting Dialog Semiconductor

United Kingdom (Headquarters) Dialog Semiconductor (UK) LTD Phone: +44 1793 757700

Germany

Dialog Semiconductor GmbH Phone: +49 7021 805-0

The Netherlands

Dialog Semiconductor B.V. Phone: +31 73 640 8822

Email: enquiry@diasemi.com North America Dialog Semiconductor Inc.

Phone: +1 408 845 8500

Japan

Dialog Semiconductor K. K. Phone: +81 3 5769 5100

Taiwan

Dialog Semiconductor Taiwan Phone: +886 281 786 222

Web site:

www.dialog-semiconductor.com

Hong Kong Dialog Semiconductor Hong Kong Phone: +852 2607 4271

Korea Dialog Semiconductor Korea Phone: +82 2 3469 8200

China (Shenzhen) Dialog Semiconductor China Phone: +86 755 2981 3669

China (Shanghai) Dialog Semiconductor China Phone: +86 21 5424 9058