SLG47910 Datasheet

1K LUT Digital Configurable Array

Description

The SLG47910 is a small size, low power component for common FPGA applications. The user creates their circuit design by writing RTL Verilog or using the graphical mode to configure the interconnections, logic blocks, and input/output pins of the SLG47910. This highly versatile device allows a wide variety of FPGA applications to be designed.

Features

- Dense Array of Configurable Logic
  - 1120 5-bit Look-Up Tables (LUTs)
  - 1120 D-type Flip Flops (DFFs)
  - 5 kb distributed Static Random-Access Memory (SRAM)
  - 32 kb embedded SRAM (BRAM)
  - Configurable through onboard NVM and/or SPI interface
- 50 MHz On-chip Oscillator (OSC)
- Phase-Locked Loop (PLL)
  - Clock from external source or internal Oscillator
- Power Supply
  - V_{DDIO}: 1.71 V to 3.465 V
  - V_{DDC}: 1.1 V ± 5 %
- Power-On-Reset (POR)
- General Purpose Input Output (GPIO) Count
  - 19 GPIOs + 2 GPIs in STQFN Packaging
- Configuration Modes
  - Internal One-Time Programmable (OTP) Non-Volatile Memory (NVM)
  - External SPI Flash Memory with power-down option
  - External SPI Microcontroller (MCU)
- Maximum Configuration Bitstream Security (OTP Mode)
- Reset and Low Power Sleep Functionality with data retention (GPO, FPGA Core, BRAMs)
- Operating Temperature Range: -40 °C to +85 °C
- RoHS Compliant/Halogen-Free Package
  - 24-pin STQFN: 3.0 mm x 3.0 mm x 0.55 mm, 0.4 mm pitch

Applications

- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics
- Notebooks and Tablet PCs
- Industrial Applications

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1. Overview

The components of the SLG47910 are shown in the Block Diagram (Figure 1).

1.1 Block Diagram

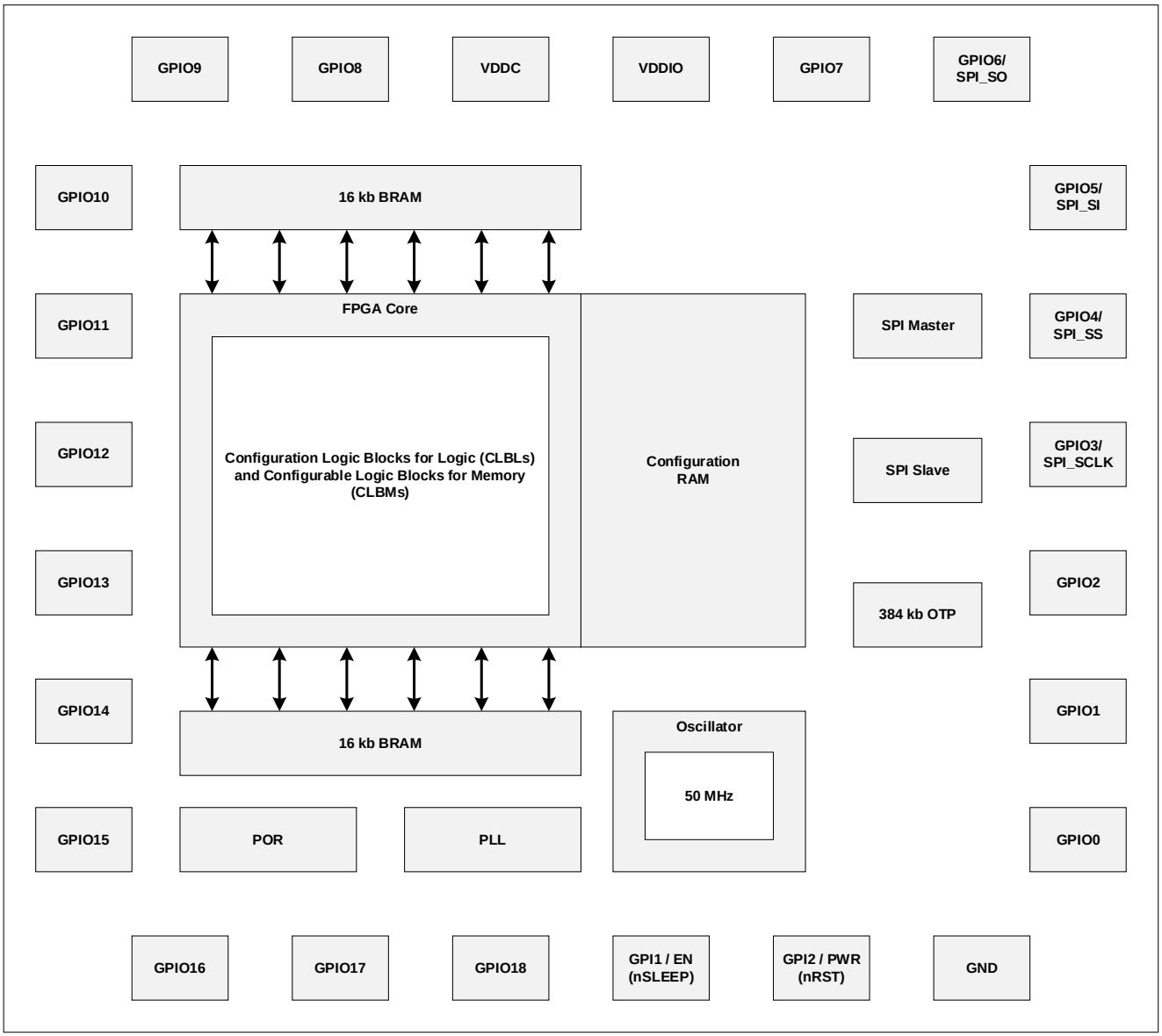


Figure 1. Block Diagram

1.2 Block Description

GPIO

The GPIO pins are general-purpose digital input-output circuits that can be programmed as inputs, a push-pull output, an open drain or bidirectional. They contain configurable output buffers with different strengths and input buffers with two types of pull-up resistors. The GPIOs connect to the FPGA Core via an interface of Input Output Blocks (IOBs). Output enable (OE) signal is available for each GPIO. If the GPIO is configured as an output, the signal is also received by the input buffer. GPIO [6:3] are used to configure the device in SPI modes.

BRAM

The 32 kb embedded SRAM is separated into two 16kb blocks (BRAM). One BRAM consists of four SRAM instances. The SRAM instance is a synchronous one write port, and one read port memory and can be configured as a dual port SRAM. Two-port addressing allows simultaneous reading and writing of two different address locations. Positive edge-triggered input latches are on the ports for address, data, and enable signals. Each SRAM instance can be programmed in different width and depth configurations. The width and depth configurations are the same for the write and read ports and can be changed asynchronously by IOB signals. Four SRAM instances have shared clock paths for read ports and one more for write ports. FPGA Core has a separate interface with North and South 16k BRAMs. The BRAM does not connect directly with the GPIO.

FPGA Core

The FPGA Core consists of FPGA fabric and a ring of interface blocks called IOBs. The IOBs are used to communicate between the FPGA fabric and the other embedded blocks. The FPGA fabric consists of an Interconnect Matrix, an array of Configurable Logic Blocks (CLBs), Configuration Registers, and a Global Clock Tree. Each CLB contains LUTs, DFFs, and a clock network, which are used to implement user-defined logic functions. In addition, some CLBs in the Array can be configured in Embedded Memory Mode (EMM) and Shift Register Mode (SRM). These modes are used to implement distributed RAM. The Configuration Registers are a volatile type of memory that stores the FPGA design after the chip configuration. The Configuration Registers can be loaded from the OTP or SPI modes.

OTP Block

The 384 kb OTP is used to store user defined configurations. The 384 kb OTP is a One Time Programmable NVM block that allows users to store the FPGA design once the design has been finalized. The device will load the FPGA design from OTP during the power-up sequence.

Power-on Reset

The POR circuit monitors the VDDIO and VDDC power supplies and keeps the SLG47910 in reset state upon power up until V_{DDIO} and V_{DDC} are within the specified voltage ranges. The POR reset will occur if power rails drop below the specified voltage range after the device has been powered up. A POR reset will tri-state all GPIOs.

SPI

The SPI Master and SPI Slave are dedicated circuits that allow the Configuration RAM to be programmed. The SPI Master and SPI Slave connect to GPIO3 (SPI_SCLK), GPIO4 (SPI_SS), GPIO5 (SPI_SI), and GPIO6 (SPI_SO). This block cannot be accessed by user logic due to Hard IP.

Clocking

SLG47910 has three clocking sources: PLL, OSC, and LaC (Logic-As-Clock).

The PLL and Oscillator can be used to generate internal clocks. The PLL receives clock sources from the Oscillator or through GPIO2. The PLL can generate a wide range of frequencies. The Oscillator frequency is 50 MHz. The OSC, PLL, and LaCs can drive the BRAM and the FPGA Core. GPIO can be used to input external Logic-As -Clock (LaC) with the help of the IO Planner in the software. LaC can be used to route logic signal from the core to the clock tree input.

Note: Only two clock domains are supported simultaneously.

EN/PWR

The EN (nSLEEP) and PWR (nRST) inputs are used to control the power consumption as shown in Table 1.

Table 1. Block Control

PWR (nRST)	EN (nSLEEP)	Description
0	X	**Device Reset/Off State:** ▪ Configuration of FPGA Core is not retained, and Array Power is gated ▪ PLL, OSC, and OTP memory are disabled ▪ BRAM data is not retained unless BRAM Keep Register value at Reset = 1 (see Reg [193] in A Register Definitions) ▪ GPIO in Hi-Z state and not retained unless REG_GPIO_KEEP = 1.
1	0	**Lower Power/Retention State:** ▪ Configuration of FPGA Core is retained, and Array Power is gated ▪ PLL, OSC and OTP memory are disabled ▪ BRAM data is retained if BRAM (0..3) Register Enable = 0 (see Reg[320] in A Register Definitions) and if BRAM (4..7) Register Enable = 0 (see Reg[321] in A Register Definitions) ▪ GPIO is not in Hi-Z state and data is retained.
1	1	**Configuration Mode:** ▪ From internal OTP ▪ From external SPI ▪ From MCU interface ▪ FPGA Core, GPIO, BRAM, PLL, and OSC are controlled by IOBs.

2. Pin Information

2.1 Pin Assignments - STQFN

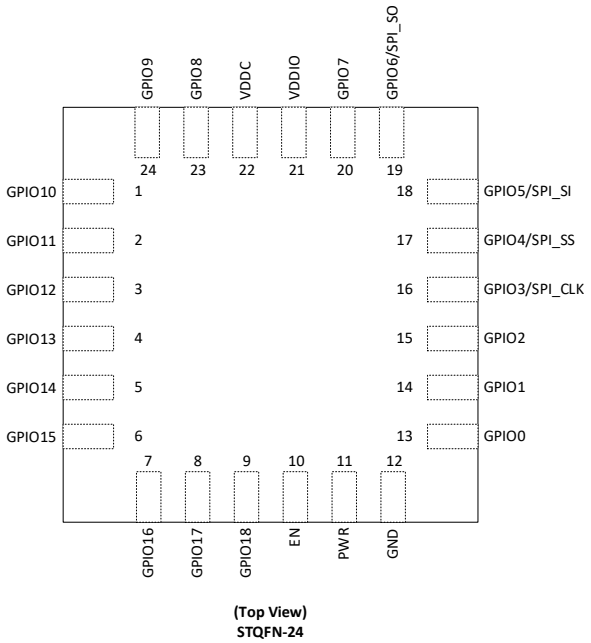


Figure 2. Pin Assignments for 24-pin STQFN

Table 2. STQFN-24 Pin Assignments

Pin #	Signal Name	Pin Functions
1	GPIO10	General Purpose IO
2	GPIO11	General Purpose IO
3	GPIO12	General Purpose IO
4	GPIO13	General Purpose IO
5	GPIO14	General Purpose IO
6	GPIO15	General Purpose IO
7	GPIO16	General Purpose IO
8	GPIO17	General Purpose IO
9	GPIO18	General Purpose IO
10	EN (nSLEEP)	Sleep Mode Control Input (active LO)
11	PWR (nRST)	Reset Mode Control Input (active LO)
12	GND	Ground
13	GPIO0	General Purpose IO
14	GPIO1	General Purpose IO
15	GPIO2	General Purpose IO or PLL refCLK Input
16	GPIO3/SPI_CLK	General Purpose IO or SPI Serial Clock
17	GPIO4/SPI_SS	General Purpose IO or SPI Slave Select
18	GPIO5/SPI_SI	General Purpose IO or SPI Serial Input
19	GPIO6/SPI_SO	General Purpose IO or SPI Serial Output/Config
20	GPIO7	General Purpose IO
21	VDDIO	Power for IO
22	VDDC	Power for Core
23	GPIO8	General Purpose IO
24	GPIO9	General Purpose IO

2.2 Pin Descriptions

Table 3. Pin Descriptions

STQFN Pin No	Pin Name	Secondary Function during Boot Sequence		
		OTP Mode	SPI Mode	MCU Mode
1	GPIO10	--	--	--
2	GPIO11	--	--	--
3	GPIO12	--	--	--
4	GPIO13	--	--	--
5	GPIO14	--	--	--
6	GPIO15	--	--	--
7	GPIO16	--	--	--
8	GPIO17	--	--	--
9	GPIO18	--	--	--
10	EN	--	--	--
11	PWR	--	--	--
12	VSS	--	--	--
13	GPIO0	--	--	--
14	GPIO1	--	--	--
15	GPIO2	--	--	--
16	GPIO3	--	SPI_SCLK	SPI_SCLK
17	GPIO4	--	SPI_SS	SPI_SS
18	GPIO5	--	SPI_SI (MISO)	SPI_SI (MOSI)
19	GPIO6	--	SPI_SO (MOSI)	SPI_SO (MISO)/CONFIG
20	GPIO7	--	--	--
21	VDDIO	--	--	--
22	VDDC	--	--	--
23	PIO8	--	--	--
24	GPIO9	--	--	--

[1] Note: Green cells correspond to Input signals and orange cells correspond to output signals

2.3 Signal Descriptions

2.3.1 Power and Control Pins

Table 4. Power and Control Pins

Pin Name (Signal Name)	Function	Description
VDDC	Power	Core Power Supply
VDDIO	Power	Power for IO in Bank
GND	Ground	Ground
EN (nSLEEP)	Sleep	Retention Function
PWR (nRST)	Reset	Reset Signal

2.3.2 Configuration Pins

Table 5. Configuration Pins

Signal Name		Function	IO	Description
Primary	Secondary			
GPIO3	SPI_SCLK	Configuration SPI Mode	Clock Output	In Master SPI Mode, this pin outputs the clock to external SPI memory.
		Configuration MCU Mode	Clock Input	In Slave SPI (MCU) Mode, this pin inputs the clock from external processor.
	--	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO4	SPI_SS	Configuration SPI Mode	Input	Depending on the SPI and Slave settings, the SPI_SS in is used to select programming mode SPI.
		Configuration MCU Mode	Output	Depending on the SPI and Slave settings, the SPI_SS in is used to select programming MCU load mode.
	--	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function
GPIO5	SPI_SO (MISO)	Configuration SPI Mode	Input	MISO is a data pin. This pin is used to transmit data from the slave to the master. Whenever the slave sends data, that data will be collected over the MISO pin by the master.
	SPI_SI (MOSI)	Configuration MCU Mode		MOSI is a data pin. This pin is used to transmit data from the master to the slave device. Whenever the master sends data, that data will be collected over the MOSI pin by the slave.
	--	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function
GPIO6	SPI_SO (MOSI)	Configuration SPI Mode	Output	MOSI is a data pin. This pin is used to transmit data from the master to the slave device. Whenever the master sends data, that data will be collected over the MOSI pin by the slave.
	SPI_SI (MISO) / CONFIG	Configuration MCU Mode		MISO is a data pin. This pin is used to transmit data from the slave to the master. Whenever the slave sends data, that data will be collected over the MISO pin by the master. In MCU Mode, the CONFIG signal is flagged at this pin.
	--	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function

2.3.3 Global Pins

Table 6. Global Pins

Signal Name	Function	IO	Description
GPIO [1:0]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
GPIO2	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.
	PLL ref CLK	Input	This IO can be programmed as a reference clock for the device in user function when receiving clock from PLL.
GPIO [18:7]	General IO	IO	In user mode, after configuration, this pin can be programmed as general IO in user function.

3. Specifications

3.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to the absolute maximum conditions for extended periods may affect the device reliability.

Parameter	Conditions	Min	Max	Unit
Supply Voltage (V_{DDC})	Non-operational	-0.3	1.21	V
Supply Voltage (V_{DDIO})		-0.3	3.465	V
Voltage at Digital Input Pins	I_{OL} = -100 µA	-0.3	3.465	V
Maximum RMS or DC current (through single GPIO pin)	Push-pull 1x	--	10	mA
	Push-pull 2x	--	20	mA
	Open-drain 1x	--	9	mA
	Open-drain 2x	--	18	mA
Current at Digital Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
I_{VDDIO} DC Current through V_{DDIO} Pin [1]		--	200	mA
I_{VDDC} DC Current though V_{DDC} Pin [1]		--	200	mA
I_{GND} DC Current through GND [1]		--	200	mA
Continuous Power Dissipation (JESD51-7, T_A = +85 ºC)	QFN-24 (Derate 17.9 mW/°C above T_A = +85 ºC)	--	1161	mW
Storage Temperature Range		-65	+150	°C
Junction Temperature		--	+150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

[1] Package limits.

3.2 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage (V_{DDC})	1.045	1.1	1.155	V
Supply Voltage (V_{DDIO})	1.710	2.5	3.465	V
Operating Junction Temperature (T_J) [1]	-40	+25	+85	°C
Capacitor Value at V_{DDC} and V_{DDIO}	0.1	--	--	µF

[1] Parameters were measured with $T_A = T_J$.

3.3 Electrical Specifications

3.3.1 GPIOs Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ±5%, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage Current	I_{I_LKG}	V_{DDIO} = 3.465 V, V_{IN} = 0 to V_{DDIO}	-600	--	+600	nA
Max Absolute Data Skew – Input Paths	$T_{skew\_di\_pin}$	V_{DDC} = 1.1 ±5 %, V_{DDIO} = 1.71 V	1.51	3.25	6.23	ns
Max Absolute Data Skew – Output Paths	$T_{skew\_do\_pin}$	V_{DDC} = 1.1 ±5 %, V_{DDIO} = 1.71 V	1.65	3.62	7.96	ns
Input/Output Pin Capacitance	C_{IO_PIN}	T_J = +25 °C $C_{IO\_PIN} = C_{GPIO} + C_{PAD} + C_{PIN}$	--	3.6	--	pF
V_{DDIO} = 1.8 V ±5 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		--	0.28	4.37	µA
HIGH-level Input Voltage	V_{IH}	Logic Input HIGH	0.65 x V_{DDIO}	--	3.465	V
LOW-level Input Voltage	V_{IL}	Logic Input LOW	GND - 0.3 V	--	0.35 x V_{DDIO}	V
HIGH-level Output Voltage	V_{OH}	Push-pull 1x, I_{OH} = 0.5 mA	0.982 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 1 mA	0.965 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 2 mA	0.928 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 0.5 mA	0.991 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 1 mA	0.982 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 2 mA	0.963 x V_{DDIO}	--	--	V
LOW-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 0.5 mA	--	--	0.029	V
		Push-pull 1x, I_{OL} = 1 mA	--	--	0.059	V
		Push-pull 1x, I_{OL} = 2 mA	--	--	0.12	V
		Push-pull 2x, I_{OL} = 0.5 mA	--	--	0.015	V
		Push-pull 2x, I_{OL} = 1 mA	--	--	0.03	V
		Push-pull 2x, I_{OL} = 2 mA	--	--	0.061	V
		Open-drain 1x, I_{OL} = 2 mA	--	--	0.121	V
		Open-drain 2x. I_{OL} = 2 mA	--	--	0.061	V
HIGH-level Output Current	I_{OH}	Push-pull 1x, V_{OH} = 1.35 V	4.5	--	--	mA
		Push-pull 2x, V_{OH} = 1.35 V	8.7	--	--	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-level Output Current	I_{OL}	Push-pull 1x, V_{OL} = 0.45 V	5.1	--	--	mA
		Push-pull 2x, V_{OL} = 0.45 V	9.9	--	--	mA
		Open-drain 1x, V_{OL} = 0.45 V	5.1	--	--	mA
		Open-drain 2x, V_{OL} = 0.45 V	9.9	--	--	mA
Max GPIO output frequency	F_{IO_MAX}	Push-pull 1x, C_{LOAD} = 10 pF	50	110	180	MHz
		Push-pull 2x, C_{LOAD} = 10 pF	120	195	280	MHz
V_{DDIO} = 2.5 V ±10 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		--	1.44	6.93	µA
HIGH-level Input Voltage	V_{IH}	Logic Input HIGH	1.7	--	3.465	V
LOW-level Input Voltage	V_{IL}	Logic Input LOW	GND – 0.3 V	--	0.35 x V_{DDIO}	V
HIGH-level Output Voltage	V_{OH}	Push-pull 1x, I_{OH} = 0.5 mA	0.989 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 1 mA	0.979 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 2 mA	0.958 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 0.5 mA	0.994 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 1 mA	0.989 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 2 mA	0.978 x V_{DDIO}	--	--	V
LOW-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 0.5 mA	--	--	0.023	V
		Push-pull 1x, I_{OL} = 1 mA	--	--	0.046	V
		Push-pull 1x, I_{OL} = 2 mA	--	--	0.092	V
		Push-pull 2x, I_{OL} = 0.5 mA	--	--	0.012	V
		Push-pull 2x, I_{OL} = 1 mA	--	--	0.024	V
		Push-pull 2x, I_{OL} = 2 mA	--	--	0.047	V
		Open-drain 1x, I_{OL} = 2 mA	--	--	0.092	V
		Open-drain 2x, I_{OL} = 2 mA	--	--	0.047	V
HIGH-level Output Current	I_{OH}	Push-pull 1x, V_{OH} = 1.7 V	8.8	--	--	mA
		Push-pull 2x, V_{OH} = 1.7 V	16.6	--	--	mA
LOW-level Output Current	I_{OL}	Push-pull 1x, V_{OL} = 0.7 V	9.9	--	--	mA
		Push-pull 2x, V_{OL} = 0.7 V	19.4	--	--	mA
		Open-drain 1x, V_{OL} = 0.7 V	9.9	--	--	mA
		Open-drain 2x, V_{OL} = 0.7 V	19.4	--	--	mA
Max GPIO output Frequency	F_{IO_MAX}	Push-pull 1x, C_{LOAD} = 10 pF	75	160	250	MHz
		Push-pull 2x, C_{LOAD} = 10 pF	165	235	300	MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
V_{DDIO} = 3.3 V ± 5 %						
V_{DDIO} Leakage Current	I_{DDIO_LKG}		--	4.41	11.80	µA
HIGH-level Input Voltage	V_{IH}	Logic Input HIGH	2.0	--	3.465	V
LOW-level Input Voltage	V_{IL}	Logic Input LOW	GND – 0.3 V	--	0.35 x V_{DDIO}	V
HIGH-level Output Voltage	V_{OH}	Push-pull 1x, I_{OH} = 0.5 mA	0.993 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 1 mA	0.987 x V_{DDIO}	--	--	V
		Push-pull 1x, I_{OH} = 2 mA	0.974 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 0.5 mA	0.996 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 1 mA	0.993 x V_{DDIO}	--	--	V
		Push-pull 2x, I_{OH} = 2 mA	0.986 x V_{DDIO}	--	--	V
LOW-level Output Voltage	V_{OL}	Push-pull 1x, I_{OL} = 0.5 mA	--	--	0.020	V
		Push-pull 1x, I_{OL} = 1 mA	--	--	0.038	V
		Push-pull 1x, I_{OL} = 2 mA	--	--	0.077	V
		Push-pull 2x, I_{OL} = 0.5 mA	--	--	0.010	V
		Push-pull 2x, I_{OL} = 1 mA	--	--	0.020	V
		Push-pull 2x, I_{OL} = 2 mA	--	--	0.040	V
		Open-drain 1x, I_{OL} = 2 mA	--	--	0.077	V
		Open-drain 2x, I_{OL} = 2 mA	--	--	0.040	V
HIGH-level Output Current	I_{OH}	Push-pull 1x, V_{OH} = 2.4 V	12.3	--	--	mA
		Push-pull 2x, V_{OH} = 2.4 V	22.7	--	--	mA
LOW-level Output Current	I_{OL}	Push-pull 1x, V_{OL} = 0.4 V	8.1	--	--	mA
		Push-pull 2x, V_{OL} = 0.4 V	15.5	--	--	mA
		Open-drain 1x, V_{OL} = 0.4 V	8.1	--	--	mA
		Open-drain 2x, V_{OL} = 0.4 V	15.5	--	--	mA
Max GPIO output Frequency	F_{IO_MAX}	Push-pull 1x, C_{LOAD} = 10 pF	110	212	304	MHz
		Push-pull 2x, C_{LOAD} = 10 pF	189	281	363	MHz
[1] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.						

3.3.2 GPIO Pull-Up Resistance Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ±5%, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Pull-up 1x (single resistor)	R_{PU1}	V_{DDIO} = 1.71 V to 1.98 V	124	190	256	kΩ
		V_{DDIO} = 2.25 V to 2.75 V	79	119	165	kΩ
		V_{DDIO} = 3.135 V to 3.465 V	62	87	115	kΩ
Pull-up 2x (two resistors in parallel)	R_{PU2}	V_{DDIO} = 1.71 V to 1.98 V	64	95	127	kΩ
		V_{DDIO} = 2.25 V to 2.75 V	40	59	82	kΩ
		V_{DDIO} = 3.135 V to 3.465 V	32	44	57	kΩ

3.3.3 PLL Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 ±5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Clock Frequency	f_{IN}		5	--	500	MHz
Output Clock Frequency	f_{OUT}		10	--	2000 [1]	MHz
VCO Frequency	f_{VCO}		500	--	2000	MHz
Output Duty Cycle	f_{PLL_DC}	f_{OUT} VCO at any Frequency	44.2	48.9	51.6	%
Number of PFD Cycles for PLL to Lock [2]	n_{PLL_LOCK}		--	600	900	cycles
PFD Frequency Range	f_{PFD}		5	--	f_{VCO}/16	MHz
Peak to Peak Period Jitter	$t_{JIT\_10.2}$	f_{OUT} = 10.2 MHz	--	210	681	ps
Peak to Peak Period Jitter	$t_{JIT\_55.6}$	f_{OUT} = 55.6 MHz	--	106	307	ps
Peak to Peak Period Jitter	t_{JIT_100}	f_{OUT} = 100 MHz	--	75	232	ps
Peak to Peak Period Jitter	t_{JIT_115}	f_{OUT} = 125 MHz	--	84	363	ps

[1] The PLL block can support this range but in practice the frequency would be much lower due to peripheral logic limitations.

[2] PLL Lock signal will go high after 256 consecutive no slip cycles.

3.3.4 Oscillator Specifications

V_{DDIO} = 2.5 V ± 10 %, V_{DDC} = 1.1 V ±5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Frequency	f_{OSC_50}	T_J = +25 °C	46.752	50.0	52.549	MHz
		T_J = -40 °C to +85 °C	43.495	50.0	54.110	
Output Duty Cycle	$f_{OSC\_DC\_50}$	T_J = -40 °C to +85 °C	35.1	48.2	61.2	%
Initial Setting Time	$f_{OSC\_SET\_50}$	T_J = +25 °C	0.59	105	182	µs
		T_J = -40 °C to +85 °C	0.46	105	213	
Period Jitter (peak-to-peak)	T_{PJIT_50}	T_J = +25 °C	68	135	222	ps
		T_J = -40 °C to +85 °C	47	135	277	ps

3.3.5 Power-On-Reset Specifications

T_A = -40 °C to +85 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{DDC} power-on-reset delay	$T_{VDDC\_POR\_DELAY}$	V_{DDC} ramp = 300 µs...10 ms, V_{DDIO} = 2.5 V ±10%	0.921	1.446	1.888	ms
V_{DDIO} power-on-reset delay	$T_{VDDIO\_POR\_DELAY}$	V_{DDIO} ramp = 300 µs...10 ms, V_{DDC} = 1.1 V	0.829	1.371	1.872	ms
V_{DDC} power-on threshold	$V_{POR\_VDDC\_ON}$	V_{DDIO} = 2.5 V	0.887	0.906	0.98	V
V_{DDC} power-off threshold	$V_{POR\_VDDC\_OFF}$	V_{DDIO} = 2.5 V	0.328	0.693	0.95	V
V_{DDIO} power-on threshold	$V_{POR\_VDDIO\_ON}$	V_{DDC} = 1.1 V	1.595	1.628	1.67	V
V_{DDIO} power-off threshold	$V_{POR\_VDDIO\_OFF}$	V_{DDC} = 1.1 V	0.91	1.109	1.293	V
V_{DDC}/V_{DDIO} Supply ramp	T_{POR_VRAMP}	V_{DDC} = 0 to 1.1 V ±5 %, V_{DDIO} = 0 to (1.71 V…3.465 V),	0.3	--	10	ms
Note: Refer to section 7 Power-Up and Configuration Sequence for more information.						

3.3.6 Estimated Current Consumption Values

T_A = +25 °C, V_{DDIO} = 2.5 V ±10 %, V_{DDC} = 1.1 V ±5 %, unless otherwise specified.

Parameter	Symbol	Note	Typ	Unit
Current	I_{DDC}	OSC 50 MHz	422	µA
		PLL Active Current Consumption (f_{VCO} = 500 MHz)	610	µA
		PLL Active Current Consumption (f_{VCO} = 2000 MHz)	2820	µA
		Single BRAM Block Quiescent Power (BRAM_PG = LOW)	5.76	µA
		Single BRAM Slice Read (RCLK = 40 MHz)	113.87	µA
		Single BRAM Slice Write (RCLK = 40 MHz)	92.922	µA
		Single BRAM Block RCLK Tree (RCLK = 40 MHz)	100	µA
		Single BRAM Block WCLK Tree (WCLK = 40 MHz)	85	µA
		Average I_{VDDC} Current consumption during FPGA Core with 90+% utilization at 100 MHz (V_{DDIO} = 1.8 V) [1]	47	mA
[1] Device Utilization is 90+ % of LUTs/FF in each Slice of CLB (power-virus); PWR = 1 and EN = 1, BRAM – disabled, f = 100 MHz).				

3.3.7 Timing Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ±5 %, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Configuration						
Configuration Time. Time from PWR (nRST) release (set HIGH) to device configuration done	t_{CONF_OTP}	OTP Configuration Mode	--	19	--	ms
	t_{CONF_MCU}	MCU Configuration mode, F_{CLK_SPI} = 16 MHz	--	25	--	ms
	t_{CONF_SPI}	SPI Master Configuration Mode	--	33	--	ms
SPI Master Configuration (Config from SPI Flash Memory)						
Master Clock Frequency during Configuration	f_{CLKM}	--	--	12.5	13.4	MHz
Master Clock Duty Cycle during Configuration	$CLKM_{DC}$	--	40	50	60	%
Delay from PWR (nRST) release to SPI_SSn Falling Edge	t_{PORT_MCLK}	--	--	205	--	µs
Data In Setup Time before Clock Rising Edge	$t_{M\_DI\_SU}$	--	35	--	--	ns
Data In Hold Time after Clock Rising Edge	$t_{M\_DI\_HD}$	--	12	--	--	ns
Clock Rising / Faling Edge to Valid Output Delay	$T_{M\_CLK\_VOD}$	--	10	--	--	ns
SPI_SSn stays HIGH after Wake-up Command before sending the next SPI FLASH command	$T_{M\_SSN\_WKUP\_H}$	--	275	--	--	µs
SPI_SSn Setup Time before Clock Falling Edge	$t_{M\_SSN\_SU}$	--	75	--	--	ns
SPI_SSn Hold Time after Clock Rising Edge	$t_{M\_SSN\_HD}$	--	6	--	--	ns
SPI Slave Configuration (Config from MCU)						
Max Slave Clock Frequency	f_{CLKS_MAX}	--	--	--	16	MHz
Data In Setup Time before Clock Rising Edge	$t_{S\_DI\_SU}$	--	5	--	--	ns
Data In Hold Time after Clock Rising Edge	$t_{S\_DI\_HD}$	--	15	--	--	ns
SPI_SSn Setup Time before Clock Falling Edge	$T_{S\_SSN\_SU}$	--	60	--	--	ns
SPI_SSn Hold Time after Clock Rising Edge	$T_{S\_SSN\_HD}$	--	10	--	--	ns
SPI_SSn keep HIGH Time (between SigWord and Bitstream)	$T_{S\_SSN\_H}$	--	3	--	--	µs
Min Clock Pulse HIGH	T_{S_CLKH}	--	10	--	--	ns
Min Clock Pulse LOW	T_{S_CLKL}	--	10	--	--	ns
Clock Tree						
Global Clock Buffer Frequency	f_{GB_MAX}	T_A = +25 °C	--	--	2793	MHz
		T_A = -40 °C	--	--	2793	MHz

3.3.8 Supply Current Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ± 5 %.

Parameter	Symbol	Min	Typ	Max	Unit
V_{DDC} power supply current, device in sleep mode (PWR = 1, EN = 0, BRAM_PG = HIGH (power gated))	I_{DDC_RET}	--	14	171	µA
V_{DDC} power supply current, device in reset state (PWR = 0, EN = X, BRAM_PG = HIGH (power gated))	I_{DDC_RST}	--	14	170	µA
V_{DDC} power supply current, device in sleep mode (PWR = 1, EN = 0, BRAM_PG = LOW (data retained))	I_{DDC_RST}	--	20.52	335	µA
V_{DDC} power supply current, device in functional mode (PWR = 1, EN = 1, BRAM_PG = HIGH (power gated), FPGA core in static state)	$I_{DDC\_FUNC\_STAT}$	--	52.27	1100	µA
V_{DDIO} power supply current, device in reset state (PWR = 0, EN = X, GPIOs are retained = HIGH)	I_{DDIO_RST}	--	0.862	6.8	µA
Peak (Inrush) I_{DDIO} Current during Device RESET to On-State Transition (nRST (PWR) = LOW to HIGH)	$I_{DDIO\_PWR\_PK}$	--	--	2.48	mA
Peak (Inrush) I_{DDC} Current during Device RESET to On-State Transition (nRST (PWR) = LOW to HIGH)	$I_{DDC\_PWR\_PK}$	--	--	23.54	mA
V_{DDC} Power Supply Peak Current during startup and configuration	I_{DDC_PEAK}	--	--	8.45	mA
V_{DDIO} Power Supply Peak Current during startup and configuration	I_{DDIO_PEAK}	--	--	7	mA

3.3.9 BRAM Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
Read Max Frequency	f_{RD_MAX}	--	--	45	MHz
Read Max Frequency, T_A = +25 °C	$f_{RD\_MAX\_25}$	--	86.9	--	MHz
Write Max Frequency	f_{WR_MAX}	--	--	63.9	MHz
Write Max Frequency, T_A = +25 °C	$f_{WR\_MAX\_25}$	--	123.5	--	MHz

3.3.10 PWR (nRST) and EN (nSLEEP) Specifications

T_A = -40 °C to +85 °C, V_{DDIO} = 1.71 V to 3.465 V, V_{DDC} = 1.1 V ± 5 %, unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit
PWR (nRST) = (HIGH to LOW) transition to GPO Retention (or Hi-Z) state delay (when OSC_EN = 1 in Functional mode [1] [2]) Note: Same is for reset through IOB int_rst = HIGH.	$T_{nRST\_GPO\_RST\_RET\_DLY}$	--	292	376	ns
PWR (nRST) = (LOW to HIGH) transition to Power-on State (start of configuration) delay	T_{nRST_EX}	--	215.5	310.0	µs
PWR (nRST) = (HIGH to LOW) transition to getting in Device-off State delay Note: During this time PWR (nRST) should be held LOW.	T_{nRST_ENT}	500	--	--	µs
EN (nSLEEP) = (HIGH to LOW) transition to GPO Retention state delay(OSC_EN = 1 in Functional mode [1] [2])Note: Same for sleep through IOB sleep_start = HIGH	$T_{nSLEEP\_GPO\_RET\_DLY}$	--	40	157	ns
EN (nSLEEP) = (LOW to HIGH) transition to Functional State	T_{nSLEEP_EX}	--	149	225	µs
EN (nSLEEP) = (HIGH to LOW) transition to getting into Retention State delay Note: During this time EN (nSLEEP) should be held LOW.	T_{nSLEEP_ENT}	500	--	--	µs
Max delay for user-clocks to be stopped before transition to sleep or reset	$T_{USR\_CLK\_STOP\_MAX\_DLY}$	--	--	5	µs

[1] In the case of Functional mode OSC_EN = 0 – these parameters should be increased by $t_{OSC\_SET\_50}$.

[2] In the case of using slow external clock or Logic-as-Clock – these times would be increased by 2 periods of slowest clock up to $T_{USR\_CLK\_STOP\_MAX\_DLY}$ (after that delay all user clocks would be forced to LOW state.

Note: Refer to Section 7 Power-Up and Configuration Sequence timing diagram:

T_{nSLEEP_CYC} (EN (nSLEEP) pin cycle time) = T_{nSLEEP_ENT} + T_{nSLEEP_EX};

T_{nRST_CYC} (PWR (nRST) cycle time) = T_{nRST_ENT} + T_{nRST_EX}.

3.3.11 Typical Building Block Performance

3.3.11.1 Pin-to-Pin Performance

Function	Timing	Unit
4:1 MUX	19.0	ns
16:1 MUX	25.5	ns

Note:

1. Exact performance may vary with device and tool version. The ForgeFPGA Workshop Software tool uses internal parameters that have been characterized but are not tested on every device.2. Under typical operating conditions.

3.3.11.2 Register-to-Register Performance (LVCMOS18)

Function	Timing	Unit
16-bit Counter	79	MHz
32-bit Counter	56	MHz
256 x 8 Pseudo Dual Port RAM	48	MHz
DFF to DFF	212	MHz
DFF to LUT5 to DFF	182	MHz

Notes:

[1] Exact performance may vary with device and tool version. The ForgeFPGA Workshop Software tool uses internal parameters that have been characterized but are not tested on every device.

[2] Under typical operating conditions.

4. General Purpose Input Output Buffers

4.1 Digital IO

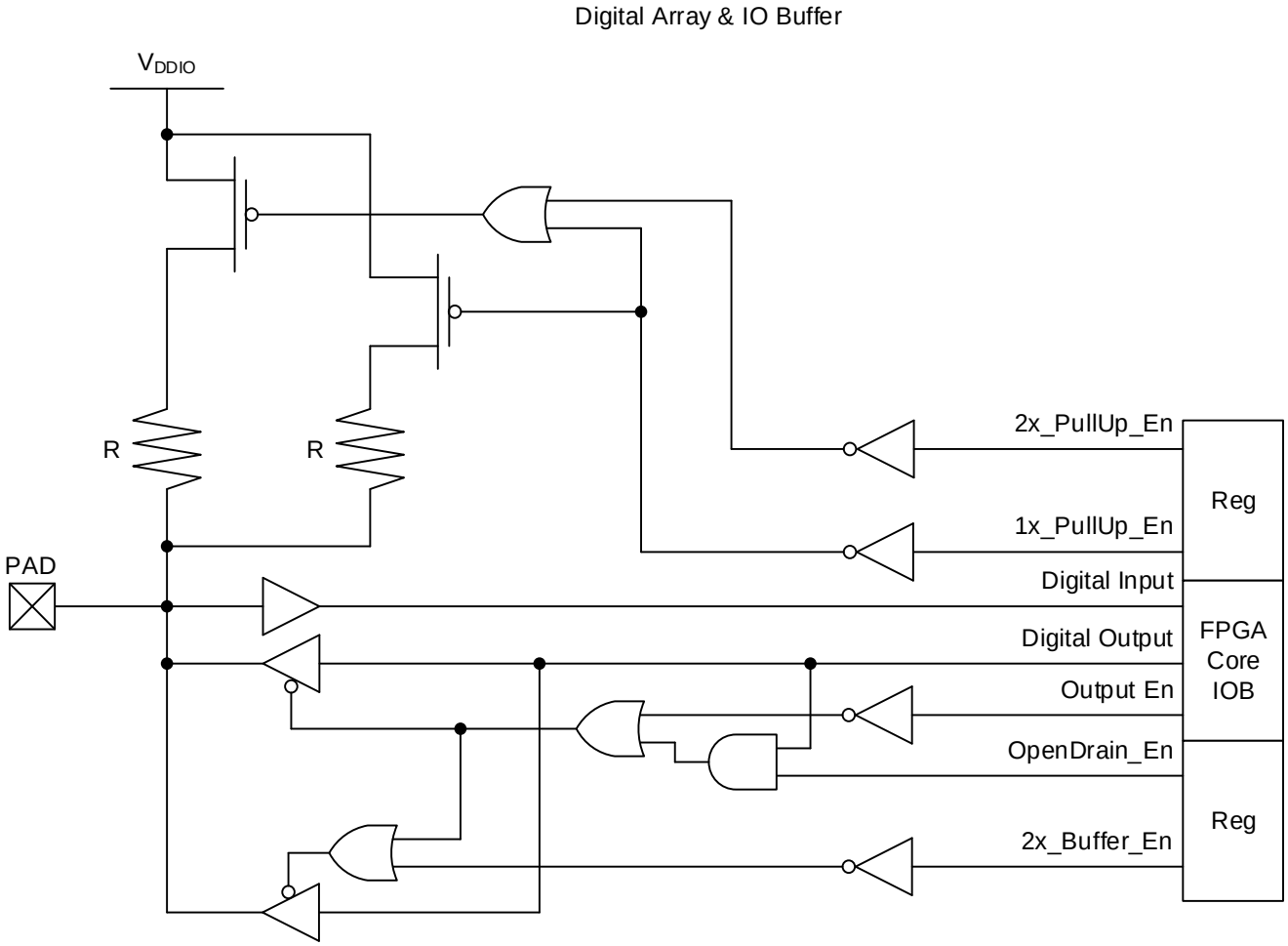


Figure 3. GPIO Buffers

The SLG47910 has 24 pins,19 of which are digital GPIO in STQFN Package. The remaining pins are V_{DDC}, V_{DDIO}, GND, and input only pins for EN (nSLEEP) and PWR (nRST). The elements labelled “Reg” in Figure 3 are configuration registers.

The following configuration options are available for each GPIO pin:

- Input
- Output, 1x Drive Push-pull
- Output, 2x Drive Push-pull
- Output, 1x Drive Open-drain
- Output, 2x Drive Open-drain.

The GPIO has four registers (2x_PullUp_En, 1x_PullUp_En, OpenDrain_En, and 2x_Buffer_En) that control the drive strength as shown in Table 7. The table below represents the bits from the NVM in the software. Using GPIO as input or output can be controlled by users dynamically through RTL code.

Table 7. GPIO Functionality

2x_Buffer_En	OpenDrain_En	Output Buffer Configuration		1x_PullUp_En	2x_PullUp_En	Pull-up Configuration
0	0	1x Push-pull		0	0	No Pull-up
0	1	1x Open-drain		0	1	No Pull-up
1	0	2x Push-pull		1	0	1x Pull-up
1	1	2x Open-drain		1	1	2x Pull-up

All Input and Output options may additionally include a resistive pull-up option. The pull-up resistor values are shown in section 3.3.2 GPIO Pull-Up Resistance . The values shown are dependent on V_{DDIO} and cover process and temperature. The R Minimum, R Typical and R Maximum cover the ±10 % variation of V_{DDIO}.

Output configuration (type and drive strength) and pull-up option are not dynamically changeable after FPGA configuration has been loaded. Output enable and digital output can be changed dynamically. Prior to release of the POR signal all GPIO are Hi-Z.

5. FPGA Core

5.1 Introduction

The FPGA Core is composed of an array of 140 Configurable Logic Blocks (CLB). At its lowest level, a 5-bit Look-up Table (LUT) is used to implement an arbitrary logic function with up to five inputs and one output. Two 5-bit LUTs are arranged in a pair, yielding a 6-bit LUT with two outputs. Each output of each of the 5-bit LUTs also has a D Flip-flop. The array of CLBs is surrounded on each side with IO Buffers (140 IOBs) to make the signal connections external to the FPGA Core resources.

Considering the total number of 140 CLB blocks in the SLG47910 with eight 5-bit LUTs (four 6-bit LUTs) with eight FFs each, the total logic count is 1120 5-bit LUTs (or in other terms 560 6-bit LUTs) and 1120 FFs.

5.2 FPGA Core Composition

From the FPGA Core's 140 total CLBs, 100 of them are Configurable Logic Blocks for Logic (CLBLs) and 40 are Configurable Logic Blocks for Memory (CLBMs). Figure 4 below shows the manner that these CLBs are tiled across the FPGA core in each tile.

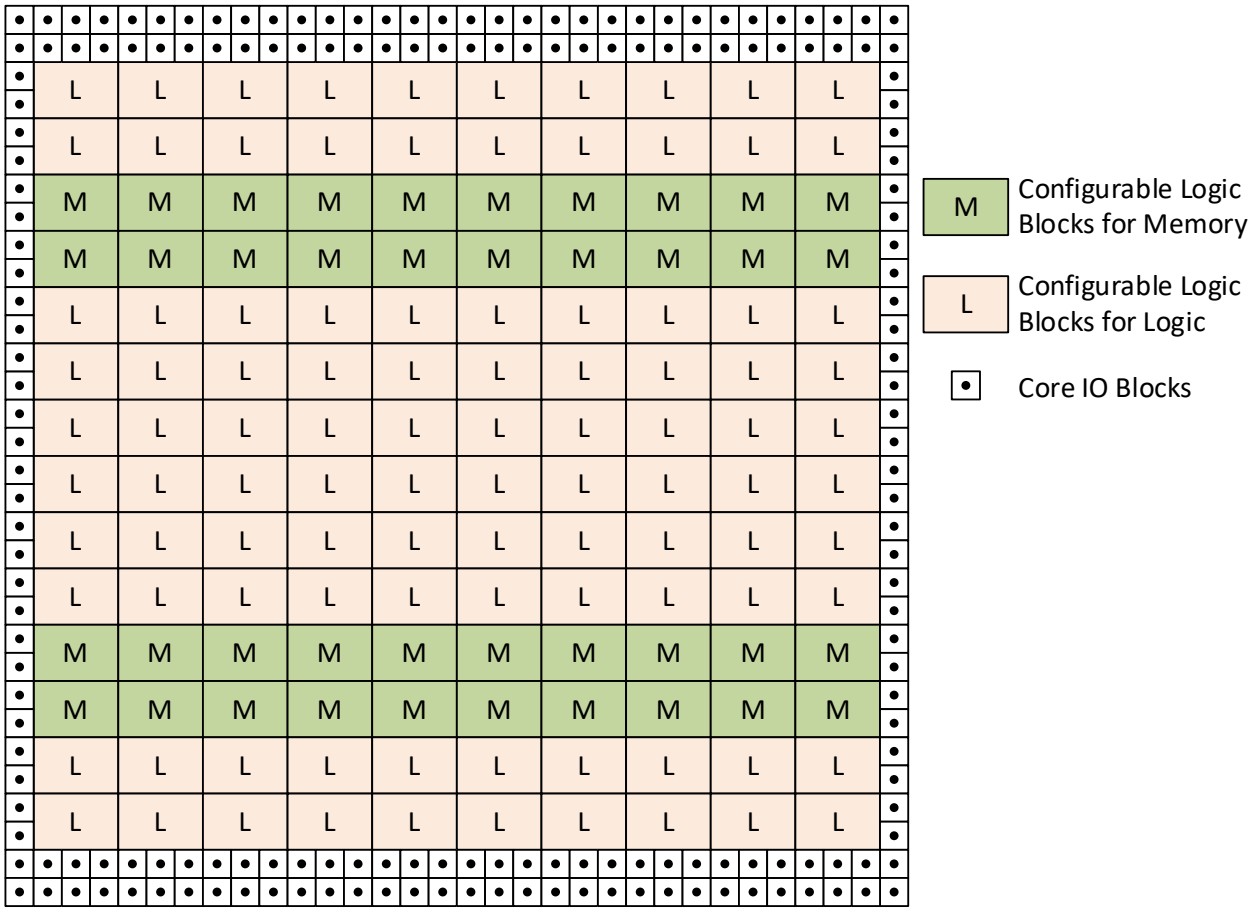


Figure 4. FPGA Core

5.3 Configurable Logic Blocks

The Configurable Logic Block (CLB) is composed of four 6-input/2-output LUTs and eight D Flip-flops. The four 6-Bit LUTs and 4-bit carry chains are grouped in this manner inside the CLBs to support efficient carry arithmetic and implementation of N-bit counters/adders. The further inclusion of the D Flip-Flops in the CLBs support high efficiency and LOW latency mapping of user defined functions. At the output of each CLB there is a cross-point switch to enable the flexible routing of signals going into the interconnect fabric. Configurable Logic Blocks for Logic (CLBL) are a subset of Configurable Logic Blocks for Memory (CLBM), with the difference between which is that the CLBM type also includes two additional operating modes, Embedded Memory Mode (EMM) and Shift Register Mode (SRM). These two modes are described in detail in section 5.3.2 Configurable Logic Blocks for Memory.

5.3.1 Configurable Logic Blocks for Logic

The diagram in Figure 5 shows the external connectivity for the Configurable Logic Blocks for Logic, including all the external control signals that are supported. Figure 6 also includes details on internal logic and signal multiplexing within the CLB.

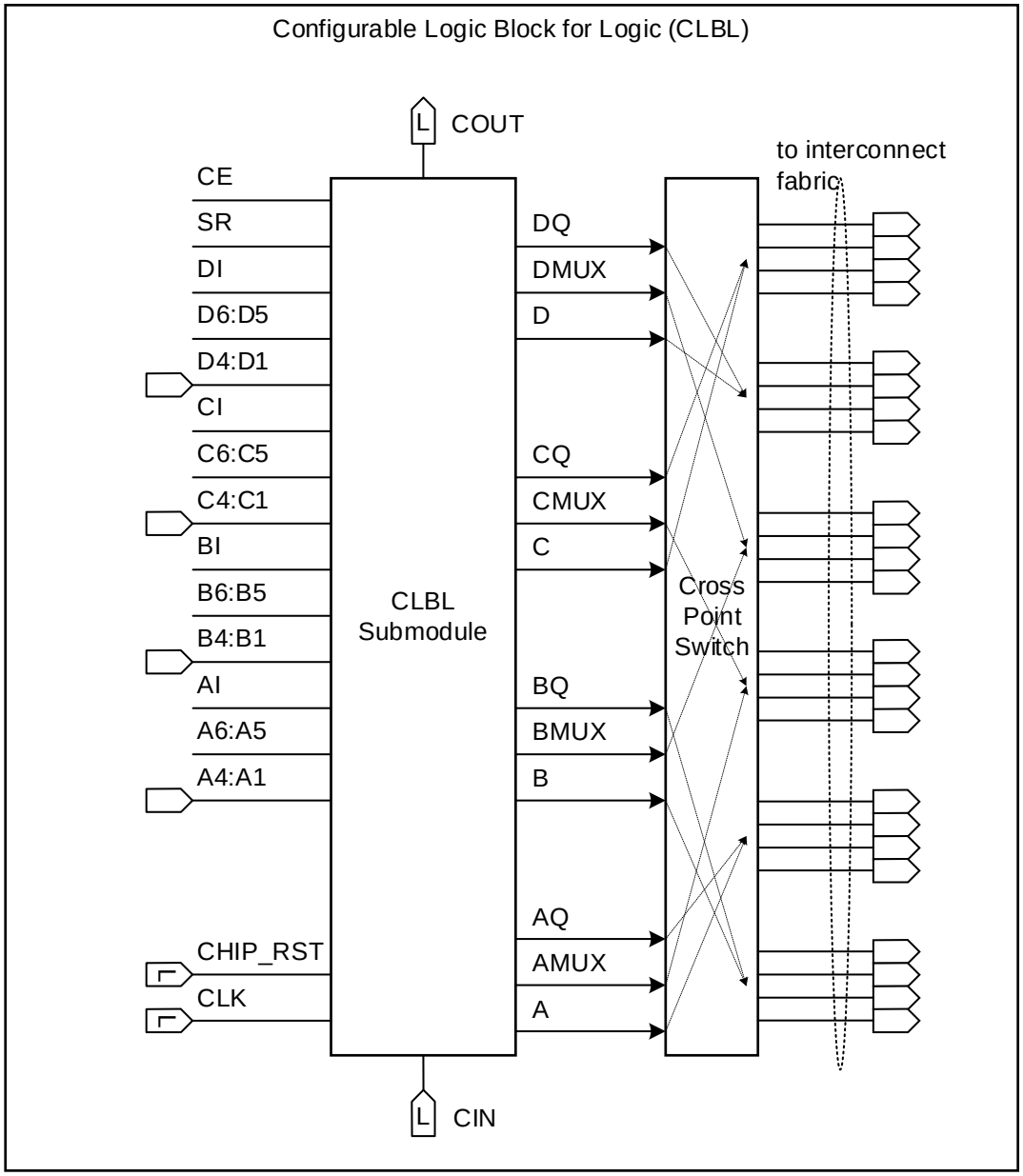


Figure 5. Configurable Logic Blocks for Logic

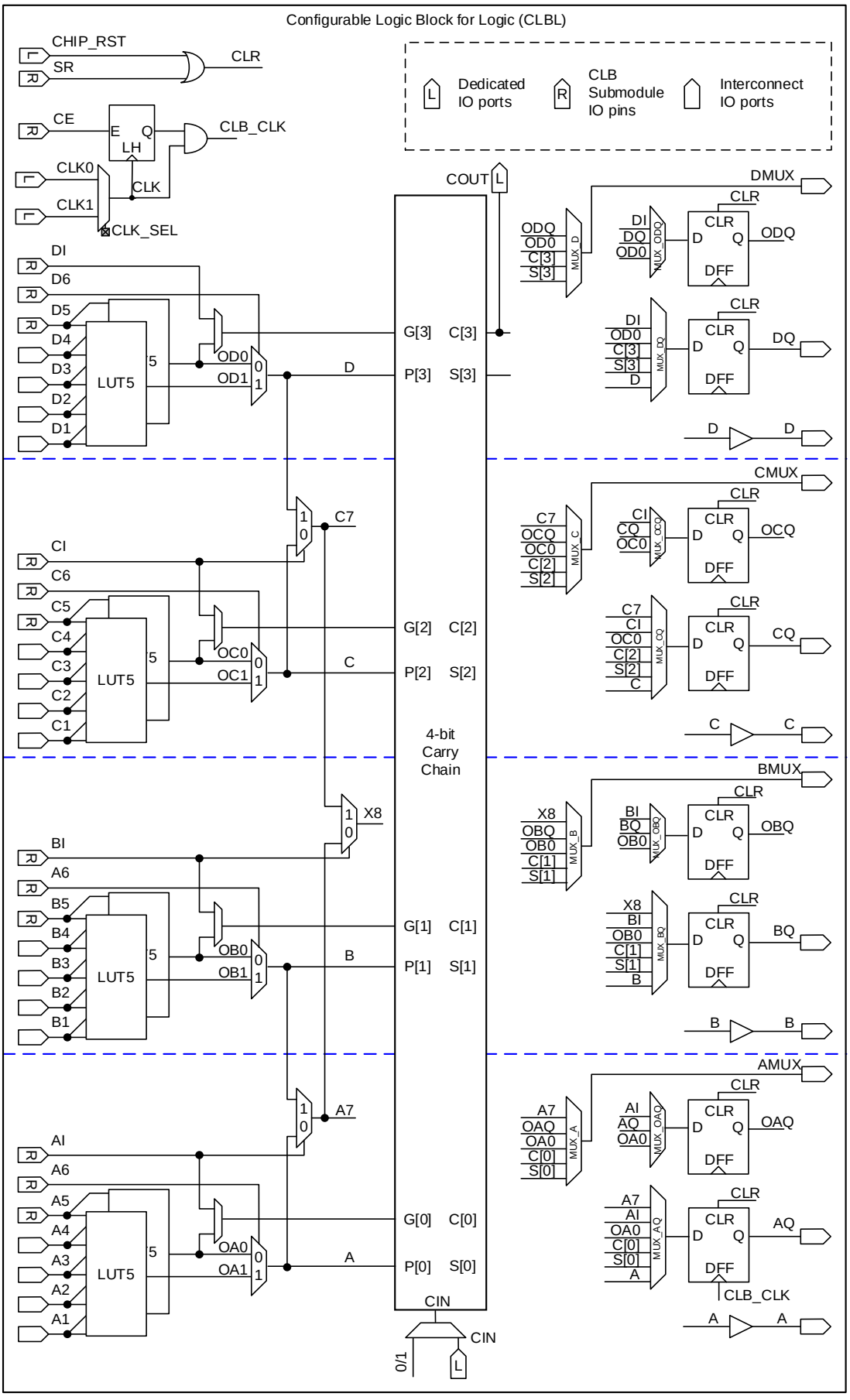


Figure 6. Configurable Logic Blocks for Logic (cont.)

5.3.2 Configurable Logic Blocks for Memory

The diagram in Figure 7 shows the external connectivity for the Configurable Logic Blocks for Memory (CLBM), including all of the external control signals that are supported. Figure 8 includes details on the internal logic and signal multiplexing within the CLBM when used in one of three different configurations of the Shift Register Mode (SRM). Figure 9 shows internal logic and signal multiplexing within the CLBM when used in one of three different configurations of the Embedded Memory Mode (EMM).

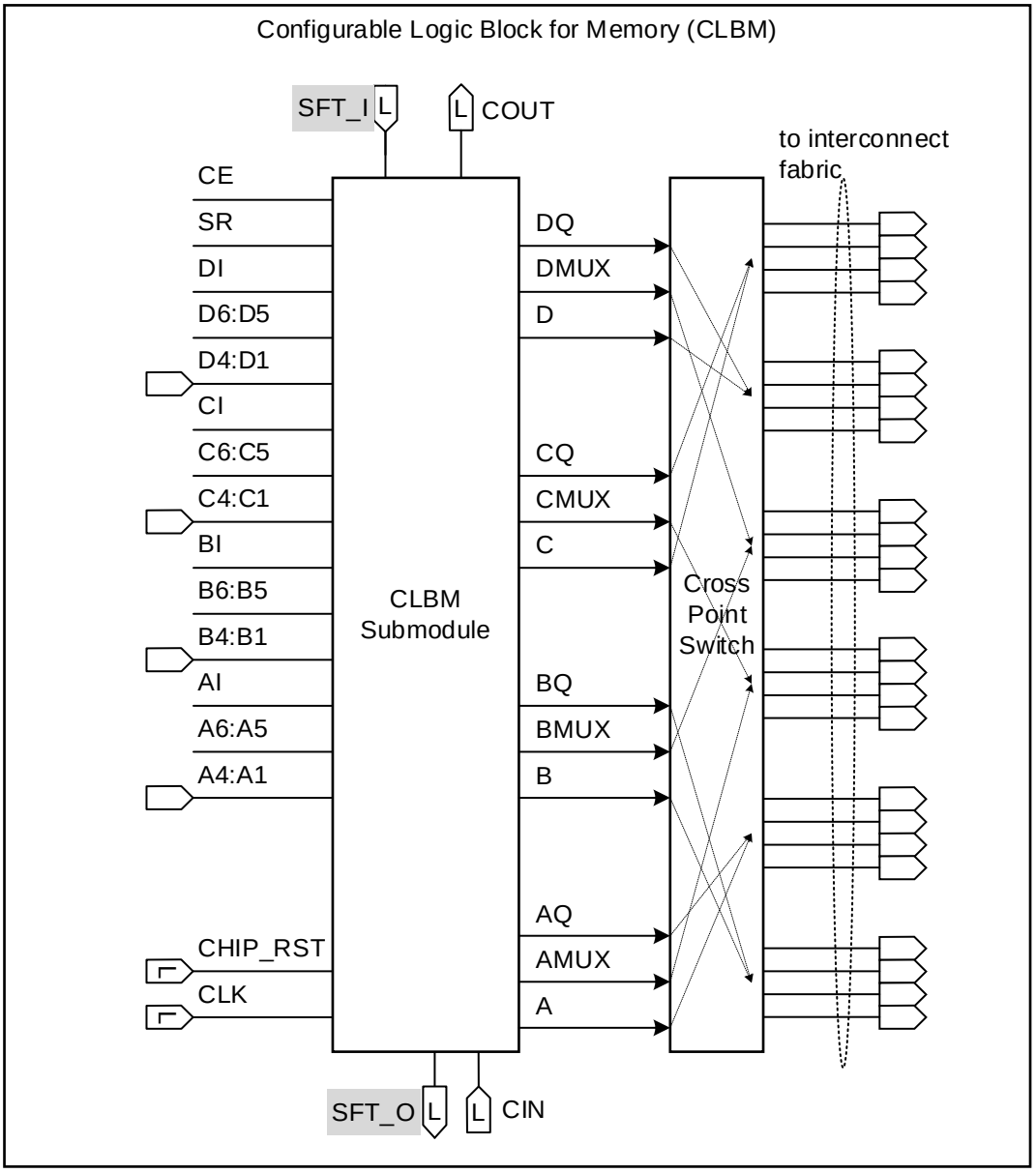


Figure 7. Configurable Logic Blocks for Memory

5.3.2.1 Configurable Logic Block for Memory Used in Shift Register Mode

When using the Configurable Logic Blocks for Memory in Shift Register Mode (SRM), there is a selectable choice in terms of the width of the shift registers that are implemented. The three choices are to have four independent 16-bit shift registers (SRL16E), two independent 32-bit shift registers (SRL32E) or one independent 64-bit shift register (SRL64E). This configuration is a part of the internal 5 kb distributed memory.

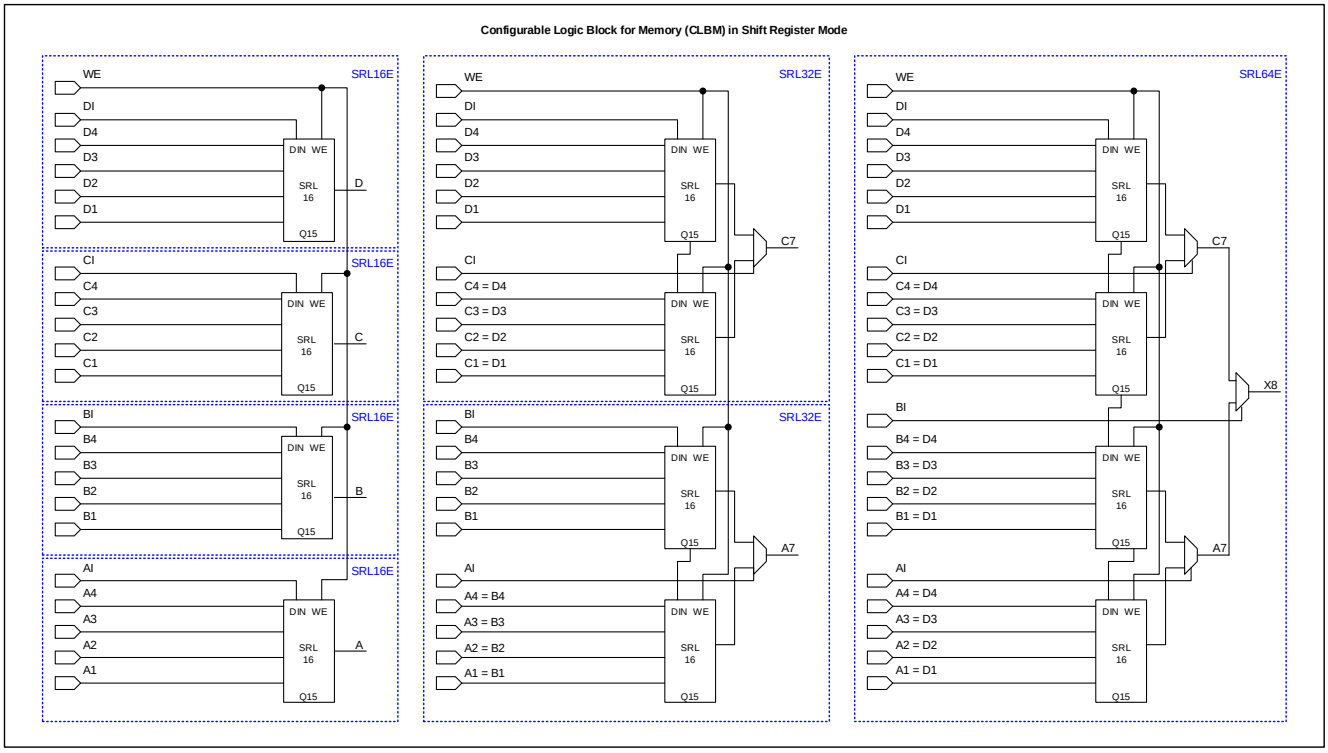


Figure 8. Configurable Logic Blocks for Memory used in Shift Register Mode

5.3.2.2 Configurable Logic Blocks for Memory used in Embedded Memory Mode

When using the Configurable Logic Blocks for Memory in Embedded Memory Mode (EMM), there is a selectable choice in terms of the width and depth of the memory elements that are implemented. The three choices are to have four independent 32 x 1-bit memory arrays, two independent 64 x 1-bit memory arrays, or one independent 128 x 1-bit memory array that can be used in single or dual-port configuration (applicable only to 32 and 64-bit memory array). This configuration is a part of the internal 5 kb distributed memory.

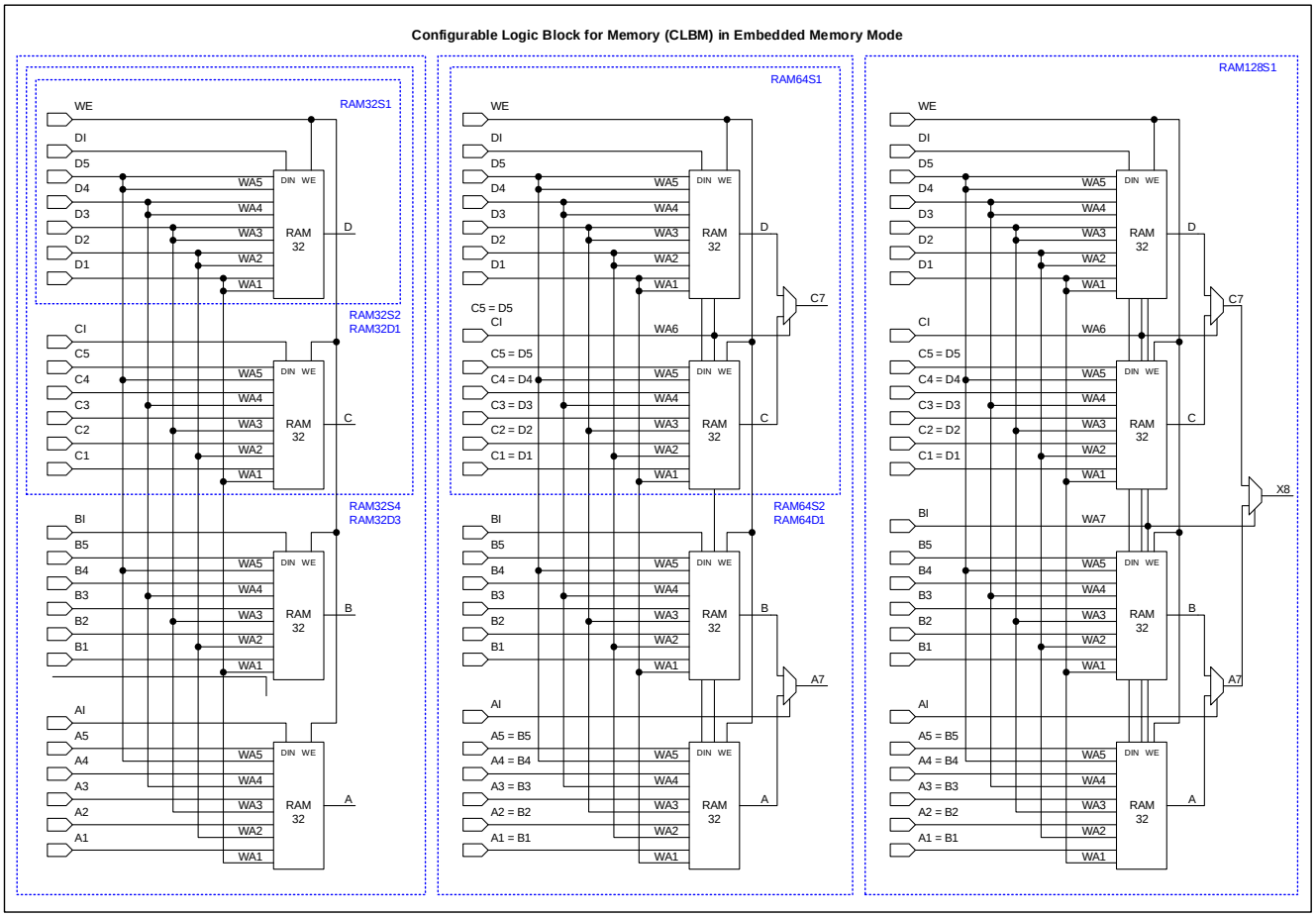


Figure 9. Configurable Logic Blocks for Memory used in Embedded Memory Mode

5.4 Core IO Buffers

The Core IO Buffers (IOB) serve as the interface between the CLBs and resources external to the FPGA Core. These buffers are arranged around the periphery of the FPGA Core. The structure of the Core IOBs is shown in Figure 10.

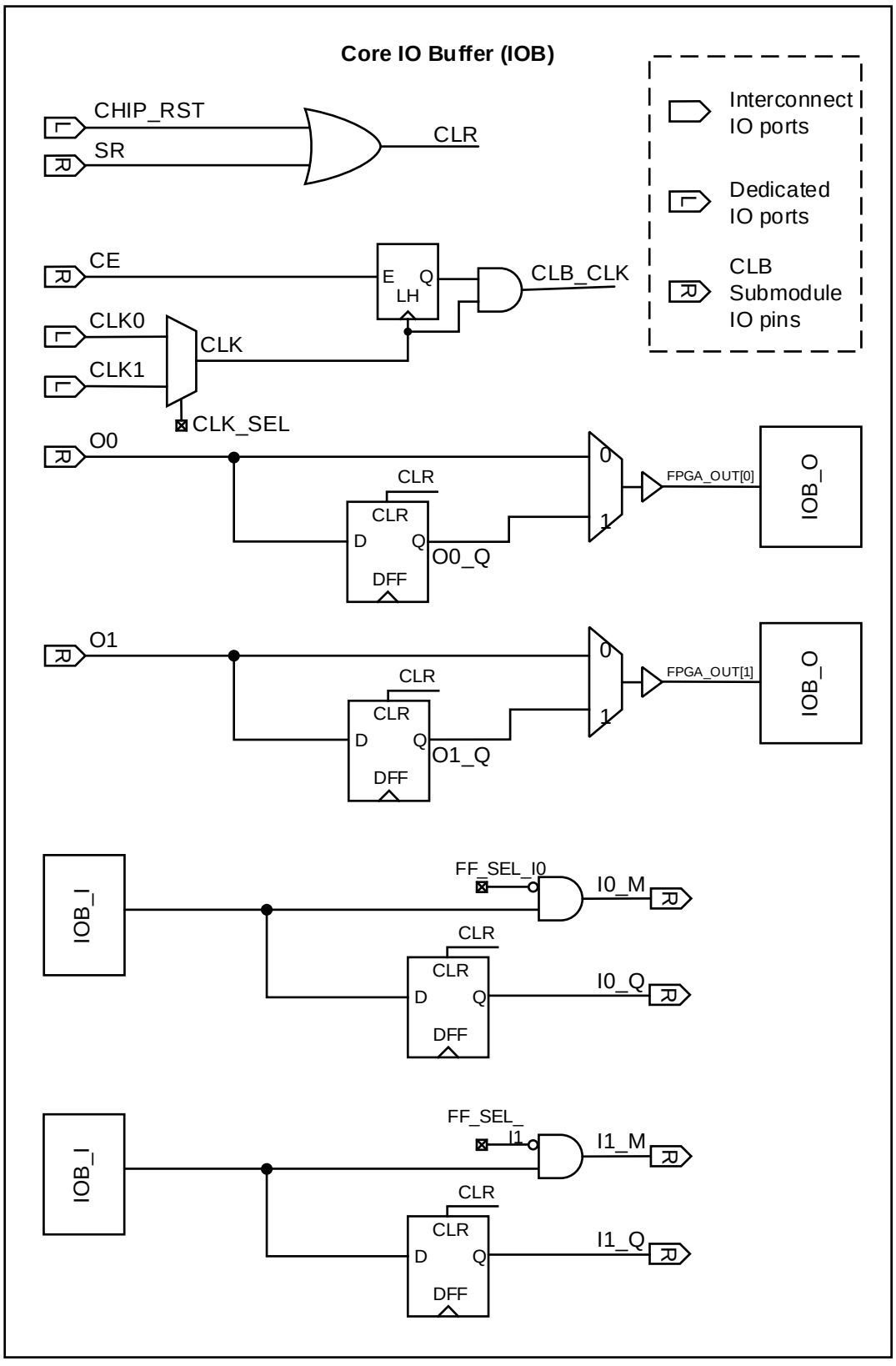


Figure 10. Core IO Buffers

5.4.1 Typical IO Behavior During Power-Up

Upon reaching the defined levels of V_{DDC} and V_{DDIO} in section 3.3 Electrical Specifications, the internal power-on reset (POR) signal is deactivated, and the FPGA core logic is enabled. To ensure the proper functionality of the critical IO banks in your application, it is essential to have all V_{DDIO} banks active with valid input logic levels. By default, the IO pins are tri-stated. This state persists until V_{DDC} and V_{DDIO} reach the defined levels. After the POR signal is deactivated and a successful configuration is loaded, the IO pins adopt the user-configured state.

5.4.2 Supported Standards

The SLG47910 ForgeFPGA GPIO buffer supports single-ended input/output standards. The buffer has individually configurable options for bus maintenance (weak Pull-up or none). Table 8 shows the IO standards (together with their supply and reference voltages) supported by the SLG47910 ForgeFPGA device.

Table 8. Supported Input/Output Standards

Single-ended Interfaces	
Input/Output Standards	**V_{DDIO} (typ)**
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V

5.4.3 Programmable Pull-Up Resistors

The SLG47910 ForgeFPGA GPIO buffers can be configured with programmable Pull-up resistors on every GPIO independently. The values of the resistors are dependent on V_{DDIO} (see section 3.3.2 GPIO Pull-Up Resistance).

6. Clocking

6.1 Clock Network

The FPGA Core has two main clock domains namely, Clock_0 and Clock_1. Each of these active clocks are internally connected to the sub clocks within the core.

The core is divided into four directions, on the North side of the core we have the REF_BRAM [3:0] WRITE_CLK & REF_BRAM [3:0] _READ_CLK as outputs. Similarly, on the South side of the core we have REF_BRAM [7:4] _WRITE_CLK & REF_BRAM [7:4] _READ_CLK as outputs. On the East side of the core, we have the two LOGIC_AS_CLK0/1. This clock is an output from the FPGA Core itself. And on the West side of the FPGA core, we have the three input clocks PLL_CLK, OSC_CLK, and GPIO through which the clock can also be supplied to the core. Using rising/falling edge of the same clock the core can utilize two clock domains CLK0 and CLK1.

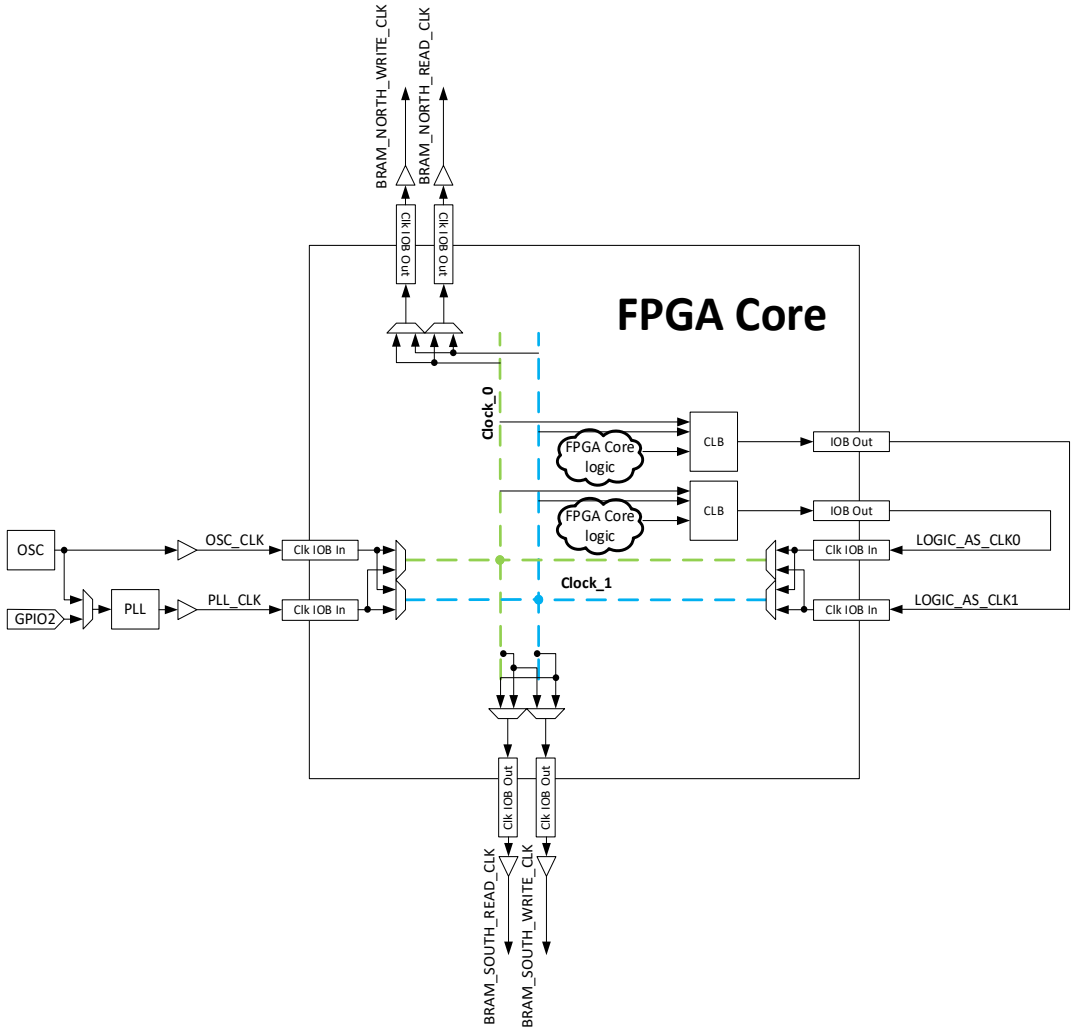


Figure 11. Clock Network Signals and Positions

Table 9. Clock Network Signals & Positions in GoConfigure Software

Clock Signal	Position
LOGIC_AS_CLK0	Clk_side = E, Input0
LOGIC_AS_CLK1	Clk_side = E, Input1
REF_LOGIC_AS_CLK0	Coord [31,11], Output0
REF_LOGIC_AS_CLK1	Coord [31,11], Output1
OSC_CLK	Clk_side = W, Input0
PLL_CLK	Clk_side = W, Input1
REF_BRAM [3:0]_WRITE_CLOCK	Clk_side = N, Output0
REF_BRAM [3:0]_READ_CLOCK	Clk_side = N, Output1
REF_BRAM [7:4]_WRITE_CLOCK	Clk_side = S, Output0
REF_BRAM [7:4]_READ_CLOCK	Clk_side = S, Output1

6.2 On-Chip Oscillator

6.2.1 Overview

The SLG47910 has an on-board 50 MHz oscillator for use within the FPGA Core. When the OSC_EN signal is set to HIGH, there is a delay in receiving the signal at OSC_CLK. This delay allows the signal to stabilize avoid any glitches on the output. OSC_CLK and OSC_READY are connected directly to dedicated FPGA Core IOB.

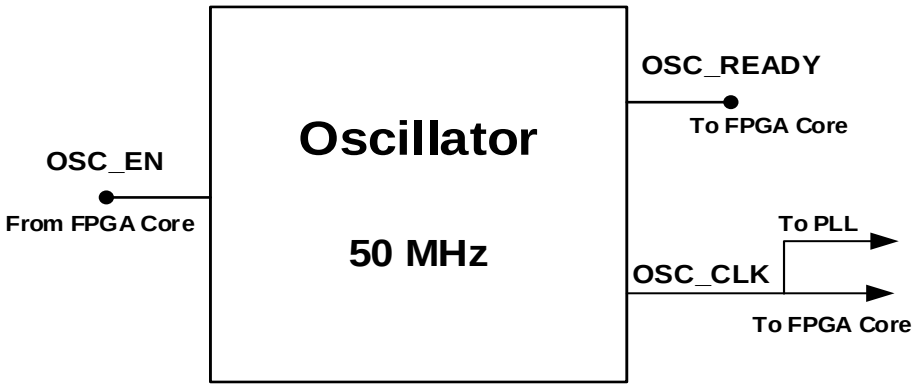


Figure 12. On-Chip Oscillator

6.2.2 Signal Descriptions

Control inputs and outputs are derived from the FPGA Core.

- **OSC _EN** (Input) – enable signal for the oscillator. Active HIGH on this signal activates the OSC.
- **OSC_CLK** (Output) – buffered oscillator clock. Oscillator clock can be sent to global interconnect network of FPGA Core or clock input source of PLL.
- **OSC_READY** (Output) – the device outputs a “1” on this signal to represent that the oscillator frequency is stable. This signal is connected to the FPGA Core

6.3 Phase-Locked Loop

6.3.1 Overview

The SLG47910 includes a LOW power, wide input and output Phase-Locked Loop (PLL) for use in applications requiring various frequencies. To maintain a LOW power state the PLL has a power-down. The input reference clock for the PLL comes from the on-chip oscillator through REF_CLK_OSC or from the external clock, routed through GPIO2 pin as REF_CLK_EXT.

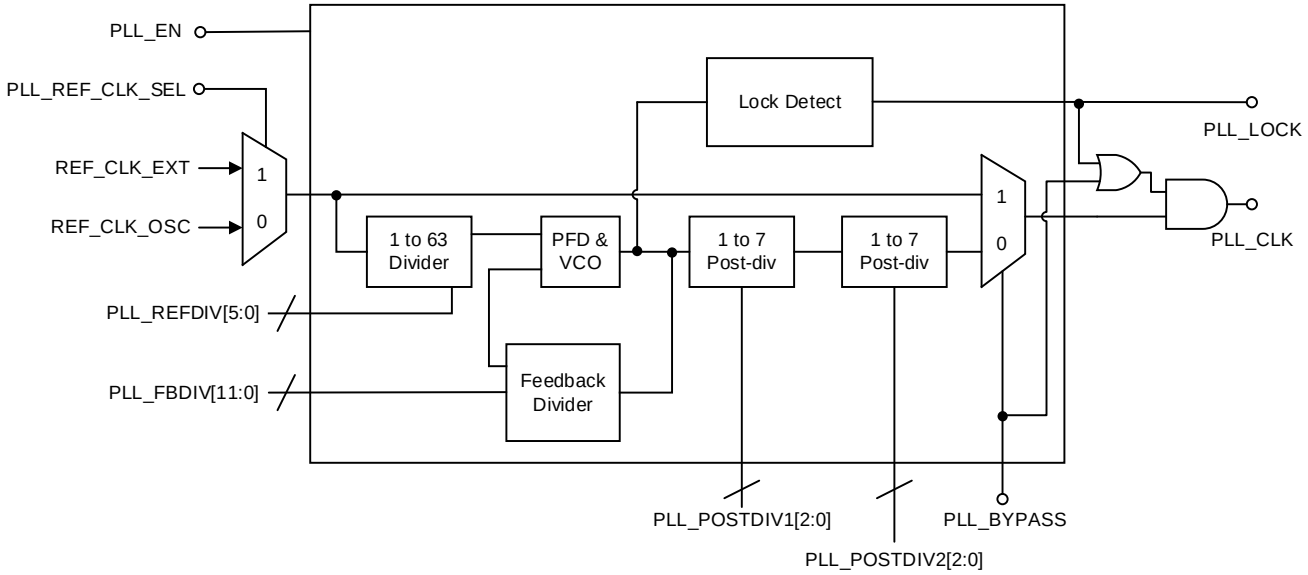


Figure 13. Phase-Locked Loop Block Diagram

The behavior of the SLG47910's PLL is to receive a reference frequency and either divide or multiply the frequency value per the following equation, where f_{input_clock} is the reference frequency of the external clock source or on-chip OSC, chosen through PLL_REF_CLK_SEL:

$$PLL\_CLK = \frac{f_{input\_clock} \times PLL\_FBDIV}{PLL\_REFDIV \times PLL\_POSTDIV1 \times PLL\_POSTDIV2}$$

Note: Using larger values for the variables in the numerator and denominator will reduce clock jitter at the expense of increased current consumption.

VCO frequency is calculated as:

$$VCO\_FREQ = \frac{f_{input\_clock} \times PLL\_FBDIV}{PLL\_REFDIV}$$

PFD frequency is calculated as:

$$PFD\_FREQ = \frac{f_{input\_clock}}{PLL\_REFDIV}$$

For the PLL to behave correctly, several conditions on the input and output clock signals must be met:

- The reference clock input must be a stable, single frequency within the frequency range specified in section 3.3.3 PLL Specifications. Jitter and duty cycle should also be confirmed to be within the acceptable range specified in section 3.3.3 PLL Specifications.
- PLL_CLK must be within the frequency range specified within section 3.3.3 PLL Specifications. The PLL_LOCK output must be employed to ensure a stable output frequency.
- VCO and PFD Frequency must be within the frequency range specified with in section 3.3.3 PLL Specifications

Valid PLL_FBDIV, PLL_REFDIV, and PLL_POSTDIV values (see section 6.3.2 Signal Descriptions)

6.3.2 Signal Descriptions

Clock and control inputs determine the input clock source and intended output frequency.

- **PLL_REF_CLK_SEL** (Input) – selects the PLL Input Clock source between the on-chip OSC and an external clock, originating from GPIO2. When LOW the clock input to the PLL is the OSC.
- **PLL_BYPASS** (Input) – PLL_BYPASS is an active HIGH signal that asserts a direct path between the clock input and PLL_CLK.
- **PLL_REFDIV [5:0]** (Input) – sets the reference divide value from 1 to 63.
- **PLL_FBDIV [11:0]** (Input) – sets the PLL Feedback Divide value from 16 to 400.
- **PLL_POSTDIV1[2:0] & PLL_POSTDIV2[2:0]** (Input) – the two stages of post-dividers are used to divide down the VCO Frequency before the PLL_FOUT clock output. Each post-divider has options for division from 1 to 7. Total post divide is PLL_POSTDIV1 * PLL_POSTDIV2.

Note: If a PLL has multiple post dividers in series, the value of the first post divide should be maximized before enabling the second post divide.

For example, Divide by 4:

- Recommended: Set PLL_POSTDIV1 = 4, PLL_POSTDIV2 = 1
- Not recommended but accepted: Set PLL_POSTDIV1 = 2, PLL_POSTDIV2 = 2
- Not accepted: PLL_POSTDIV1 = 1, PLL_POSTDIV2 = 4.

User can use the PLL Calculator feature in the GoConfigure Software to change the above parameters to meet the desired output frequency value.

Power inputs determine the existing power state of the PLL. Enable inputs are used to enable the different clock outputs that can be used in the FPGA fabric and can lower power consumption when properly utilized.

- **PLL_EN** (Input) – Power-on for PLL. Active HIGH.
- **PLL_CLK** (Output) – PLL output clock (depending on Lock state of the PLL).
- **PLL_LOCK** (Output) – Lock state of the PLL. Indicates no cycle slips between the feedback clock and the Phase Frequency Detector for 256 consecutive cycles. Lock goes to HIGH after stable frequency on the PLL output.

All PLL signals are connected to dedicated FPGA Core IOBs.

6.4 Logic-As-Clock

In the SLG47910 FPGA Core, the user logic can be utilized as clock signal through logic-as-clock path.

For this purpose, the user signal which is to be used as the clock should first be output through Logic-IOB (REF_LOGIC_AS_CLK0/1) and then looped back into the FPGA core as the clock through clock-IOB (LOGIC_AS_CLK0/1) (see Figure 14). This is known as Logic-as-Clock circuitry (LaC Circuitry). There are two LaC paths available (see Figure 14).

To activate Logic-as-clock paths there are dedicated IOBs, LOGIC_AS_CLK0_EN and LOGIC_AS_CLK1_EN.

With Logic-as-Clock circuitry there are two ways to transform the data signal into a clock signal:

- The clock signal is generated inside the FPGA Core (for example OSC/8) and then fed through LaC1 path.
- The clock signal is fed through any GPIO to the FPGA Core, transfers it without processing (in an asynchronous manner) and is fed through LaC0 path.

Note: There are only two clock trees in the FPGA Core, so only one LaC path can be used if OSC or PLL is used as well.

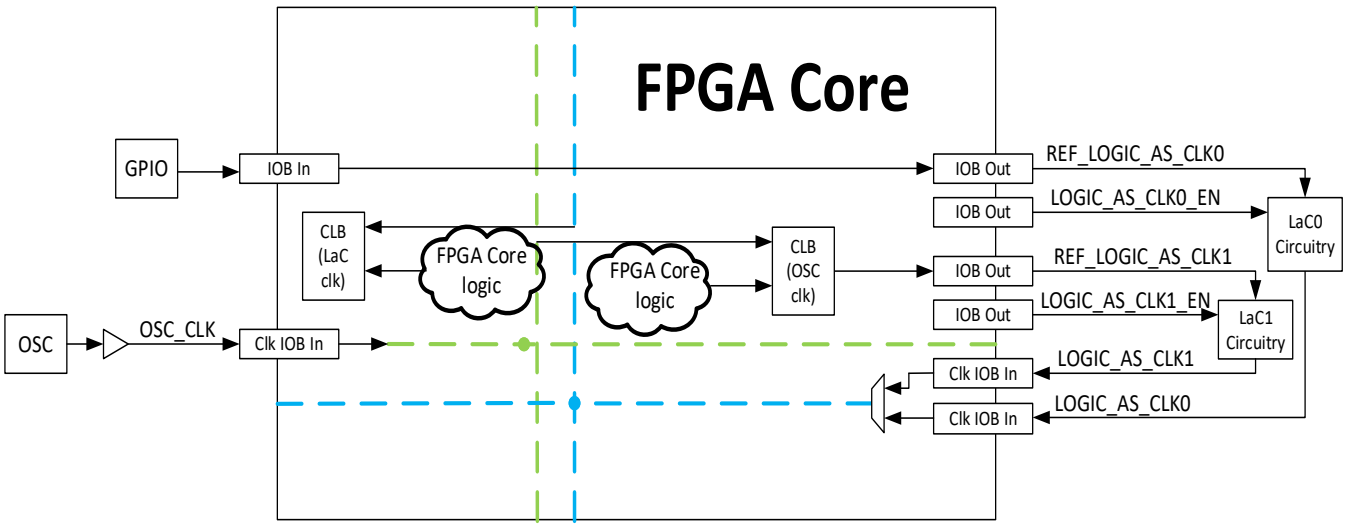


Figure 14. Logic-As-Clock Network

Note: More information about this in [4] Application Notes, ForgeFPGA Application Notes & Design Files.

7. Power-Up and Configuration Sequence

This section describes sequence during power-up, configuration and PWR (nRST) or EN (nSLEEP) assertion.

The general sequence is shown in Figure 15.

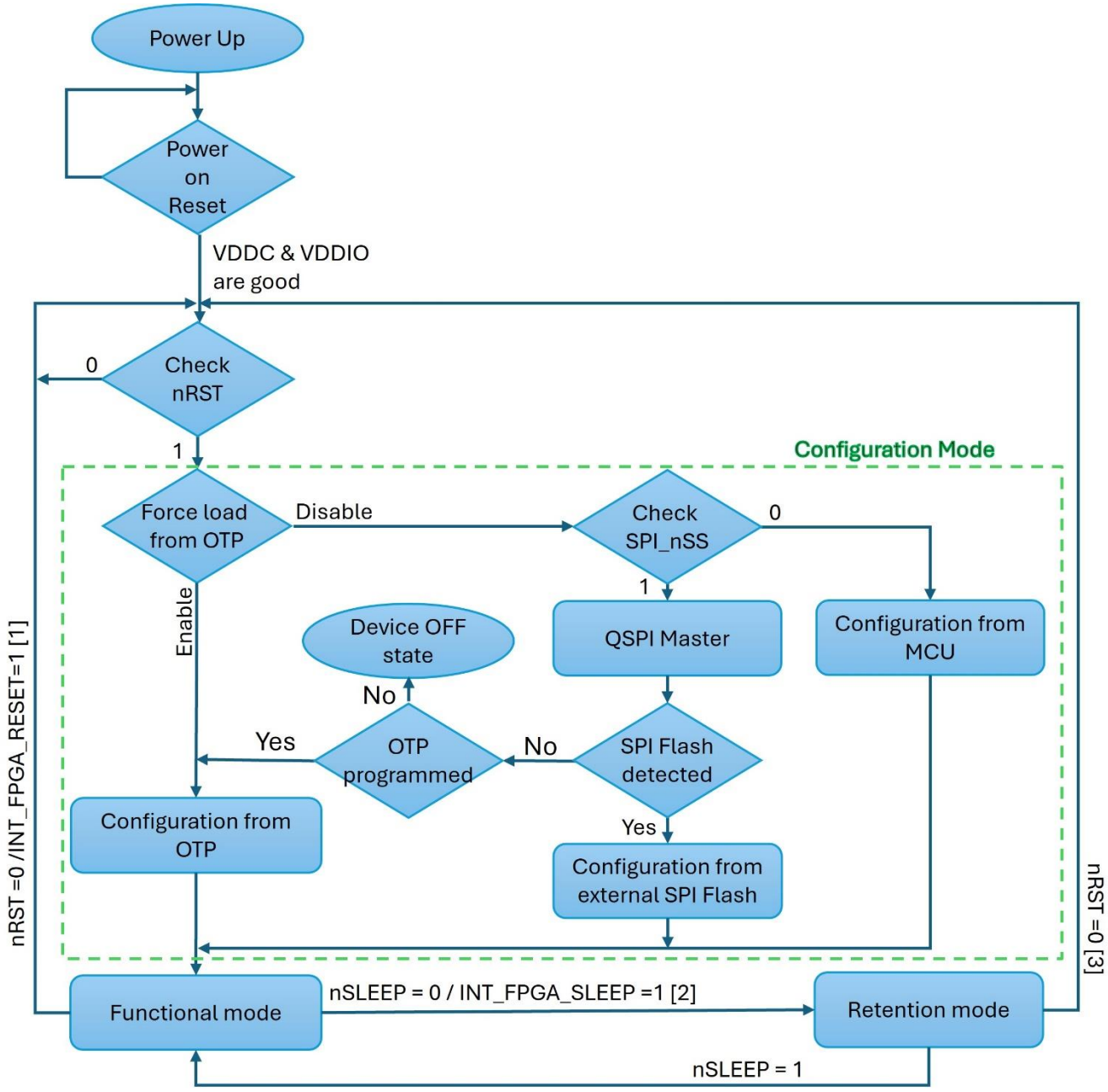


Figure 15. Power-Up Sequence

Notes:

1. The “Chip Reset source” register gives the ability to choose the signal that will be used to reset the device.
2. The “Sleep Mode source” register gives the ability to choose the signal that will be used for transitioning the device into retention mode.
3. The nRST = 0 can only operate when the "Chip Reset source" register is set to 0 and device will configure only from internal OTP.

To start the configuration sequence in the SLG47910, the V_{DDC} and V_{DDIO} voltages should be higher than Power-On threshold. Parameters of the Power-on-Reset (POR) are given in section 3.3.5 Power-On-Reset Specifications. The device will start checking nRST state and if nRST = 1 it transits to **Configuration Mode** else stays in a low power state.

In the next state, the device checks “Force load form OTP” register. Depends on state of this register configuration happens only from internal OTP or MCU/External SPI Flash/internal OTP.

If “Force load form OTP” register is disabled, device will check the SPI_nSS state (GPIO4). If nSS is LOW, the chip will wait for configuration from the MCU. However, if nSS is HIGH (due to an external pull-up resistor on SPI_nSS), the SLG47910 will act as an SPI Master and attempt to configure itself from the external SPI flash. The device will make 6 attempts to configure from the external SPI flash before reverting to OTP configuration (if OTP was programmed). **Configuration Mode** can be interrupted at any time by setting nRST = 0 which would result in moving to the lowest power mode. The **FPGA_CORE_READY** signal indicates when FPGA Core has been configured. It goes HIGH before entering **Functional mode**. The **FPGA_CORE_READY** signal can be used as reset or enable signal for user logic. When **Configuration Mode** is completed successfully the device transits to **Functional Mode**.

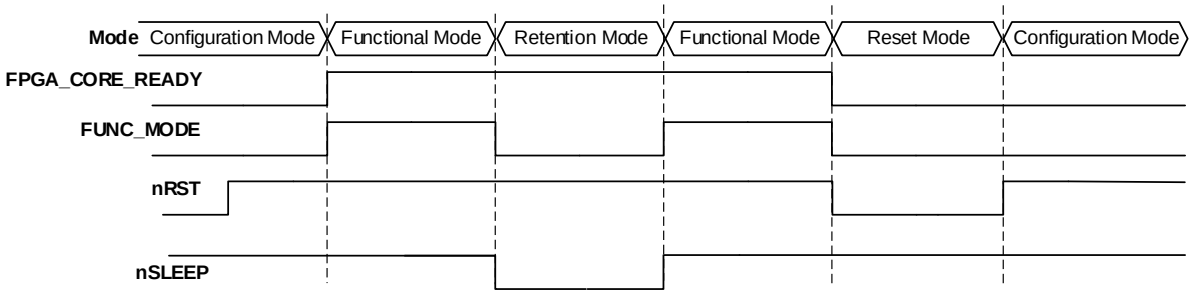


Figure 16. FPGA_CORE_READY and FUNC_MODE Signals Behaviour

The device includes an additional signal known as FUNC_MODE, which indicates that the device is in Functional mode. The distinction between FPGA_CORE_READY and FUNC_MODE is that FPGA_CORE_READY goes HIGH before the device enters **Functional mode** and stays HIGH throughout the entire operation of the device. It can only be reset by entering **Reset Mode**. On the other hand, **FUNC_MODE** goes HIGH after the configuration phase and will go LOW each time the device enters retention mode. Similar to FPGA_CORE_READY, it can be reset by entering **Reset Mode**. The FUNC_MODE signal can be utilized by user logic if the user wishes to reset the sequential logic each time the device exits retention mode.

Notes:

1. There is an external Resistor Divider applied to the GPIO. After POR is shut down, the GPIO is configured to pulled-low.
2. All the macrocells such as GPIOs, BRAMs, PLL, OSC turn on after TPOR_VRAM.

Functional Mode might be interrupted by two methods: **Reset Mode** or **Retention mode.**

The device can transit to **Retention Mode** by EN (nSLEEP) = 0 (“nSLEEP signal source” register = 0) or INT_FPGA_SLEEP = 1 (“nSLEEP signal source” register = 1). Second case allows user to use EN (nSLEEP) pin as a general purpose input. In **Retention Mode** the memory from the FPGA Core/BRAM is retained (saved) and it functions in LOW-powered mode. User logic is stopped, clocks are not provided to FPGA Core. GPIOs retain state that they had before transition to **Retention Mode**. Also, the OSC and PLL are powered down.

When rising edge is detected on EN (nSLEEP) pin (no matter a value of “nSLEEP signal source” register) – device transits back to **Functional Mode**: no reconfiguration needed, internal states of FPGA Core and BRAMs are restored. User’s logic would continue operation. Minimal EN (nSLEEP) low-pulse duration should be 45 µs (if OSC was ON in Functional mode) or 300 µs (if OSC was OFF in Functional mode).

If PWR (nRST) = 0 (“nRST signal source” register = 0) or INT_FPGA_RESET = 1 (“nRST signal source” register = 1), the device transits to initial state after POR – Idle Mode. During this transition the FPGA Core’s memory is not retained as it is in its lowest powered state. When reg_bram_keep = 0 – the BRAM memory is also not retained; if reg_bram_keep = 1 then the contents of the BRAMs are retained (see A Register Definitions). If reg_gpio_keep = 1 – GPIOs would retain their states, otherwise it is in Hi-Z state. OSC and PLL is in powered down mode.

When HIGH level is detected on PWR (nRST) pin the device proceeds to **Configuration Mode**. In this case FPGA Core is re-configured and previous internal states are not restored. Whenever the transition from **Functional mode** to **Retention Mode** or **Reset Mode** is triggered, it is required to wait until all user clocks are stopped. This would require 2 falling edges of the respective clock or a 5 µs delay (in case if clock is very slow and time to get 2 falling edges is more than this delay) after which all user clocks would be forced into a LOW state.

Table 10. State of Modules in Different Chip Modes

Mode	Module					
	FPGA Core	**BRAM**	**OSC**	**PLL**	**GPIO**	**User logic**
Configuration	Re-configured	Re-configured	Re-configured	Re-configured	Hi-Z	Re-configured
Functional	Operation	Operation [1]	Operation [1]	Operation [1]	Operation	Operation
Retention	Retained	Retained	Power Down	Power Down	Retained	Retained
Reset	Not retained/ Lowest power state	Retained/ Not retained [3]	Power Down	Power Down	Retained/Hi-Z [4]	Not retained

Notes:

1. It depends on the design.
2. If EN goes high from Retention mode, ForgeFPGA will return to Functional mode without needing reconfiguration.
3. Depends on the value of reg_bram_keep.
4. Depends on the value of reg_gpio_keep.

Figure 17 depicts the general behaviour during PWR (nRST) and EN (nSLEEP) assertion.

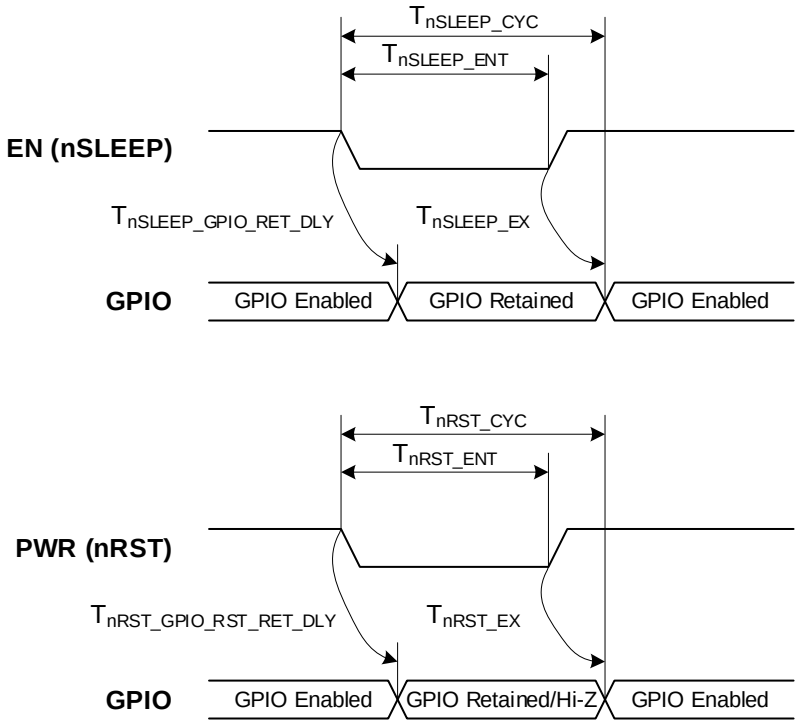


Figure 17. Device On/Off State Cycle Timing Diagram (PWR/EN Pin)

Notes:

5. When PWR = 0 and EN = X – GPIO is Hi-Z (unless REG_GPIO_KEEP = 1) state and memory is not retained (unless REG_BRAM_KEEP = 1).
6. When PWR = 1 and EN = 0 – device is in Retention Mode, GPIO and the data are retained.
7. When PWR = 1 and EN = 1 – device is in Functional Mode, GPIOs and BRAMs under user's logic control.
8. Refer to section 3.3.10 PWR (nRST) and EN (nSLEEP) Specifications for the PWR and EN Power Down and Retention Characteristics.

PWR and EN modes are supported only in the functional and configuration states and are **not** supported in the Read/Programming state.

8. Configuration Modes

An internal configuration wrapper is used to configure the ForgeFPGA core. The GoConfigure software is used to generate the bitstream. The configuration can be done using three different configuration bitstream sources:

1. External SPI Flash (SPI Master Mode)

In this mode the SLG47910 is the SPI Master, and the external SPI Flash is the SPI Slave. During SPI mode, GPIO3 is used to output the SPI_SCLK. GPIO4, GPIO5, and GPIO6 are used as SPI_SS, SPI_SI and SPI_SO respectively. To enter SPI Master mode, the SPI_SS line should be HIGH when the chip configuration process starts.

2. MCU as a host

In this mode the SLG47910 is the SPI Slave and a connected MCU is the SPI Master. During SPI mode, GPIO3 is used to input the SPI_SCLK. GPIO4, GPIO5, and GPIO6 are used as SPI_SS, SPI_SI and SPI_SO respectively. To enter MCU Slave mode, the SPI_SS line should be LOW when the chip configuration process starts.

3. Internal OTP (One Time Programmable)

In this mode, the configuration for the FPGA is stored in the One Time Programmable (OTP) Non-Volatile Memory (NVM). The FPGA core is configured by reading the bitstream from OTP memory. To enter OTP mode, the otp_en register should be HIGH when the chip configuration process starts.

See Table 3. For more information, refer to the [3] ForgeFPGA Configuration Document.

9. Block RAM

9.1 BRAM Structure

The SLG47910 contains 32 kb of embedded block RAM (BRAM) that is connected directly to the FPGA core's IOBs. The diagram below highlights the interfacing with the BRAM. The BRAM connections will take the majority of IOB connections within the device, including the entire top and bottom row of the FPGA Core.

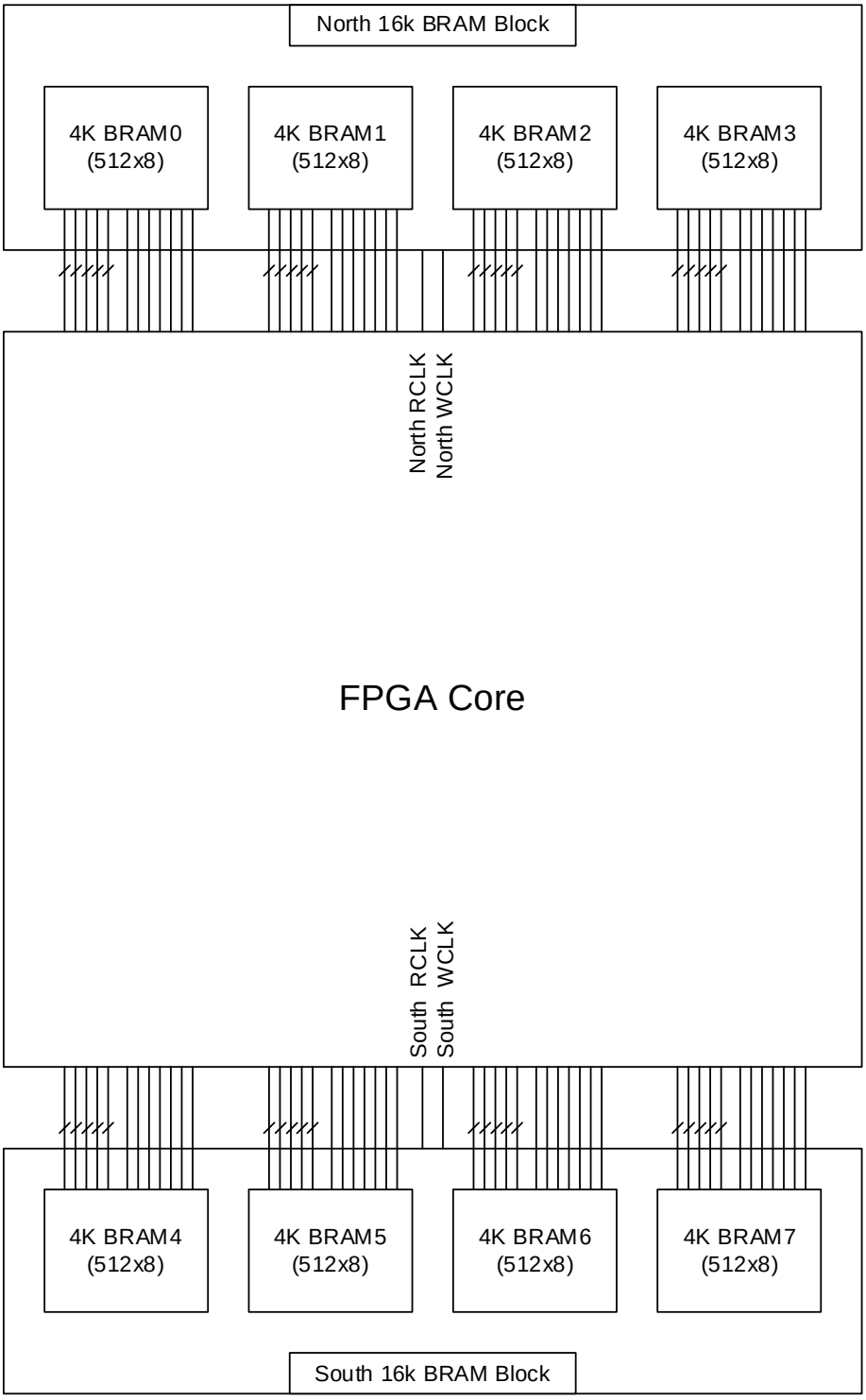


Figure 18. Embedded Block RAM

9.2 BRAM Slices

9.2.1 BRAM Slice Structure

The SLG47910's 32 kb of BRAM is divided into two individual 16 kb blocks, each of which are further broken down into 4 kb (512 x 8) slices. Each 4 kb slice is provided with its own set of IOB connections to the core, allowing for individual access to any slice. Each slice may also be configured to contain either an 8, 4, 2, or 1-bit data width. The diagram for a single 4 kb memory slice is shown below in Figure 19 and the functionality of these BRAM signals are specified in Table 11.

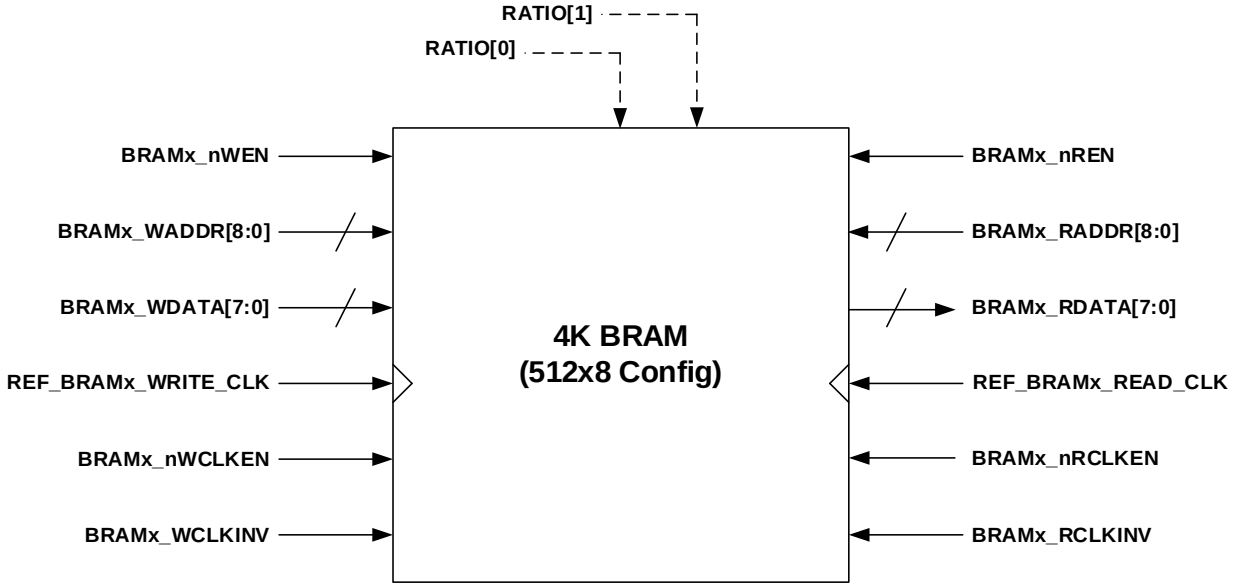


Figure 19. BRAM Slice Structure

Table 11. BRAM Configuration

Name	Direction	Description
BRAMx_nWEN	Input	Write Enable (active LOW)
BRAMx_WADDR[8:0]	Input	Write Address Bits; for anything deeper than 512, the unused DINs can be repurposed as WADDR
BRAMx_WDATA[7:0]	Input	Data Input Bits
BRAMx_nWCLKEN	Input	Write Clock Enable (active LOW)
REF_BRAMx_WRITE_CLK	Input	Reference Write Clock
BRAMx_WCLKINV	Input	Write Clock Inversion Control
BRAMx_RCLKINV	Input	Read Clock Inversion Control
BRAMx_nRCLKEN	Input	Read Clock Enable (active LOW)
REF_BRAMx_READ_CLK	Input	Reference Read Clock
BRAMx_RDATA[7:0]	Output	Data Output Bits
BRAMx_RADDR[8:0]	Input	Read Address Bits; for anything deeper than 512, the unused DINs can be repurposed as RADDR
BRAMx_nREN	Input	Read Enable (active LOW)
BRAMx_RATIO[1:0]	Input	Data Width Selection Bits 00: 512 x 8 01: 1024 x 4 10: 2048 x 2 11: 4096 x 1

9.3 BRAM Considerations

- Read Data Register Undefined Immediately After Configuration

  The initial value of RDATA read value is '0' during configuration. But once configured, the RDATA port does not automatically reset unlike the FFs in the Programmable Logic Blocks and Programmable IO pins.

- LOW Power Setting

  To place the BRAM block in its lowest power mode, keep BRAMx_nWCLKEN = 0 and BRAMx_nRCLKEN = 0. In other words, when not actively using the BRAM block, disable the clock inputs. BRAM blocks can be power gated with dedicated registers to minimize the power consumption.

9.4 Address Extension

To accommodate the previously mentioned bit-width configurability, a method for extending the memory address beyond its native 9 bits is required. This is accomplished by utilizing specific bits of the BRAMx_WDATA byte as address extension bits. In all address extension cases, the BRAMx_WDATA bits used will represent the least significant bits of the address.

Table 12. Write Address Extension using bits 5-7

	BRAMx_WADDR									BRAMx_WDATA								BRAMx_RDATA
512 x 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[7:0]
	A8	A7	A6	A5	A4	A3	A2	A1	A0									
1024 x 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[3:0]
	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0								
2048 x 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[1:0]
	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0							
4096 x 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[0]
	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0						

For write addressing, the BRAMx_WADDR and BRAMx_WDATA bits are shown above for each data width.

For read addressing, the same method of address extension is used, except bits 2-4 are used instead of bits 5-7.

Table 13. Read Address Extension using bits 2-4

	BRAMx_RADDR									BRAMx_RDATA								BRAMx_RDATA
512 x 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[7:0]
	A8	A7	A6	A5	A4	A3	A2	A1	A0									
1024 x 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[3:0]
	A9	A8	A7	A6	A5	A4	A3	A2	A1				A0					
2048 x 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[1:0]
	A10	A9	A8	A7	A6	A5	A4	A3	A2				A1	A0				
4096 x 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	[0]
	A11	A10	A9	A8	A7	A6	A5	A4	A3				A2	A1	A0			

9.4.1 Write Operations for BRAM

All write operations are synchronized to the rising edge of BRAMx_WCLK (default) when BRAMx_WCLKInv = 0, if BRAMx_WCLKInv = 1, then write operation happens on the falling edge.

To write data into the BRAM block, perform the following operations:

- Supply a valid address on the BRAMx_WADDR [8:0] address input port
- Supply valid data on the BRAMx_WDATA [7:0] data input port
- Enable the BRAM write port (BRAMx_nWEN = 0)
- Enable the BRAM write clock (BRAMx_nWCLKEN = 0)
- Apply a rising clock edge on WCLK (BRAMx_WCLKInv = 0).

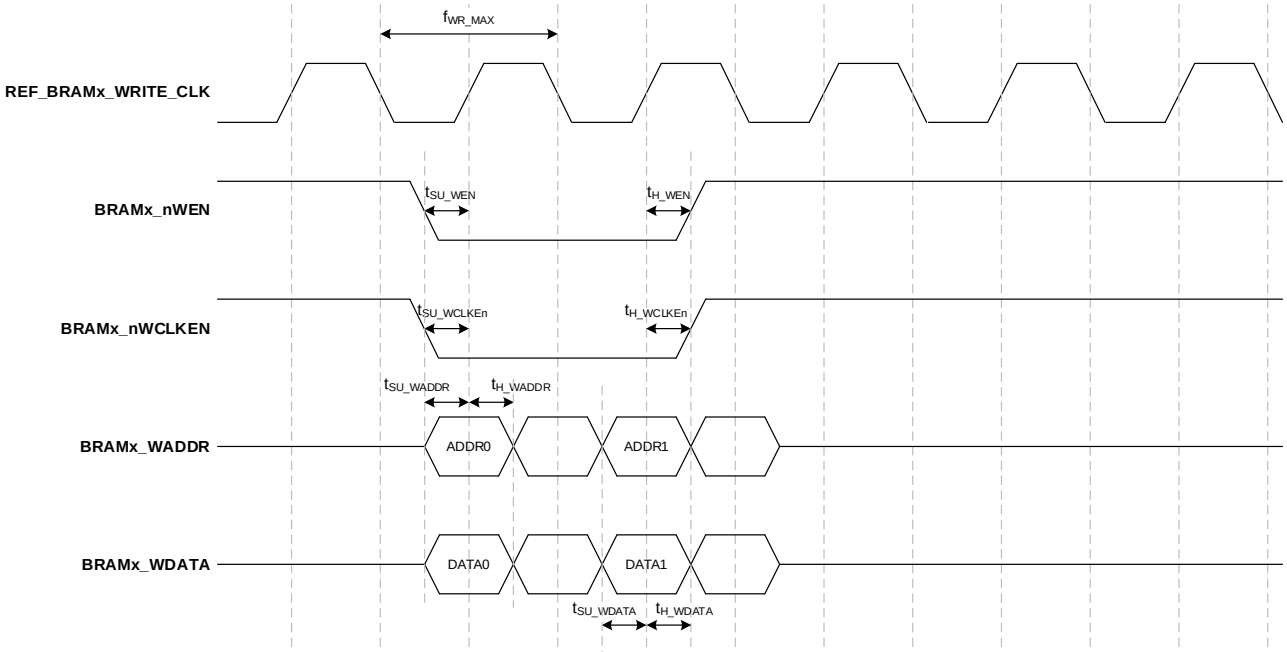


Figure 20. BRAM Timing Diagram for Write Operations

9.4.2 Read Operation for BRAM

All read operations are synchronized to the rising edge of BRAMx_RCLK when BRAMx_RCLKInv = 0, if BRAMx_RCLKInv = 1, then read operation happens on the falling edge.

To read data from the BRAM block, perform the following operations:

- Supply a valid address on the BRAMx_RADDR [8:0] address input port
- Enable the BRAM read port (BRAMx_nREN = 0)
- Enable the BRAM read clock (BRAMx_nRCLKEN = 0)
- Apply a rising edge clock on BRAMx_RCLK
- After the clock edge, the BRAM contents located at the specified address (BRAMx_RADDR) appear on the BRAMx_RDATA output port
- The read data is held when BRAMx_nREN is de-asserted.

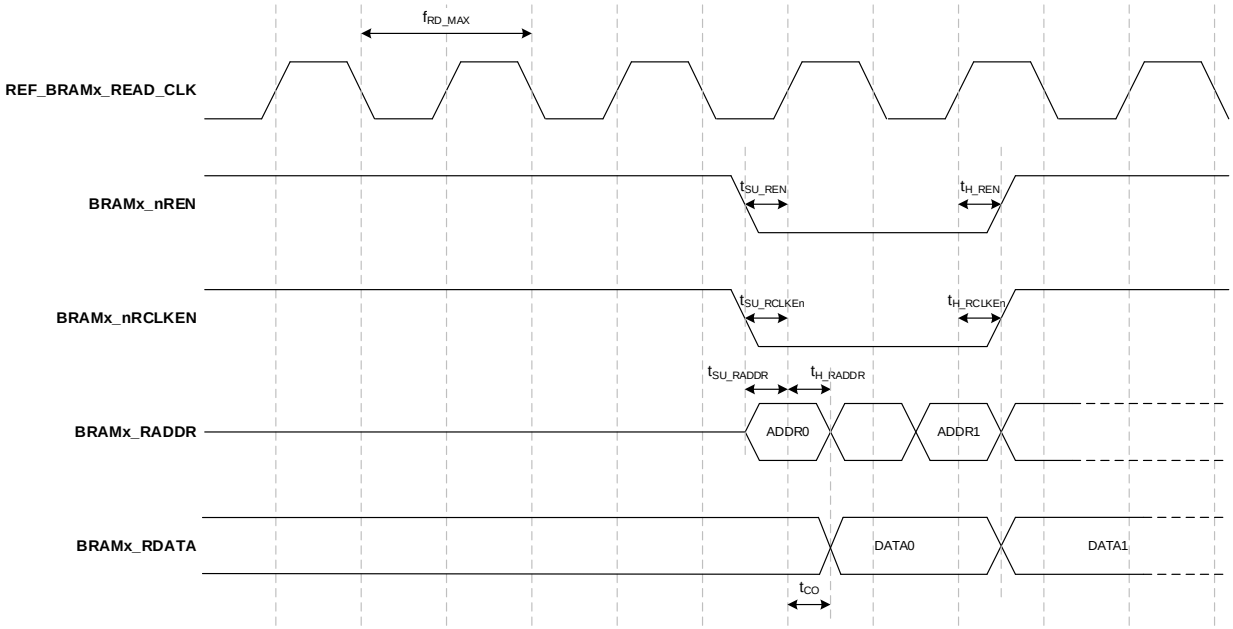
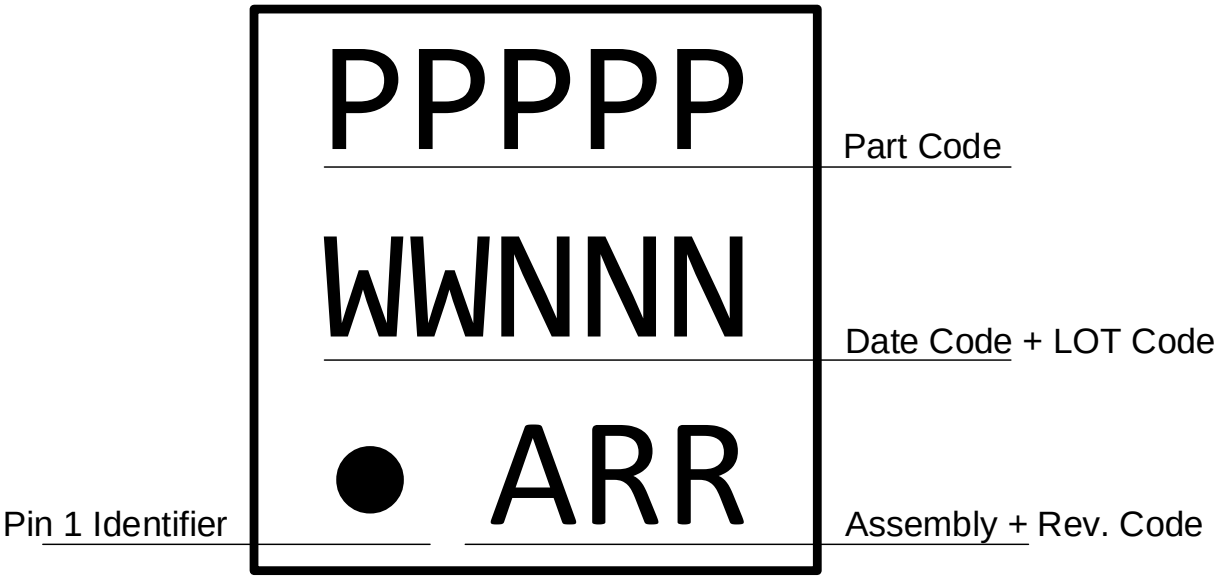


Figure 21. BRAM Timing Diagram for Read Operations

10. Package Top Marking Definitions

10.1 STQFN 24L 3.0 mm x 3.0 mm, 0.4P FCA



PPPPP – Part ID Field
WW – Date Code Field [1]
NNN – Lot Traceability Code Field [1]
A – Assembly Side Code Field [2]
RR – Part Revision Code Field [2]

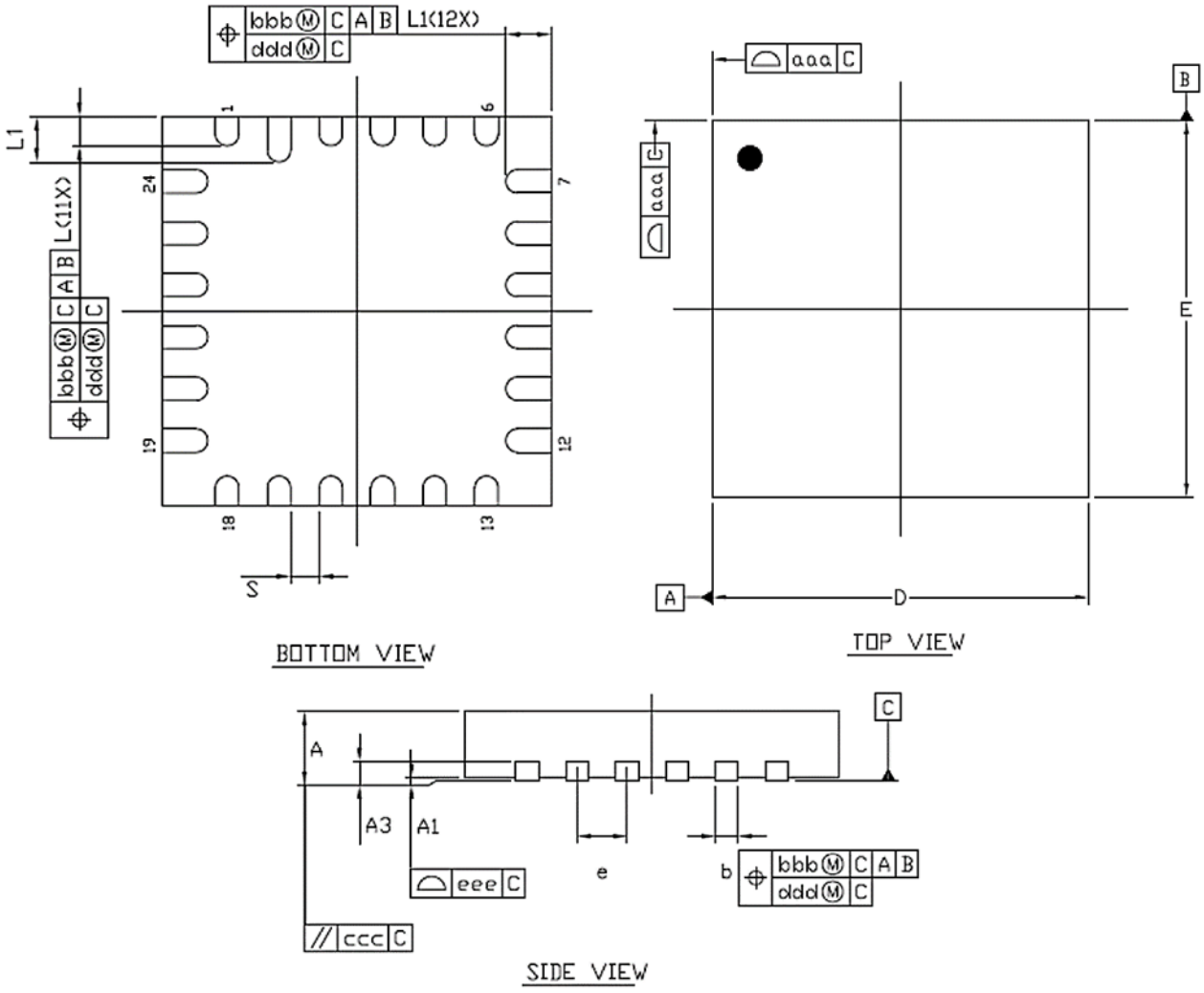
[1] Each character in the code field can be alphanumeric A – Z and 0 – 9.
[2] Character in code field can be alphanumeric A – Z.

Figure 22. STQFN-24 Package Top Marking

11. Package Information

11.1 Package Outline Drawing for STQFN 24L 3.0 mm x 3.0 mm x 0.55 mm, 0.4P FC Package

JEDEC MO-220



PKG CODE	UQFN					
SYMBOLS	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
b	0.13	0.18	0.23	0.005	0.007	0.009
D	2.95	3.00	3.05	0.116	0.118	0.120
E	2.95	3.00	3.05	0.116	0.118	0.120
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.30	0.35	0.40	0.012	0.014	0.016
S	0.22 REF.			0.009 REF.		
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

'A1' MAX LEAD COPLANARITY 0.05mm
STANDARD TOLERANCE : ±0.05

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

PAD SIZE	LEAD FINISH		JEDEC CODE
	Pure Tin	PPF	
	V	X	N/A

Figure 23. STQFN-24 Package Outline Drawing

11.2 Junction-to-Ambient Thermal Resistance (θ_{JA})

Table 14. Junction-to-Ambient Thermal Resistance

Package Option	Thermal Resistance (θ_{JA})
STQFN-24 (SLG47910V)	56 °C / W

11.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 15.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The STQFN-24L package is qualified for MSL 1.

Table 15. MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C/60 % RH
MSL 3	168 hours	30 °C/60 % RH
MSL 2A	4 weeks	30 °C/60 % RH
MSL 2	1 year	30 °C/60 % RH
MSL 1	Unlimited	30 °C/60 % RH

11.4 STQFN Handling

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

11.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12. Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to +85 °C. To guarantee reliable operation, the junction temperature of the SLG47910 must not exceed +150 °C.

13. Layout Guidelines

13.1 Layout Guidelines for STQFN 24L 3.0 mm x 3.0 mm x 0.55 mm, 0.4P FC Package

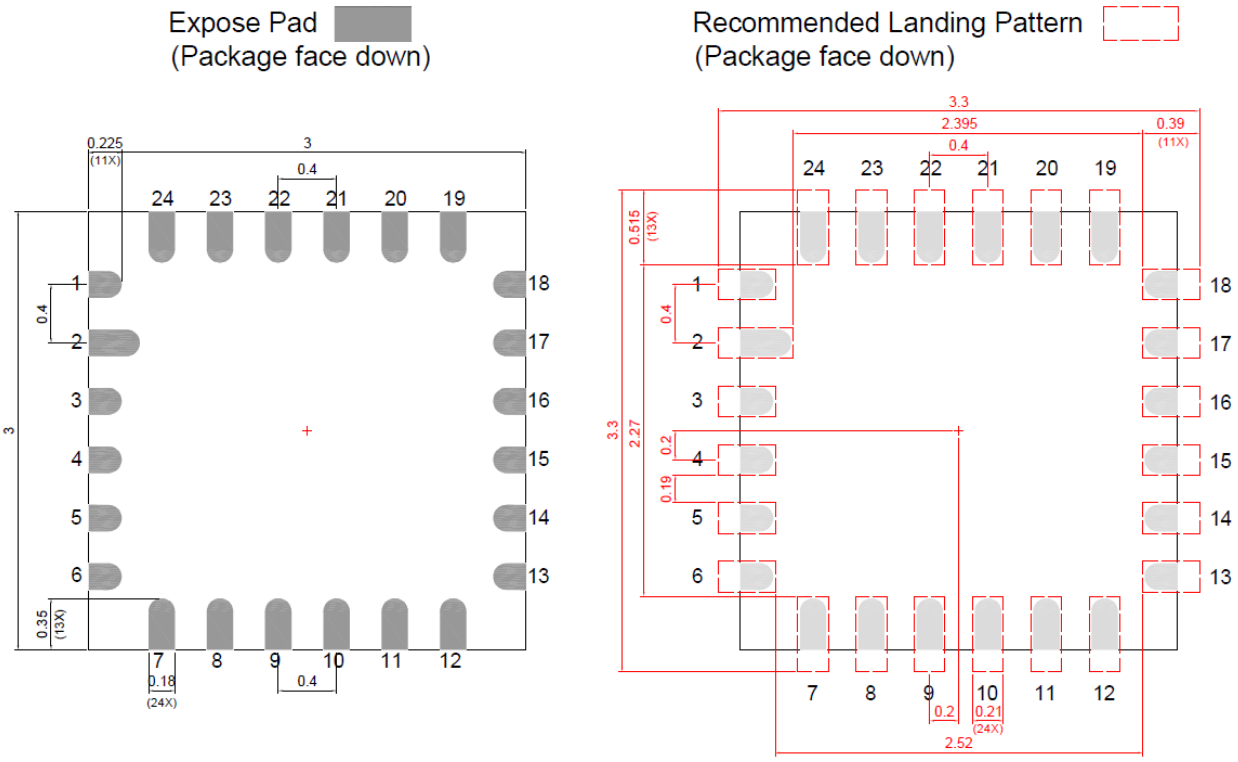


Figure 24. Recommended Landing Pattern for STQFN 24L

14. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
SLG47910V	24-pin STQFN	Tape and Reel	-40°C to +85°C

14.1 Tape and Reel Specifications

Table 16. Tape and Reel Specifications

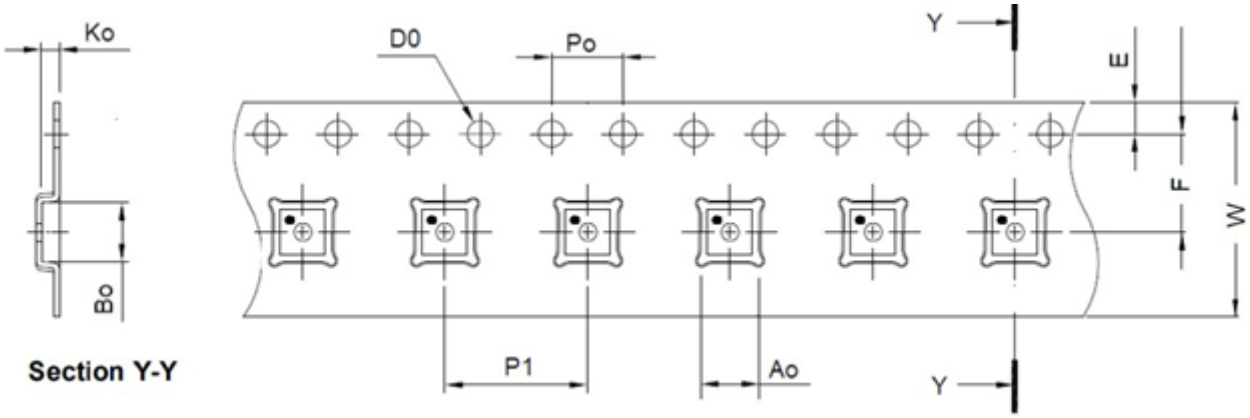
Package Type	# of Pins	Nominal Package size [mm]	Max units		Reel & Hub size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 24L 3.0 mm x 3.0 mm x 0.55 mm 0.4P FCA Green	24	3.0 x 3.0 x 0.55	5,000	10,000	330 / 100	42	336	42	336	12	8

14.2 Carrier Tape Drawing and Dimensions

Table 17. Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 24L 3.0 mm x 3.0 mm x 0.55 mm 0.4P FCA Green	3.3	3.3	0.8	4	8	1.55	1.75	5.5	12

14.2.1 STQFN 24L Carrier Tape Drawing



Note: Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Figure 25. Carrier Tape Drawing for STQFN 24L

Glossary

B

BRAM Block Random Access Memory

C

CLB Configurable Logic Blocks

CLBL Configurable Logic Blocks for Logic

CLBM Configurable Logic Blocks for Memory

E

EMM Embedded Memory Mode

EN nSLEEP

G

GPIO General Purpose Input/Output

I

IOB Input Output Buffers

L

LUT Look Up Table

LaC Logic-As-Clock

N

NVM Non-Volatile Memory

O

OTP One Time Programmable

OSC Oscillator

P

PLL Phase Locked Loops

POR Power-on Reset

PWR nRST

S

SCLK Serial Clock for SPI

SPI Serial Peripheral Interface

SRM Shift Register Mode

STQFN Super Thin Quad Flat No-Lead packaging

V

VCO Voltage-Controlled Oscillator

References

For related documents and software, please visit our website: https://www.renesas.com/us/en.

Download our free ForgeFPGA Designer software [1] and follow the steps in the software user guide [2]. Use Configuration Document to understand the different modes of configuration [3]. Renesas Electronics provides a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Renesas IC. Please visit the product page to download the following:

[1] GoConfigure Software Hub, Software Download, Renesas Electronics

[2] ForgeFPGA Workshop User Guide, Renesas Electronics

[3] ForgeFPGA Configuration Document, Renesas Electronics

[4] Application Notes, ForgeFPGA Application Notes & Design Files, Renesas Electronics

[5] ForgeFPGA Evaluation Board User Manual, Renesas Electronics.

A. Register Definitions

The table below represents the NVM Register Map as showcased in the GoConfigure Software.

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
0	[0]	[0]	Load configuration from OTP	0: device configuration from external SPI device (MCU (master) or SPI flash memory (slave)) 1: device configuration from internal OTP only and OTP R/W interface is locked	OTP	0
	[24:1]	[24:1]	Base address for SPI	XX..X: 24-bit address indicates the starting position for reading the configuration from a flash memory	OTP	0
	[25]	[25]	Disable OTP Read	0: OTP reading is allowed through OTP R/W interface 1: OTP reading is not allowed through OTP R/W interface Note: Once these bits are set, RMA analysis will be limited.	OTP	0
	[26]	[26]	Disable OTP Write	0: OTP writing is allowed through OTP R/W interface 1: OTP writing is not allowed through OTP R/W interface Note: Once these bits are set, RMA analysis will be limited.	OTP	0
	[27]	[27]	Reserved	Reserved	OTP	1
	[28]	[28]	Reserved	Reserved	OTP	0
	[29]	[29]	Reserved	Reserved	OTP	1
	[31:30]	[31:30]	Reserved	Reserved	OTP	0
1	[0]	[32]	Reserved	Reserved	OTP	0
	[12:1]	[44:33]	Reserved	Reserved	OTP	0
	[28:13]	[60:45]	Reserved	Reserved	OTP	0
	[31:29]	[63:61]	Reserved	Reserved	OTP	0
2	[31:0]	[95:64]	Reserved	Reserved	OTP	A5A5A5A5
3	[31:0]	[127:96]	Reserved	Reserved	OTP	0
4	[31:0]	[159:128]	Reserved	Reserved	OTP	0
5	[31:0]	[191:160]	Reserved	Reserved	OTP	5A5A5A5A
6	[0]	[192]	GPIO Keep Enable (REG_GPIO_KEEP)	0: GPO pins are in Hi-Z states when chips are in reset (after setting the logic '0' value at 'PIN_DEV_nRST' or after rising edge at 'INT_FPGA_RESET') 1: GPO pins keep their states when chips is in reset (after setting the logic '0' value at 'PIN_DEV_nRST' or after rising edge at 'INT_FPGA_RESET')	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
6	[1]	[193]	BRAM Keep Enable (REG_BRAM_KEEP)	0: SRAM instances do not retain their contents when chips are in reset (after setting the logic '0' value at 'PIN_DEV_nRST' or after rising edge at 'iob_int_dev_rst') 1: SRAM instances retain their contents when chips are in reset (after setting the logic '0' value at 'PIN_DEV_nRST' or after rising edge at 'iob_int_dev_rst')	OTP/SPI	0
	[2]	[194]	Reserved	Reserved	OTP/SPI	0
	[11:3]	[203:195]	Reserved	Reserved	OTP/SPI	0
	[12]	[204]	Reserved	Reserved	OTP/SPI	0
	[14:13]	[206:205]	Reserved	Reserved	OTP/SPI	0
	[15]	[207]	Reserved	Reserved	OTP/SPI	0
	[17:16]	[209:208]	Reserved	Reserved	OTP/SPI	0
	[18]	[210]	System waits for OSC/PLL to stabilize before entering functional mode	0: chip will transition from configuration/retention mode to function mode without waiting for OSC/PLL clock stabilization 1: chip will transition from configuration/retention mode to function mode after OSC/PLL clock is stable	OTP/SPI	0
	[19]	[211]	Logic-As-Clock1 output enable synchronizer control	0: LaC1 clock output is enabled Asynchronously 1: LaC1 clock output is enabled synchronously w.r.t iob_logic_as_clk1{user}	OTP/SPI	0
	[20]	[212]	Logic-As-Clock0 output enable synchronizer control	0: LaC0 clock output is enabled Asynchronously 1: LaC0 clock output is enabled synchronously w.r.t iob_logic_as_clk0{user}	OTP/SPI	0
	[21]	[213]	PLL clock output enable synchronizer control	0: PLL clock output will be enabled by iob_pll_en{user} asynchronously 1: PLL clock output will be enabled by iob_pll_en{user} synchronously	OTP/SPI	0
	[22]	[214]	OSC clock output enable synchronizer control	0: OSC clock output will be enabled by iob_osc_en{user} asynchronously 1: OSC clock output will be enabled by iob_osc_en{user} synchronously	OTP/SPI	0
	[23]	[215]	Sleep Mode source	0: Use nSLEEP (EN) pin to enter Sleep mode 1: Use INT_FPGA_SLEEP IOB to enter Sleep mode	OTP/SPI	0
	[24]	[216]	Chip Reset source	0: Use nRST (PWR) pin to reset the chip 1: Use INT_FPGA_RESET IOB to reset the chip	OTP/SPI	0
	[25]	[217]	Clocks gating Timeout control when entering Sleep	0: If user clocks will not stop (go LOW) within 5us after initiating enter to Sleep, they will be gated and Sleep sequence will continue 1: Chips will wait indefinitely for clock to stop (go LOW), sleep may not occur if any enabled clock stays HIGH.	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
6	[31:26]	[223:218]	Reserved	Reserved	OTP/SPI	0
7	[0]	[224]	GPIO0 2x Pull-up Resistor	GPIO0: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[1]	[225]	GPIO0 1x Pull-up Resistor	GPIO0: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[2]	[226]	GPIO0 Driver Type	GPIO0: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[3]	[227]	GPIO0 Driver Strength	GPIO0 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[4]	[228]	GPIO1 2x Pull-up Resistor	GPIO1: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[5]	[229]	GPIO1 1x Pull-up Resistor	GPIO1: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[6]	[230]	GPIO1 Driver Type	GPIO1: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[7]	[231]	GPIO1 Driver Strength	GPIO1: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[8]	[232]	GPIO2 2x Pull-up Resistor	GPIO2: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[9]	[233]	GPIO2 1x Pull-up Resistor	GPIO2: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[10]	[234]	GPIO2 Driver Type	GPIO2: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[11]	[235]	GPIO2 Driver Strength	GPIO2: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[12]	[236]	GPIO3 2x Pull-up Resistor	GPIO3: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[13]	[237]	GPIO3 1x Pull-up Resistor	GPIO3: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[14]	[238]	GPIO3 Driver Type	GPIO3: 0: Push-pull. 1: Open-drain.	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
7	[15]	[239]	GPIO3 Driver Strength	GPIO3: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[16]	[240]	GPIO4 2x Pull-up Resistor	GPIO4: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[17]	[241]	GPIO4 1x Pull-up Resistor	GPIO4: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[18]	[242]	GPIO4 Driver Type	GPIO4: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[19]	[243]	GPIO4 Driver Strength	GPIO4: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[20]	[244]	GPIO5 2x Pull-up Resistor	GPIO5: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[21]	[245]	GPIO5 1x Pull-up Resistor	GPIO5: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[22]	[246]	GPIO5 Driver Type	GPIO5: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[23]	[247]	GPIO5 Driver Strength	GPIO5: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[24]	[248]	GPIO6 2x Pull-up Resistor	GPIO6: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[25]	[249]	GPIO6 1x Pull-up Resistor	GPIO6: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[26]	[250]	GPIO6 Driver Type	GPIO6: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[27]	[251]	GPIO6 Driver Strength	GPIO6: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[28]	[252]	GPIO7 2x Pull-up Resistor	GPIO7: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[29]	[253]	GPIO7 1x Pull-up Resistor	GPIO7: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[30]	[254]	GPIO7 Driver Type	GPIO7: 0: Push-pull. 1: Open-drain.	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
7	[31]	[255]	GPIO7 Driver Strength	GPIO7: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
8	[0]	[256]	GPIO8 2x Pull-up Resistor	GPIO8: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[1]	[257]	GPIO8 1x Pull-up Resistor	GPIO8: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[2]	[258]	GPIO8 Driver Type	GPIO8: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[3]	[259]	GPIO8 Driver Strength	GPIO8: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[4]	[260]	GPIO9 2x Pull-up Resistor	GPIO9: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[5]	[261]	GPIO9 1x Pull-up Resistor	GPIO9: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[6]	[262]	GPIO9 Driver Type	GPIO9: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[7]	[263]	GPIO9 Driver Strength	GPIO9: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[8]	[264]	GPIO10 2x Pull-up Resistor	GPIO10: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[9]	[265]	GPIO10 1x Pull-up Resistor	GPIO10: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[10]	[266]	GPIO10 Driver Type	GPIO10: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[11]	[267]	GPIO10 Driver Strength	GPIO10: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[12]	[268]	GPIO11 2x Pull-up Resistor	GPIO11: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[13]	[269]	GPIO11 1x Pull-up Resistor	GPIO11: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[14]	[270]	GPIO11 Driver Type	GPIO11: 0: Push-pull. 1: Open-drain.	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
8	[15]	[271]	GPIO11 Driver Strength	GPIO11: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[16]	[272]	GPIO12 2x Pull-up Resistor	GPIO12: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[17]	[273]	GPIO12 1x Pull-up Resistor	GPIO12: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[18]	[274]	GPIO12 Driver Type	GPIO12: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[19]	[275]	GPIO12 Driver Strength	GPIO12: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[20]	[276]	GPIO13 2x Pull-up Resistor	GPIO13: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[21]	[277]	GPIO13 1x Pull-up Resistor	GPIO13: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[22]	[278]	GPIO13 Driver Type	GPIO13: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[23]	[279]	GPIO13 Driver Strength	GPIO13: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[24]	[280]	GPIO14 2x Pull-up Resistor	GPIO14: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[25]	[281]	GPIO14 1x Pull-up Resistor	GPIO14: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[26]	[282]	GPIO14 Driver Type	GPIO14: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[27]	[283]	GPIO14 Driver Strength	GPIO14: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[28]	[284]	GPIO15 2x Pull-up Resistor	GPIO15: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[29]	[285]	GPIO15 1x Pull-up Resistor	GPIO15: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[30]	[286]	GPIO15 Driver Type	GPIO15: 0: Push-pull. 1: Open-drain.	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
8	[31]	[287]	GPIO15 Driver Strength	GPIO15: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
9	[0]	[288]	GPIO18 2x Pull-up Resistor	GPIO16: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[1]	[289]	GPIO18 1x Pull-up Resistor	GPIO16: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[2]	[290]	GPIO18 Driver Type	GPIO16: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[3]	[291]	GPIO18 Driver Strength	GPIO16: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[4]	[292]	GPIO17 2x Pull-up Resistor	GPIO17: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[5]	[293]	GPIO17 1x Pull-up Resistor	GPIO17: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[6]	[294]	GPIO17 Driver Type	GPIO17: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[7]	[295]	GPIO17 Driver Strength	GPIO17: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[8]	[296]	GPIO16 2x Pull-up Resistor	GPIO18: 0: 2nd Pull-up resistor is disabled 1: 2nd Pull-up resistor is enabled	OTP/SPI	0
	[9]	[297]	GPIO16 1x Pull-up Resistor	GPIO18: 0: 1st Pull-up resistor is disabled 1: 1st Pull-up resistor is enabled	OTP/SPI	1
	[10]	[298]	GPIO16 Driver Type	GPIO18: 0: Push-pull. 1: Open-drain.	OTP/SPI	0
	[11]	[299]	GPIO16 Driver Strength	GPIO18: 0: Digital output with 1x strength 1: Digital output with 2x strength	OTP/SPI	0
	[15:12]	[303:300]	Reserved	Reserved	OTP/SPI	0
	[16]	[304]	nRST (PWR) PAD auto Pull-up control	1: nRST (PWR) pad Pull-up is always on. 0: auto - Pull-up follows input state.	OTP/SPI	0 (STQFN 24);
	[17]	[305]	nSLEEP (EN) PAD PAD auto Pull-up control	1: nSLEEP (EN) pad Pull-up is always on. 0: auto - Pull-up follows input state.	OTP/SPI	0
	[31:18]	[319:306]	Reserved	Reserved	OTP/SPI	0

Register	Relative Bit Address	Abs Bit Address	Signal Function	Signal Description	Register Bits Loaded from	Default Value
10	[0]	[320]	BRAM [3:0] Power down	0: BRAM enabled 1: BRAM disabled (default).	OTP/SPI	1
	[1]	[321]	BRAM [7:4] Power down	0: BRAM enabled 1: BRAM disabled (default).	OTP/SPI	1
	[31:2]	[351:322]	Reserved	Reserved	OTP/SPI	0
11	[31:0]	[383:352]	Reserved	Reserved	OTP/SPI	0
12	[31:0]	[415:384]	Reserved	Reserved	OTP/SPI	0
13	[31:0]	[447:416]	Reserved	Reserved	OTP/SPI	0
14	[31:0]	[479:448]	Reserved	Reserved	OTP/SPI	0

Revision History

Revision	Date	Description
1.04	Feb 25, 2025	Changed I_{OL}/I_{OH} values in GPIO Specifications under Electrical Specifications Section Updated Power-Up and Configuration Sequence Section Fixed typos and formatting Changed GPIO Functionality Table Fixed POR, BRAM images
1.03	Oct 31, 2024	Increased maximum V_{DDIO} to 3.465 V and added characteristics data for it Edited the POR specifications and Figure Added Ambient Temperature specifications Fixed typos and formatting
1.02	Jun 27, 2024	Updated package references to STQFN packaging Updated Absolute Max Ratings disclaimer. Fixed typ. value for Output Duty Cycle in 3.3.4 Oscillator Specifications Fixed some formatting
1.01	Jun 20, 2024	Fixed typos Improved image quality for some charts and diagrams Moved Revision History to last page
1.00	May 31, 2024	Production Release