# GreenPAK Programmable Mixed Signal Matrix with Dual 44 mΩ/2 A P-FET

## General Description

The SLG46867 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins and the macrocells of the SLG46867. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

## Key Features

- Two High Speed General Purpose Analog Comparators (ACMPxH)
- Two Low Power General Purpose Analog Comparators (ACMPxL)
- Two Voltage References (Vref)
  - Two Vref Outputs
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Nine Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/Latch or 4-bit LUTs
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/Latch or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/Latch or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - $I^2C$ Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset (POR)
- Dual P-FET Power Switch
- Read Back Protection (Read Lock)
- Power Supply
  - 2.5 V (±8 %) to 5 V (±10 %)
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant/Halogen-Free/Pb-Free
- Available Package
  - 1.6 mm x 3.0 mm x 0.4 mm 20-pin MSTQFN package

## Applications

- Power Sequencing with Complex Analog Control
- Power Plane Component Size Reduction Project
- Consumer Electronics
- LED Driver
- Haptic Motor Driver
- System RESET with Power Switch

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# 1 Block Diagram

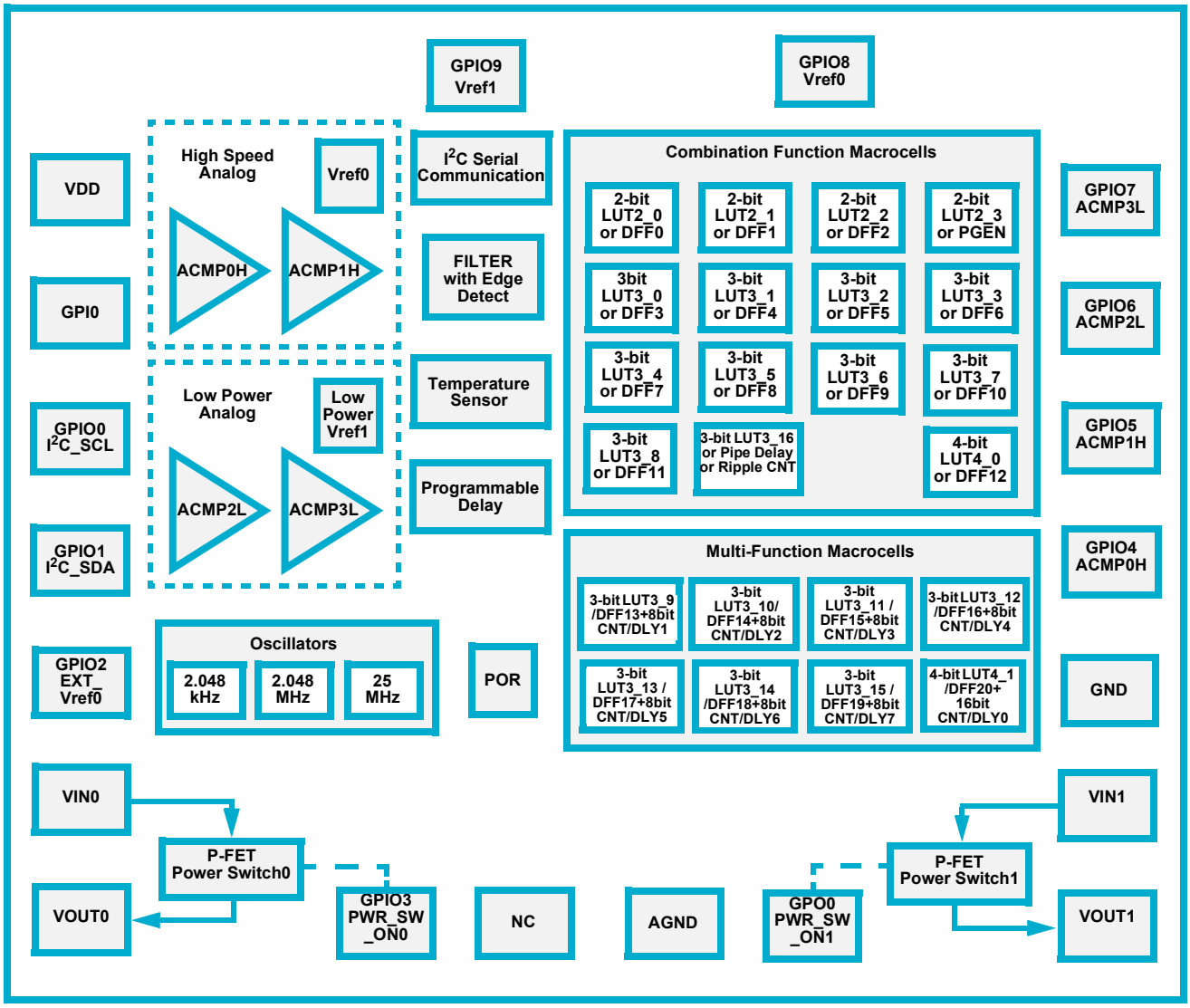
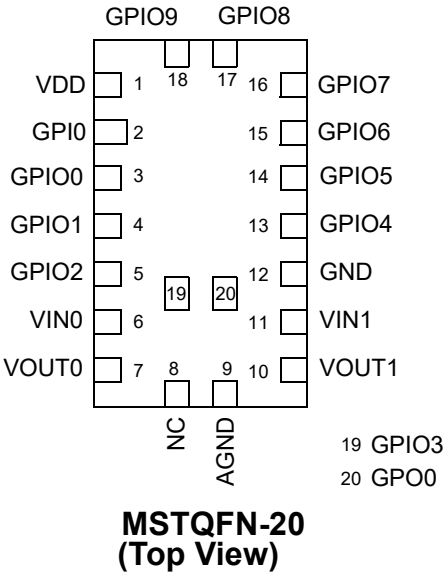



**Figure 1: Block Diagram**

# 2 Pinout

## 2.1 PIN CONFIGURATION - MSTQFN- 20L




**MSTQFN-20**
**(Top View)**

| Pin # | Signal Name | Pin Functions |
|---|---|---|
| 1 | $V_{DD}$ | Power Supply |
| 2 | GPI0 | GPI, SLA_0 |
| 3 | GPIO0 | GPIO, SCL |
| 4 | GPIO1 | GPIO, SDA |
| 5 | GPIO2 | GPIO with OE, EXT_Vref0, SLA_1 |
| 6 | VIN0 | P-FET Power Switch Input |
| 7 | VOUT0 | P-FET Power Switch Output |
| 8 | NC | No Connect |
| 9 | AGND | P-FET Power Switch Ground |
| 10 | VOUT1 | P-FET Power Switch Output |
| 11 | VIN1 | P-FET Power Switch Input |
| 12 | GND | Ground |
| 13 | GPIO4 | GPIO with OE, ACMP0H+, SLA_2 |
| 14 | GPIO5 | GPIO with OE, ACMP1H+, SLA_3 |
| 15 | GPIO6 | GPIO with OE, ACMP2L+ |
| 16 | GPIO7 | GPIO with OE, ACMP3L+ |
| 17 | GPIO8 | GPIO with OE, Vref0_OUT, TS_OUT |
| 18 | GPIO9 | GPIO with OE, Vref1_OUT |
| 19 | GPIO3<br>PWR_SW_ON0 | GPIO with OE, P-FET Power Switch On |
| 20 | GPO0<br>PWR_SW_ON1 | GPO, P-FET Power Switch On |

*Legend:*

**OE**: Output Enable
**ACMPx+**: ACMPx Positive Input
**ACMPx-**: ACMPx Negative Input
**SCL**: $I^2C$ Clock Input
**SDA**: $I^2C$ Data Input/Output
**Vrefx**: Voltage Reference Output
**EXT_CLKx**: External Clock Input
**SLA:** Slave Address
**TS_OUT**: Temperature Output

**Table 1: Functional Pin Description**

| MSTQFN 20L Pin # | Pin Name | Signal Name | Function | Input Options | Output Options |
|---|---|---|---|---|---|
| 1 | VDD | VDD | Power Supply | -- | -- |
| | | ACMP0_H+ | Analog Comparator 0 Positive Input | Analog | -- |
| | | ACMP1_H+ | Analog Comparator 1 Positive Input | Analog | -- |
| | | ACMP2_L+ | Analog Comparator 2 Positive Input | Analog | -- |
| | | ACMP3_L+ | Analog Comparator 3 Positive Input | Analog | -- |
| 2 | GPI0 | GPI0 | General Purpose Input | Digital Input without Schmitt Trigger | -- |
| | | | | Digital Input with Schmitt Trigger | -- |
| | | | | Low Voltage Digital Input | -- |
| | | Slave Address 0 | | -- | -- |
| 3 | GPIO0 | GPIO0 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | SCL | $I^2C$ Serial Clock | Digital Input without Schmitt Trigger | -- |
| | | | | Digital Input with Schmitt Trigger | -- |
| | | | | Low Voltage Digital Input | -- |
| 4 | GPIO1 | GPIO1 | General Purpose IO | Digital Input without Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | |
| | | | | Low Voltage Digital Input | |
| | | SDA | $I^2C$ Serial Data | Digital Input without Schmitt Trigger | -- |
| | | | | Digital Input with Schmitt Trigger | -- |
| | | | | Low Voltage Digital Input | -- |
| 5 | GPIO2 | GPIO2 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | Slave Address 1 | | -- | -- |
| | | EXT_Vref0 | Analog Comparator Negative Input | Analog | -- |
| 6 | VIN0 | VIN0 | P-FET Power Switch Input | -- | -- |

**Table 1: Functional Pin Description** (continued)

| MSTQFN 20L Pin # | Pin Name | Signal Name | Function | Input Options | Output Options |
|---|---|---|---|---|---|
| 7 | VOUT0 | VOUT0 | P-FET Power Switch Output | -- | -- |
| 8 | NC | NC | No Connect | -- | -- |
| 9 | AGND | AGND | P-FET Power Switch Ground | -- | -- |
| 10 | VOUT1 | VOUT1 | P-FET Power Switch Output | -- | -- |
| 11 | VIN1 | VIN1 | P-FET Power Switch Input | -- | -- |
| 12 | GND | GND | Power Supply | -- | -- |
| 13 | GPIO4 | GPIO4 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) (4x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) (4x) |
| | | | | Low Voltage Digital Input | -- |
| | | ACMP0_H+ | Analog Comparator 0_H Positive Input | Analog | -- |
| | | Slave Address 2 | | -- | -- |
| 14 | GPIO5 | GPIO5 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | ACMP1_H+ | Analog Comparator 1_H Positive Input | Analog | -- |
| | | Slave address 3 | | -- | -- |
| 15 | GPIO6 | GPIO6 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | ACMP2_L+ | Analog Comparator 2_L Positive Input | Analog | -- |
| 16 | GPIO7 | GPIO7 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | ACMP3_L+ | Analog Comparator 3_L Positive Input | Analog | -- |
| 17 | GPIO8 | GPIO8 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | Vref0 | Vref0 Output | Analog | -- |

**Table 1: Functional Pin Description** (continued)

| MSTQFN 20L Pin # | Pin Name | Signal Name | Function | Input Options | Output Options |
|---|---|---|---|---|---|
| 18 | GPIO9 | GPIO9 | General Purpose IO with OE **(Note 1)** | Digital Input without Schmitt Trigger | Push-Pull (1x) (2x) |
| | | | | Digital Input with Schmitt Trigger | Open Drain NMOS (1x) (2x) |
| | | | | Low Voltage Digital Input | -- |
| | | Vref1 | Vref1 Output | Analog | -- |
| 19 | GPIO3 | PWR_SW_ON0 | ON0 turns Power Switch 0 ON | P-FET gate with 200 Ω resistor | -- |
| 20 | GPO0 | PWR_SW_ON1 | ON1 turns Power Switch 1 ON | P-FET gate with 200 Ω resistor | -- |

**Note 1** General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

# 3 Characteristics

## 3.1 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Table 2: Absolute Maximum Ratings**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{HIGH}$ to GND | | -0.3 | 7 | V |
| Voltage at Input Pin | | -0.3 | 7 | V |
| Maximum Average or DC Current (Through $V_{DD}$ or GND pin) | | -- | 90 | mA |
| Current at Input Pin | | -1.0 | 1.0 | mA |
| Storage Temperature Range | | -65 | 150 | °C |
| Junction Temperature | | -- | 150 | °C |
| ESD Protection (Human Body Model) | | 2000 | -- | V |
| ESD Protection (Charged Device Model) | | 1300 | -- | V |
| Moisture Sensitive Level | | 1 | | |
| $V_{IN}$ | P-FET | 0.3 | $V_{DD}$ | V |
| $\Theta_{JA}$ | Thermal Resistance **(Note 1)** | -- | 99 | °C/W |
| $P_D$ | Maximum Power Dissipation, $T_A$ = +25 °C | -- | 1.25 | W |
| $T_{J,MAX}$ | Maximum Junction Temperature | | 150 | °C |
| P-FET Power Switch $IDS_{CONT}$ | Total, $T_J$ < 150°C | -- | 2 | A |
| P-FET Power Switch $IDS_{PK}$ | For no more than 1 ms with 1 % duty cycle | -- | 2.5 | A |
| **Note 1** Mounted on 27.4mm x 30.1 mm PCB (1.6 mm thick, 1 oz copper, FR-4 material). | | | | |

## 3.2 RECOMMENDED OPERATING CONDITIONS

**Table 3: Recommended Operating Conditions**

| Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage ($V_{DD}$) | | 2.3 | 5.5 | V |
| Operating Temperature | | -40 | 85 | °C |
| Maximal Voltage Applied to any PIN in High Impedance State | | -- | $V_{DD}$+ 0.3 | V |
| Capacitor Value at $V_{DD}$ | | 0.1 | -- | µF |
| Analog Input Common Mode Range | Allowable Input Voltage at Analog Pins | 0 | $V_{DD}$ | V |

### 3.3 ELECTRICAL CHARACTERISTICS

**Table 4: EC at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V Unless Otherwise Noted**

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH-Level Input Voltage | Logic Input **(Note 1)** | 0.7x $V_{DD}$ | -- | $V_{DD}$+ 0.3 | V |
| | | Logic Input with Schmitt Trigger | 0.8x $V_{DD}$ | -- | $V_{DD}$+ 0.3 | V |
| | | Low-Level Logic Input **(Note 1)** | 1.25 | -- | $V_{DD}$+ 0.3 | V |
| $V_{IL}$ | LOW-Level Input Voltage | Logic Input **(Note 1)** | GND- 0.3 | -- | 0.3x $V_{DD}$ | V |
| | | Logic Input with Schmitt Trigger | GND- 0.3 | -- | 0.2x $V_{DD}$ | V |
| | | Low-Level Logic Input **(Note 1)** | GND- 0.3 | -- | 0.5 | V |
| $V_{OH}$ | HIGH-Level Output Voltage | Push-Pull, 1X Drive, $V_{DD}$ = 2.5 V ± 8%, $I_{OH}$ = 1 mA | 2.16 | -- | -- | V |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 3.3 V ± 10%, $I_{OH}$ = 3 mA | 2.7 | -- | -- | V |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 5 V ± 10%, $I_{OH}$ = 5 mA | 4.1 | -- | -- | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 2.5 V ± 8%, $I_{OH}$ = 1 mA | 2.23 | -- | -- | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 3.3 V ± 10%, $I_{OH}$ = 3 mA | 2.8 | -- | -- | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 5 V ± 10%, $I_{OH}$ = 5 mA | 4.3 | -- | -- | V |
| $V_{OL}$ | LOW-Level Output Voltage | Push-Pull, 1X Drive, $V_{DD}$ = 2.5 V ± 8%, $I_{OL}$= 1 mA | -- | -- | 0.099 | V |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 3.3 V ± 10%, $I_{OL}$ = 3 mA | -- | -- | 0.16 | V |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 5 V ± 10%, $I_{OL}$= 5 mA | -- | -- | 0.27 | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 2.5 V ± 8%, $I_{OL}$ = 1 mA | -- | -- | 0.052 | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 3.3 V ± 10%, $I_{OL}$= 3 mA | -- | -- | 0.08 | V |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 5 V ± 10%, $I_{OL}$ = 5 mA | -- | -- | 0.18 | V |

**Table 4: EC at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V Unless Otherwise Noted** (continued)

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | HIGH-Level Output Pulse Current **(Note 2)** | Push-Pull, 1X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OH}$ = $V_{DD}$ - 0.2 | 1.5 | -- | -- | mA |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OH}$ = 2.4 V | 5.29 | -- | -- | mA |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OH}$ = 2.4 V | 18.53 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OH}$ = $V_{DD}$ - 0.2 | 2.94 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OH}$ = 2.4 V | 10.38 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OH}$ = 2.4 V | 36.43 | -- | -- | mA |
| $I_{OL}$ | LOW-Level Output Pulse Current **(Note 2)** | Push-Pull, 1X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OL}$ = 0.15 V | 1.57 | -- | -- | mA |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OL}$ = 0.4 V | 4.68 | -- | -- | mA |
| | | Push-Pull, 1X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OL}$ = 0.4 V | 6.50 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OL}$ = 0.15 V | 3.10 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OL}$ = 0.4 V | 9.69 | -- | -- | mA |
| | | Push-Pull, 2X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OL}$ = 0.4 V | 12.82 | -- | -- | mA |
| | | NMOS OD, 1X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OL}$ = 0.15 V | 3.84 | -- | -- | mA |
| | | NMOS OD, 1X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OL}$ = 0.4 V | 12.07 | -- | -- | mA |
| | | NMOS OD, 1X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OL}$ = 0.4 V | 16.02 | -- | -- | mA |
| | | NMOS OD, 2X Drive, $V_{DD}$ = 2.5 V ± 8%, $V_{OL}$ = 0.15 V | 7.39 | -- | -- | mA |
| | | NMOS OD, 2X Drive, $V_{DD}$ = 3.3 V ± 10%, $V_{OL}$ = 0.4 V | 22.97 | -- | -- | mA |
| | | NMOS OD, 2X Drive, $V_{DD}$ = 5 V ± 10%, $V_{OL}$ = 0.4 V | 28.47 | -- | -- | mA |
| $T_{SU}$ | Startup Time | From $V_{DD}$ rising past $PON_{THR}$ | -- | 1 | 2 | ms |
| $PON_{THR}$ | Power-On Threshold | $V_{DD}$ Level Required to Start Up the Chip | 1.6 | 1.85 | 2.05 | V |
| $POFF_{THR}$ | Power-Off Threshold | $V_{DD}$ Level Required to Switch Off the Chip | 0.85 | 1.25 | 1.5 | V |
| $R_{PULL}$ | Pull Up or Pull Down Resistance | 1 M for Pull Up: $V_{IN}$ = GND; for Pull Down: $V_{IN}$ = $V_{DD}$ | 0.6 | 1.0 | 1.4 | MΩ |
| | | 100 k for Pull Up: $V_{IN}$ = GND; for Pull Down: $V_{IN}$ = $V_{DD}$ | 60 | 100 | 140 | kΩ |
| | | 10 k For Pull Up: $V_{IN}$ = GND; for Pull Down: $V_{IN}$ = $V_{DD}$ | 6 | 10 | 14 | kΩ |
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |

**Table 4: EC at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V Unless Otherwise Noted** (continued)

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Note 1** No hysteresis<br>**Note 2** DC or average current through any pin should not exceed value given in Absolute Maximum Conditions. | | | | | | |

**Table 5: EC of the $I^2C$ Pins at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V Unless Otherwise Noted**

| Symbol | Parameter | Condition | Fast-Mode | | Fast-Mode Plus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{IL}$ | LOW-level Input Voltage | | -0.5 | $0.3V_{DD}$ | -0.5 | $0.3\ V_{DD}$ | V |
| $V_{IH}$ | HIGH-level Input Voltage | | $0.7V_{DD}$ | 5.5 | $0.7V_{DD}$ | 5.5 | V |
| $V_{HYS}$ | Hysteresis of Schmitt Trigger Inputs | | $0.05V_{DD}$ | -- | $0.05V_{DD}$ | -- | V |
| $V_{OL1}$ | LOW-Level Output Voltage 1 | (open drain or open collector) at 3mA sink current $V_{DD}$ > 2 V | 0 | 0.4 | 0 | 0.4 | V |
| $V_{OL2}$ | LOW-Level Output Voltage 2 | (open drain or open collector) at 2 mA sink current $V_{DD} \le 2$ V | 0 | $0.2V_{DD}$ | 0 | $0.2V_{DD}$ | V |
| $I_{OL}$ | LOW-Level Output Current **(Note 1)** | $V_{OL}$ = 0.4 V, $V_{DD}$ = 2.3 V | 3 | -- | 19.5 | -- | mA |
| | | $V_{OL}$ = 0.4 V, $V_{DD}$ = 3.0 V | 3 | -- | 20 | -- | mA |
| | | $V_{OL}$ = 0.4 V, $V_{DD}$ = 4.5 V | 3 | -- | 20 | -- | mA |
| | | $V_{OL}$= 0.6 V | 6 | -- | -- | -- | mA |
| $t_{of}$ | Output Fall Time from $V_{IHmin}$ to $V_{ILmax}$ **(Note 1)** | | 14x (VDD/5.5V) | 250 | 10x (VDD/5.5V) | 120 | ns |
| $t_{SP}$ | Pulse Width of Spikes that must be suppressed by the Input Filter | | 0 | 50 | 0 | 50 | ns |
| $I_i$ | Input Current each IO Pin | $0.1V_{DD} < V_I < 0.9V_{DDmax}$ | -10 | +10 | -10 | +10 | µA |
| $C_i$ | Capacitance for each IO Pin | | -- | 10 | -- | 10 | pF |
| **Note 1** Does not meet standard $I^2C$ specifications: $t_{of}$ = 20x(VDD/5.5V) (min); For Fast-mode Plus $I_{OL}$= 20 mA (min) at $V_{OL}$ = 0.4 V.<br>**Note 2** For Fast-mode Plus SDA pin must be configured as 2x NMOS open drain, see registers [785:784] in section 18. | | | | | | | |

**Table 6: $I^2C$ Pins Timing Characteristics T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted**

| Symbol | Parameter | Condition | Fast-Mode | | Fast-Mode Plus | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $F_{SCL}$ | Clock Frequency, SCL | | -- | 400 | -- | 1000 | kHz |
| $t_{LOW}$ | Clock Pulse Width Low | | 1300 | -- | 500 | -- | ns |
| $t_{HIGH}$ | Clock Pulse Width High | | 600 | -- | 260 | -- | ns |
| $t_I$ | Input Filter Spike Suppression (SCL, SDA) | $V_{DD}$ = 2.5 V ± 8% | -- | 95 | -- | 168 | ns |
| | | $V_{DD}$ = 3.3 V ± 10% | -- | 95 | -- | 157 | |
| | | $V_{DD}$ = 5.0 V ± 10% | -- | 111 | -- | 156 | |
| $t_{AA}$ | Clock Low to Data Out Valid | | -- | 900 | -- | 450 | ns |
| $t_{BUF}$ | Bus Free Time between Stop and Start | | 1300 | -- | 500 | -- | ns |
| $t_{HD\_STA}$ | Start Hold Time | | 600 | -- | 260 | -- | ns |
| $t_{SU\_STA}$ | Start Set-up Time | | 600 | -- | 260 | -- | ns |
| $t_{HD\_DAT}$ | Data Hold Time | | 0 | -- | 0 | -- | ns |
| $t_{SU\_DAT}$ | Data Set-up Time | | 100 | -- | 50 | -- | ns |
| $t_R$ | Inputs Rise Time | | -- | 300 | -- | 120 | ns |
| $t_F$ | Inputs Fall Time | | -- | 300 | -- | 120 | ns |
| $t_{SU\_STD}$ | Stop Set-up Time | | 600 | -- | 260 | -- | ns |
| $t_{DH}$ | Data Out Hold Time | | 50 | -- | 50 | -- | ns |

**Note 1** Timing diagram can be found in the Figure 85.

**Table 7: Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C**

| Parameter | Description | Note | $V_{DD}$ = 2.5 V | $V_{DD}$ = 3.3 V | $V_{DD}$ = 5.0 V | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Current | Chip Quiescent | 0.05 | 0.08 | 0.14 | µA |
| | | Vref0 | 11.10 | 11.17 | 11.91 | µA |
| | | Vref1 | 4.86 | 4.92 | 5.21 | µA |
| | | OSC2 25 MHz, pre-divider = 1 | 51.11 | 63.41 | 91.63 | µA |
| | | OSC2 25 MHz, pre-divider = 4 | 33.90 | 40.40 | 56.10 | µA |
| | | OSC2 25 MHz, pre-divider = 8 | 30.75 | 36.20 | 49.58 | µA |
| | | OSC1 2.048 MHz, pre-divider = 1 | 21.15 | 22.52 | 25.50 | µA |
| | | OSC1 2.048 MHz, pre-divider = 4 | 19.06 | 19.72 | 21.14 | µA |
| | | OSC1 2.048 MHz, pre-divider = 8 | 18.97 | 19.51 | 20.68 | µA |
| | | OSC0 2.048 kHz, pre-divider = 1 | 0.63 | 0.67 | 0.79 | µA |
| | | OSC0 2.048 kHz, pre-divider = 4 | 0.63 | 0.67 | 0.78 | µA |
| | | OSC0 2.048 kHz, pre-divider = 8 | 0.63 | 0.67 | 0.78 | µA |
| | | 1x push-pull + 4 pF @ 2.048 k | 0.34 | 0.36 | 0.47 | µA |
| | | 1x push-pull + 4 pF @ 2.048 M | 52.4 | 64.6 | 90.4 | µA |
| | | Temperature Sensor | 14.89 | 14.96 | 15.34 | µA |
| | | All ACMPs (includes internal Vref, Vin+ = 0) | 37.69 | 38.42 | 40.69 | µA |
| | | Any ACMPxH (includes internal Vref, Vin+ = 0) | 21.89 | 22.28 | 23.47 | µA |
| | | ACMP0H 100µA Enabled (includes internal Vref, Vin+ = 0) | 46.79 | 47.32 | 49.33 | µA |
| | | Any ACMPxL (includes internal Vref, Vin+ = 0) | 1.67 | 1.70 | 1.81 | µA |

## 3.4 TIMING CHARACTERISTICS

**Table 8: Typical Delay Estimated for Each Macrocell at T = 25 °C**

| Parameter | Description | Note | $V_{DD}$ = 2.5 V | | $V_{DD}$ = 3.3 V | | $V_{DD}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Rising | Falling | Rising | Falling | Rising | Falling | |
| tpd | Delay | Digital Input to PP 1X | 27 | 29 | 19 | 21 | 14 | 16 | ns |
| tpd | Delay | Digital Input to PP 2X | 24 | 26 | 17 | 19 | 13 | 14 | ns |
| tpd | Delay | Digital Input with Schmitt Trigger to PP 1X | 27 | 29 | 19 | 21 | 14 | 16 | ns |
| tpd | Delay | Low Voltage Digital Input to PP 1X | 38 | 241 | 26 | 164 | 18 | 104 | ns |
| tpd | Delay | Digital input to NMOS 1x | -- | 25 | -- | 19 | -- | 14 | ns |
| tpd | Delay | Digital input to NMOS 2x | -- | 24 | -- | 18 | -- | 13 | ns |
| tpd | Delay | Digital input to NMOS 4x | -- | 24 | -- | 17 | -- | 13 | ns |
| tpd | Delay | Output enable from Pin, OE Hi-Z to 1 | 26 | -- | 19 | -- | 14 | -- | ns |
| tpd | Delay | Output enable from Pin, OE Hi-Z to 0 | -- | 25 | -- | 18 | -- | 13 | ns |
| tpd | Delay | 1x3 State Hi-Z to 1 | 26 | -- | 19 | -- | 14 | -- | ns |
| tpd | Delay | 1x3 State Hi-Z to 0 | -- | 25 | -- | 18 | -- | 13 | ns |

**Table 8: Typical Delay Estimated for Each Macrocell at T = 25 °C** (continued)

| Parameter | Description | Note | $V_{DD}$ = 2.5 V | | $V_{DD}$ = 3.3 V | | $V_{DD}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Rising | Falling | Rising | Falling | Rising | Falling | |
| tpd | Delay | 2x3 State Hi-Z to 1 | 23 | -- | 17 | -- | 12 | -- | ns |
| tpd | Delay | 2x3 State Hi-Z to 0 | -- | 22 | -- | 16 | -- | 12 | ns |
| tpd | Delay | Latch Q | 16 | 18 | 11 | 13 | 8 | 9 | ns |
| tpd | Delay | Latch nQ | 19 | 15 | 14 | 11 | 9 | 7 | ns |
| tpd | Delay | Latch nRESET High Q | 25 | 21 | 17 | 15 | 12 | 10 | ns |
| tpd | Delay | Latch nRESET High nQ | 22 | 24 | 16 | 17 | 11 | 12 | ns |
| tpd | Delay | Latch nRESET Low Q | 22 | 23 | 15 | 16 | 11 | 11 | ns |
| tpd | Delay | Latch nRESET Low nQ | 24 | 21 | 17 | 15 | 12 | 10 | ns |
| tpd | Delay | Latch nSET High Q | 19 | 21 | 14 | 15 | 9 | 10 | ns |
| tpd | Delay | Latch nSET High nQ | 22 | 19 | 16 | 13 | 11 | 9 | ns |
| tpd | Delay | Latch nSET Low Q | 22 | 18 | 16 | 13 | 11 | 9 | ns |
| tpd | Delay | Latch nSET Low nQ | 19 | 21 | 14 | 15 | 9 | 10 | ns |
| tpd | Delay | Multi-Function LATCH Q | 18 | 22 | 12 | 16 | 9 | 11 | ns |
| tpd | Delay | Multi-Function LATCH nQ | 22 | 18 | 16 | 12 | 11 | 9 | ns |
| tpd | Delay | Multi-Function LATCH nRESET Q | 23 | 27 | 16 | 19 | 11 | 14 | ns |
| tpd | Delay | Multi-Function LATCH nRESET nQ | 27 | 23 | 20 | 17 | 14 | 11 | ns |
| tpd | Delay | Multi-Function LATCH nSET Q | 25 | 21 | 18 | 15 | 13 | 10 | ns |
| tpd | Delay | Multi-Function LATCH nSET nQ | 21 | 25 | 15 | 18 | 10 | 13 | ns |
| tpd | Delay | LUT2bit | 15 | 16 | 11 | 11 | 7 | 8 | ns |
| tpd | Delay | LUT3bit | 16 | 17 | 11 | 12 | 8 | 9 | ns |
| tpd | Delay | LUT4bit | 19 | 17 | 13 | 12 | 9 | 9 | ns |
| tpd | Delay | Multi-Function LUT3bit | 18 | 21 | 13 | 15 | 9 | 11 | ns |
| tpd | Delay | Multi-Function LUT3bit, CNT Delay | 48 | 47 | 33 | 34 | 24 | 24 | ns |
| tpd | Delay | Multi-Function LUT4bit | 21 | 23 | 14 | 16 | 10 | 12 | ns |
| tpd | Delay | Multi-Function LUT4bit, CNT Delay | 48 | 49 | 35 | 35 | 25 | 24 | ns |
| tpd | Delay | EDGE DETECT | 19 | 20 | 13 | 14 | 9 | 9 | ns |
| tpd | Delay | EDGE DETECT Delayed | 231 | 235 | 170 | 173 | 124 | 126 | ns |
| tpd | Width | EDGE DETECT | 211 | 212 | 156 | 157 | 115 | 115 | ns |
| tpd | Delay | Ripple CLK DOWN CNT Q0 | 18 | 16 | 13 | 11 | 9 | 8 | ns |
| tpd | Delay | Ripple CLK DOWN CNT Q1 | 29 | 22 | 20 | 16 | 14 | 11 | ns |
| tpd | Delay | Ripple CLK DOWN CNT Q2 | 27 | 29 | 20 | 21 | 14 | 14 | ns |
| tpd | Delay | Ripple CLK UP CNT Q0 | 18 | 16 | 13 | 11 | 9 | 8 | ns |
| tpd | Delay | Ripple CLK UP CNT Q1 | 24 | 24 | 17 | 17 | 12 | 12 | ns |
| tpd | Delay | Ripple CLK UP CNT Q2 | 29 | 23 | 21 | 17 | 15 | 12 | ns |
| tpd | Delay | Ripple nSET DOWN CNT Q0 | 26 | 33 | 19 | 23 | 14 | 16 | ns |
| tpd | Delay | Ripple nSET DOWN CNT Q1 | 26 | 41 | 19 | 29 | 13 | 21 | ns |
| tpd | Delay | Ripple nSET DOWN CNT Q2 | 25 | 41 | 18 | 29 | 13 | 20 | ns |
| tpd | Delay | Ripple nSET UP CNT Q0 | 26 | 33 | 19 | 23 | 14 | 16 | ns |

**Table 8: Typical Delay Estimated for Each Macrocell at T = 25 °C** (continued)

| Parameter | Description | Note | $V_{DD}$ = 2.5 V | | $V_{DD}$ = 3.3 V | | $V_{DD}$ = 5.0 V | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Rising | Falling | Rising | Falling | Rising | Falling | |
| tpd | Delay | Ripple nSET UP CNT Q1 | 26 | 38 | 19 | 27 | 13 | 19 | ns |
| tpd | Delay | Ripple nSET UP CNT Q2 | 25 | 44 | 18 | 32 | 13 | 22 | ns |
| tpd | Delay | DFF Q | 17 | 17 | 12 | 12 | 8 | 8 | ns |
| tpd | Delay | DFF nQ | 18 | 16 | 13 | 11 | 9 | 8 | ns |
| tpd | Delay | DFF nRESET High Q | -- | 20 | -- | 14 | -- | 10 | ns |
| tpd | Delay | DFF nRESET High nQ | 21 | -- | 15 | -- | 10 | -- | ns |
| tpd | Delay | DFF nRESET Low Q | -- | 22 | -- | 16 | -- | 11 | ns |
| tpd | Delay | DFF nRESET Low nQ | 23 | -- | 17 | -- | 12 | -- | ns |
| tpd | Delay | DFF nSET High Q | 21 | -- | 15 | -- | 10 | -- | ns |
| tpd | Delay | DFF nSET High nQ | -- | 20 | -- | 14 | -- | 10 | ns |
| tpd | Delay | DFF nSET Low Q | 23 | -- | 16 | -- | 12 | -- | ns |
| tpd | Delay | DFF nSET Low nQ | -- | 22 | -- | 16 | -- | 11 | ns |
| tpd | Delay | Multi-Function DFF Q | 19 | 19 | 13 | 13 | 9 | 9 | ns |
| tpd | Delay | Multi-Function DFF nQ | 20 | 19 | 14 | 13 | 9 | 9 | ns |
| tpd | Delay | Multi-Function DFF nRESET Q | -- | 26 | -- | 19 | -- | 13 | ns |
| tpd | Delay | Multi-Function DFF nRESET nQ | 26 | -- | 19 | -- | 13 | -- | ns |
| tpd | Delay | Multi-Function DFF nSET Q | 26 | -- | 19 | -- | 13 | -- | ns |
| tpd | Delay | Multi-Function DFF nSET nQ | -- | 26 | -- | 19 | -- | 14 | ns |
| tpd | Delay | PGEN CLK | 16 | 16 | 12 | 11 | 8 | 8 | ns |
| tpd | Delay | PGEN nRESET (Z to 0) | -- | 21 | -- | 15 | -- | 11 | ns |
| tpd | Delay | PGEN nRESET (Z to 1) | 20 | -- | 14 | -- | 10 | -- | ns |
| tpd | Delay | Pipe Delay Out | 23 | 23 | 16 | 16 | 11 | 11 | ns |
| tpd | Delay | Pipe Delay nRESET Out | 30 | 28 | 22 | 21 | 16 | 15 | ns |
| tpd | Delay | Filter | 160 | 159 | 108 | 108 | 68 | 68 | ns |
| tpd | Delay | ACMPxH (10 mV overdrive) | 1.44 | 1.32 | 1.47 | 1.44 | 1.66 | 1.70 | µs |
| tpd | Delay | ACMPxL (10 mV overdrive) | 53.98 | 54.56 | 61.90 | 62.96 | 76.08 | 79.53 | µs |
| tpd | Delay | ACMPxH (100 mV overdrive) | 0.77 | 0.57 | 0.63 | 0.58 | 0.64 | 0.63 | µs |
| tpd | Delay | ACMPxL (100 mV overdrive) | 21.41 | 20.27 | 25.50 | 24.38 | 32.90 | 32.38 | µs |
| tw | width | filter (min transmitted) | 143 | 143 | 99 | 99 | 62 | 62 | ns |

**Table 9: Typical Propagations Delays and Pulse Widths at T = 25 °C**

| Parameter | Description | Note | $V_{DD}$ = 2.5 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| tw | Pulse Width, 1 cell | mode:(any)edge detect, edge detect output | 214 | 159 | 116 | ns |
| tw | Pulse Width, 2 cell | mode:(any)edge detect, edge detect output | 425 | 314 | 230 | ns |
| tw | Pulse Width, 3 cell | mode:(any)edge detect, edge detect output | 635 | 469 | 343 | ns |
| tw | Pulse Width, 4 cell | mode:(any)edge detect, edge detect output | 846 | 624 | 457 | ns |
| time1 | Delay, 1 cell | mode:(any)edge detect, edge detect output | 18 | 13 | 9 | ns |
| time1 | Delay, 2 cell | mode:(any)edge detect, edge detect output | 18 | 13 | 9 | ns |
| time1 | Delay, 3 cell | mode:(any)edge detect, edge detect output | 18 | 13 | 9 | ns |

**Table 9: Typical Propagations Delays and Pulse Widths at T = 25 °C**

| Parame-ter | Description | Note | $V_{DD}$ = 2.5 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| time1 | Delay, 4 cell | mode:(any)edge detect, edge detect output | 18 | 13 | 9 | ns |
| time2 | Delay, 1 cell | mode: both edge delay, edge detect output | 235 | 173 | 126 | ns |
| time2 | Delay, 2 cell | mode: both edge delay, edge detect output | 446 | 328 | 239 | ns |
| time2 | Delay, 3 cell | mode: both edge delay, edge detect output | 656 | 484 | 353 | ns |
| time2 | Delay, 4 cell | mode: both edge delay, edge detect output | 866 | 639 | 466 | ns |

**Table 10: Typical Filter Rejection Pulse Width at T = 25 °C**

| Parameter | $V_{DD}$ = 2.5 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|
| Filtered Pulse Width | < 150 | < 55 | < 35 | ns |

## 3.5 COUNTER/DELAY SPECIFICATIONS

**Table 11: Typical Counter/Delay Offset at T = 25°C**

| Parameter | RC OSC Freq | RC OSC Power | $V_{DD}$ = 2.5 V | $V_{DD}$ = 3.3V | $V_{DD}$ = 5.0V | Unit |
|---|---|---|---|---|---|---|
| Power ON time | 25 MHz | auto | 0.13 | 0.13 | 0.13 | µs |
| Power ON time | 2.048 MHz | auto | 0.3 | 0.4 | 0.4 | µs |
| Power ON time | 2.048 kHz | auto | 660 | 570 | 480 | µs |
| frequency settling time | 25 MHz | auto | 4 | 4 | 8 | µs |
| frequency settling time | 2.048 MHz | auto | 0.3 | 0.4 | 0.4 | µs |
| frequency settling time | 2.048 kHz | auto | 660 | 570 | 480 | µs |
| variable (CLK period) | 25 MHz | forced | 0-40 | 0-40 | 0-40 | µs |
| variable (CLK period) | 2.048 MHz | forced | 0-0.5 | 0-0.5 | 0-0.5 | µs |
| variable (CLK period) | 2.048 kHz | forced | 0-488 | 0-488 | 0-488 | µs |
| tpd (non-delayed edge) | 25 MHz/ 2.048 kHz | either | 35 | 14 | 10 | ns |

## 3.6 OSC SPECIFICATIONS

**Table 12: RC Oscillators Frequency Limits, $V_{DD}$ = 2.3 V to 5.5 V**

| OSC | Temperature Range | | | | | |
|---|---|---|---|---|---|---|
| | +25 °C | | | -40 °C to +85 °C | | |
| | Minimum Value, kHz | Maximum Value, kHz | Error, % | Minimum Value, kHz | Maximum Value, kHz | Error, % |
| 2.048 kHz RC OSC0 | 2.026 | 2.071 | +1.11 | 1.911 | 2.087 | +1.90 |
| | | | -1.09 | | | -6.70 |
| 2.048 MHz RC OSC1 | 2020.37 | 2073.62 | +1.25 | 1991.16 | 2079.99 | +1.56 |
| | | | -1.35 | | | -2.78 |
| 25 MHz RC OSC2 | 24555.04 | 25393.26 | +1.57 | 23855.79 | 25587.73 | +2.35 |
| | | | -1.78 | | | -4.58 |

### 3.6.1 OSC Power-On Delay

**Table 13: Oscillators Power-On Delay at T = 25°C, RC OSC Power Setting: "Auto Power-On"**

| Power Supply Range ($V_{DD}$) V | OSC0 2.048 kHz | | OSC1 2.048 MHz | | OSC2 25 MHz | | OSC2 25 MHz Start with Delay | |
|---|---|---|---|---|---|---|---|---|
| | Typical Value, µs | Maximum Value, µs | Typical Value, ns | Maximum Value, ns | Typical Value, ns | Maximum Value, ns | Typical Value, ns | Maximum Value, ns |
| 2.30 | 676.23 | 949.81 | 513.37 | 533.00 | 30.63 | 34.00 | 126.48 | 133.00 |
| 2.50 | 641.24 | 885.92 | 497.55 | 513.00 | 27.38 | 31.00 | 126.43 | 133.00 |
| 2.70 | 613.60 | 836.51 | 482.77 | 499.00 | 24.71 | 28.00 | 126.50 | 133.00 |
| 3.00 | 581.34 | 778.36 | 466.68 | 483.00 | 21.56 | 24.00 | 126.43 | 133.00 |
| 3.30 | 556.50 | 734.34 | 454.57 | 471.00 | 19.02 | 23.00 | 126.75 | 133.00 |
| 3.60 | 536.79 | 699.90 | 444.98 | 461.00 | 17.39 | 19.00 | 127.33 | 134.00 |
| 4.00 | 515.95 | 664.30 | 434.20 | 450.00 | 15.50 | 16.00 | 127.94 | 134.00 |
| 4.20 | 507.10 | 648.67 | 429.54 | 445.00 | 14.93 | 18.00 | 128.30 | 135.00 |
| 4.50 | 495.21 | 628.37 | 423.55 | 439.00 | 14.33 | 17.00 | 129.03 | 135.00 |
| 5.00 | 476.39 | 597.31 | 415.49 | 430.00 | 13.63 | 15.00 | 130.22 | 137.00 |
| 5.50 | 454.25 | 564.14 | 408.93 | 425.00 | 13.16 | 16.00 | 131.08 | 137.00 |

### 3.7 ACMP SPECIFICATIONS

**Table 14: ACMP Specifications at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V, Unless Otherwise Noted**

| Parameter | Description | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{ACMP}$ | ACMP Input Voltage Range | Positive Input | | 0 | -- | $V_{DD}$ | V |
| | | Negative Input | | 0 | -- | $V_{DD}$ | V |
| $V_{offset}$ | ACMP Input Offset | ACMPxH Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV | | -5.9 | -- | 7.0 | mV |
| | | ACMPxL Vhys = 0 mV, Gain =1, Vref = 32 mV to 2016 mV | | -7.0 | -- | 7.0 | mV |
| $t_{start}$ | ACMP Startup Time | ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH | | -- | -- | 79 | µS |
| | | ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL | | -- | -- | 128 | µS |
| $V_{HYS}$ | Built-in Hysteresis | $V_{HYS}$ = 32 mV<br>$V_{IL}$ = Vin - $V_{HYS}$<br>$V_{IH}$ = Vin | | 20.61 | -- | 37.31 | mV |
| | | $V_{HYS}$ = 64 mV<br>$V_{IL}$ = Vin - $V_{HYS}$<br>$V_{IH}$ = Vin | | 52.48 | -- | 70.50 | mV |
| | | $V_{HYS}$ = 192 mV<br>$V_{IL}$ = Vin - $V_{HYS}$<br>$V_{IH}$ = Vin | | 178.59 | -- | 198.08 | mV |
| $R_{sin}$ | Series Input Resistance | Gain = 1x | | -- | 10 | -- | GΩ |
| | | Gain = 0.5x | | -- | 1.6 | -- | MΩ |
| | | Gain = 0.33x | | -- | 1.6 | -- | MΩ |
| | | Gain = 0.25x | | -- | 1.6 | -- | MΩ |
| PROP | Propagation Delay, Response Time | ACMPxH, Vref = 1.024 V, Gain = 1, Overdrive = 100 mV | Low to High | -- | 0.67 | 2.27 | µS |
| | | | High to Low | -- | 0.57 | 0.80 | µS |
| | | ACMPxH, Vref = 32 mV to 2016 mV, Gain = 1, Overdrive = 100 mV | Low to High | -- | 0.71 | 2.27 | µS |
| | | | High to Low | -- | 0.63 | 1.01 | µS |
| | | ACMPxL, Vref=1.024 V, Gain = 1, Overdrive = 100 mV | Low to High | -- | 16.63 | 33.18 | µS |
| | | | High to Low | -- | 16.47 | 33.62 | µS |
| | | ACMPxL, Vref = 32 mV to 2016 mV, Gain = 1, Overdrive = 100 mV | Low to High | -- | 27.10 | 58.65 | µS |
| | | | High to Low | -- | 27.87 | 59.81 | µS |

**Table 14: ACMP Specifications at T = -40 °C to +85 °C, $V_{DD}$ = 2.3 V to 5.5 V, Unless Otherwise Noted** (continued)

| Parameter | Description | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| G | Gain error | G = 1 | | 1 | 1 | 1 | |
| | | G = 0.5 | | 0.496 | 0.5 | 0.504 | |
| | | G = 0.33 | | 0.330 | 0.33 | 0.338 | |
| | | G = 0.25 | | 0.247 | 0.25 | 0.254 | |
| Vref0 | Vref0 Output Capacitance Loading | | Resistance Load = 1 MΩ | -- | -- | 5 | pF |
| | | | Resistance Load = 560 kΩ | -- | -- | 10 | pF |
| | | | Resistance Load = 100 kΩ | -- | -- | 40 | pF |
| | | | Resistance Load = 10 kΩ | -- | -- | 80 | pF |
| | | | Resistance Load = 2 kΩ | -- | -- | 120 | pF |
| | | | Resistance Load = 1 kΩ, Vref = 32 mV to 1024 mV | -- | -- | 150 | pF |
| | | | | | | | |
| Vref1 | Vref1 Output Capacitance Loading | | Resistance Load = 1 MΩ | -- | -- | 15 | pF |
| | | | Resistance Load = 560 kΩ | -- | -- | 27 | pF |
| | | | Resistance Load = 100 kΩ | -- | -- | 64 | pF |
| | | | Resistance Load = 10 kΩ | -- | -- | 120 | pF |
| | | | Resistance Load = 2 kΩ | -- | -- | 180 | pF |
| | | | Resistance Load = 1 kΩ, Vref = 32 mV to 1024 mV | -- | -- | 210 | pF |

### 3.8 ANALOG TEMPERATURE SENSOR (TS) SPECIFICATIONS

**Table 15: TS Output vs Temperature (Output Range 1)**

| T, °C | $V_{DD}$ = 2.5 V | | $V_{DD}$ = 3.3 V | | $V_{DD}$ = 5.0 V | |
|---|---|---|---|---|---|---|
| | Typical, mV | Accuracy, % | Typical, mV | Accuracy, % | Typical, mV | Accuracy, % |
| -40 | 998 | ±0.67 | 997 | ±0.67 | 997 | ±0.70 |
| -30 | 975 | ±0.59 | 974 | ±0.58 | 974 | ±0.58 |
| -20 | 952 | ±0.54 | 952 | ±0.52 | 951 | ±0.52 |
| -10 | 930 | ±0.65 | 929 | ±0.63 | 929 | ±0.62 |
| 0 | 907 | ±0.69 | 906 | ±0.69 | 906 | ±0.65 |
| 10 | 884 | ±0.79 | 883 | ±0.77 | 883 | ±0.75 |
| 20 | 861 | ±0.82 | 860 | ±0.80 | 859 | ±0.78 |
| 30 | 837 | ±0.93 | 836 | ±0.89 | 836 | ±0.86 |
| 40 | 813 | ±0.89 | 813 | ±0.85 | 812 | ±0.81 |
| 50 | 789 | ±1.01 | 789 | ±0.97 | 788 | ±0.92 |
| 60 | 765 | ±1.13 | 764 | ±1.09 | 764 | ±1.05 |
| 70 | 741 | ±1.24 | 740 | ±1.21 | 740 | ±1.16 |
| 80 | 717 | ±1.36 | 716 | ±1.33 | 715 | ±1.29 |
| 85 | 704 | ±1.48 | 703 | ±1.45 | 703 | ±1.42 |

**Table 16: TS Output vs Temperature (Output Range 2)**

| T, °C | $V_{DD}$ = 2.5 V | | $V_{DD}$ = 3.3 V | | $V_{DD}$ = 5.0 V | |
|---|---|---|---|---|---|---|
| | Typical, mV | Accuracy, % | Typical, mV | Accuracy, % | Typical, mV | Accuracy, % |
| -40 | 1189 | ±0.70 | 1188 | ±0.69 | 1188 | ±0.69 |
| -30 | 1161 | ±0.58 | 1161 | ±0.57 | 1160 | ±0.59 |
| -20 | 1134 | ±0.62 | 1133 | ±0.62 | 1133 | ±0.64 |
| -10 | 1107 | ±0.69 | 1106 | ±0.68 | 1106 | ±0.68 |
| 0 | 1079 | ±0.72 | 1078 | ±0.71 | 1078 | ±0.71 |
| 10 | 1051 | ±0.80 | 1051 | ±0.79 | 1050 | ±0.80 |
| 20 | 1023 | ±0.87 | 1022 | ±0.85 | 1022 | ±0.86 |
| 30 | 995 | ±0.97 | 994 | ±0.96 | 994 | ±0.95 |
| 40 | 966 | ±0.91 | 965 | ±0.88 | 965 | ±0.86 |
| 50 | 937 | ±1.00 | 936 | ±1.01 | 936 | ±0.99 |
| 60 | 908 | ±1.14 | 907 | ±1.12 | 907 | ±1.10 |
| 70 | 879 | ±1.24 | 878 | ±1.22 | 878 | ±1.20 |
| 80 | 849 | ±1.40 | 848 | ±1.38 | 848 | ±1.37 |
| 85 | 835 | ±1.50 | 834 | ±1.48 | 833 | ±1.45 |

**Table 17: TS Output Error (Output Range 1)**

| $V_{DD}$, V | Error at T | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | -40°C, % | -20°C, % | 0°C, % | 20°C, % | 40°C, % | 60°C, % | 80°C, % | 85°C, % |
| 2.30 | ±0.67 | ±0.55 | ±0.69 | ±0.82 | ±0.90 | ±1.14 | ±1.37 | ±1.50 |
| 2.50 | ±0.67 | ±0.54 | ±0.69 | ±0.82 | ±0.89 | ±1.13 | ±1.36 | ±1.49 |
| 2.70 | ±0.68 | ±0.53 | ±0.68 | ±0.81 | ±0.88 | ±1.11 | ±1.35 | ±1.48 |
| 3.00 | ±0.67 | ±0.52 | ±0.67 | ±0.80 | ±0.86 | ±1.10 | ±1.34 | ±1.45 |
| 3.30 | ±0.67 | ±0.52 | ±0.67 | ±0.80 | ±0.85 | ±1.09 | ±1.33 | ±1.45 |
| 3.60 | ±0.68 | ±0.52 | ±0.66 | ±0.79 | ±0.84 | ±1.07 | ±1.32 | ±1.44 |
| 4.20 | ±0.68 | ±0.52 | ±0.66 | ±0.78 | ±0.83 | ±1.06 | ±1.30 | ±1.43 |
| 4.50 | ±0.69 | ±0.52 | ±0.65 | ±0.78 | ±0.82 | ±1.05 | ±1.30 | ±1.43 |
| 5.00 | ±0.70 | ±0.52 | ±0.65 | ±0.78 | ±0.81 | ±1.05 | ±1.30 | ±1.42 |
| 5.50 | ±0.71 | ±0.54 | ±0.66 | ±0.79 | ±0.81 | ±1.05 | ±1.29 | ±1.40 |

**Table 18: TS Output Error (Output Range 2)**

| $V_{DD}$, V | Error at T | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | -40°C, % | -20°C, % | 0°C, % | 20°C, % | 40°C, % | 60°C, % | 80°C, % | 85°C, % |
| 2.30 | ±0.67 | ±0.61 | ±0.73 | ±0.87 | ±0.92 | ±1.15 | ±1.41 | ±1.50 |
| 2.50 | ±0.67 | ±0.62 | ±0.72 | ±0.87 | ±0.91 | ±1.14 | ±1.40 | ±1.50 |
| 2.70 | ±0.67 | ±0.61 | ±0.72 | ±0.86 | ±0.90 | ±1.14 | ±1.40 | ±1.49 |
| 3.00 | ±0.67 | ±0.61 | ±0.71 | ±0.85 | ±0.89 | ±1.13 | ±1.39 | ±1.48 |
| 3.30 | ±0.67 | ±0.62 | ±0.71 | ±0.85 | ±0.88 | ±1.12 | ±1.39 | ±1.48 |
| 3.60 | ±0.67 | ±0.61 | ±0.71 | ±0.85 | ±0.88 | ±1.11 | ±1.38 | ±1.47 |
| 4.20 | ±0.67 | ±0.63 | ±0.71 | ±0.85 | ±0.87 | ±1.10 | ±1.37 | ±1.46 |
| 4.50 | ±0.68 | ±0.63 | ±0.71 | ±0.85 | ±0.87 | ±1.11 | ±1.37 | ±1.46 |
| 5.00 | ±0.69 | ±0.64 | ±0.71 | ±0.86 | ±0.86 | ±1.10 | ±1.37 | ±1.45 |
| 5.50 | ±0.71 | ±0.65 | ±0.72 | ±0.86 | ±0.87 | ±1.11 | ±1.35 | ±1.44 |

### 3.9 POWER SWITCH ELECTRICAL CHARACTERISTICS (EACH P-FET)

**Table 19: Power Switch EC $T_A$ = -40°C to +85°C (Typical Values at $T_A$ = +25°C), $V_{DD}$ = 5.5 V Unless Otherwise Noted**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance | $T_A$ = +25°C, $V_{GS}$ = -5.5 V, $I_D$ = -100 mA **(Note 1)** | -- | 44 | 50 | mΩ |
| | | $T_A$ = +25°C, $V_{GS}$ = -3.3 V, $I_D$ = -100 mA **(Note 1)** | -- | 58 | 65 | |
| | | $T_A$ = +25°C, $V_{GS}$ = -1.71 V, $I_D$ = -100 mA **(Note 1)** | -- | 110 | 119 | |
| | | $T_A$ = +85°C, $V_{GS}$ = -5.5 V, $I_D$ = -100 mA **(Note 1)** | -- | 51 | 58 | |
| | | $T_A$ = +85°C, $V_{GS}$ = -3.3 V, $I_D$ = -100 mA **(Note 1)** | -- | 69 | 77 | |
| | | $T_A$ = +85°C, $V_{GS}$ = -1.71 V, $I_D$ = -100 mA **(Note 1)** | -- | 129 | 138 | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -1 mA | -0.48 | -0.61 | -0.72 | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $T_A$ = +25°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = 0 V **(Note 2)** | -- | -- | 0.4 | µA |
| | | $T_A$ = +85°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = 0 V | -- | -- | 3.4 | |
| $I_{GSS}$ | Gate-Body Leakage | $T_A$ = +25°C, $V_{GS}$ = ±5.5 V **(Note 2)** | -- | ±5 | ±100 | nA |
| | | $T_A$ = +85°C, $V_{GS}$ = ±5.5 V | -- | ±400 | ±2000 | |
| $G_m$ | Forward Transconductance | $V_{DS}$ = -5.5 V, $V_{GS}$ = -1.8 V, $I_D$ = -2 A **(Note 1)** | 4.5 | 5.4 | -- | S |
| **Dynamic** | | | | | | |
| $R_G$ | Internal Gate Resistance | | -- | 200 | -- | Ω |
| $C_{iss}$ | Input Capacitance | $T_A$ = +25°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = 0 V, $f$ = 1.0 MHz **(Note 3)** | -- | 207 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 122 | -- | |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 57 | -- | |
| $Q_g$ | Total Gate Charge | $T_A$ = +25°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = -5.5 V, $I_D$ = -2 A **(Note 1)** | -- | 1.45 | 1.55 | nC |
| $Q_{gs}$ | Gate-to-Source Charge | | -- | 0.24 | -- | |
| $Q_{gd}$ | Gate-to-Drain Charge | | -- | 0.24 | -- | |
| $t_{on}$ | Turn-On Time | $T_A$ = +25°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = 0 V to -5.5 V, ID = -1 A, Internal Drive | -- | 63 | -- | ns |
| $t_{off}$ | Turn-Off Delay Time | $T_A$ = +25°C, $V_{DS}$ = -5.5 V, $V_{GS}$ = 0 V to -5.5 V, ID = -1 A, Internal Drive | -- | 287 | -- | ns |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | $T_A$ = +25°C, single channel operation | -- | -- | -2 | A |
| $V_{DSF}$ | Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 100 mA **(Note 1)** | 0.63 | 0.75 | 0.87 | V |

**Note 1** Pulse test: $f$ = 100 Hz, Duty cycle < 2%.
**Note 2** Measured to be less than 0.4 µA during production test.
**Note 3** RG influence has been excluded.

## 4 User Programmability

The SLG46867 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Dialog Semiconductor to integrate into a production process.

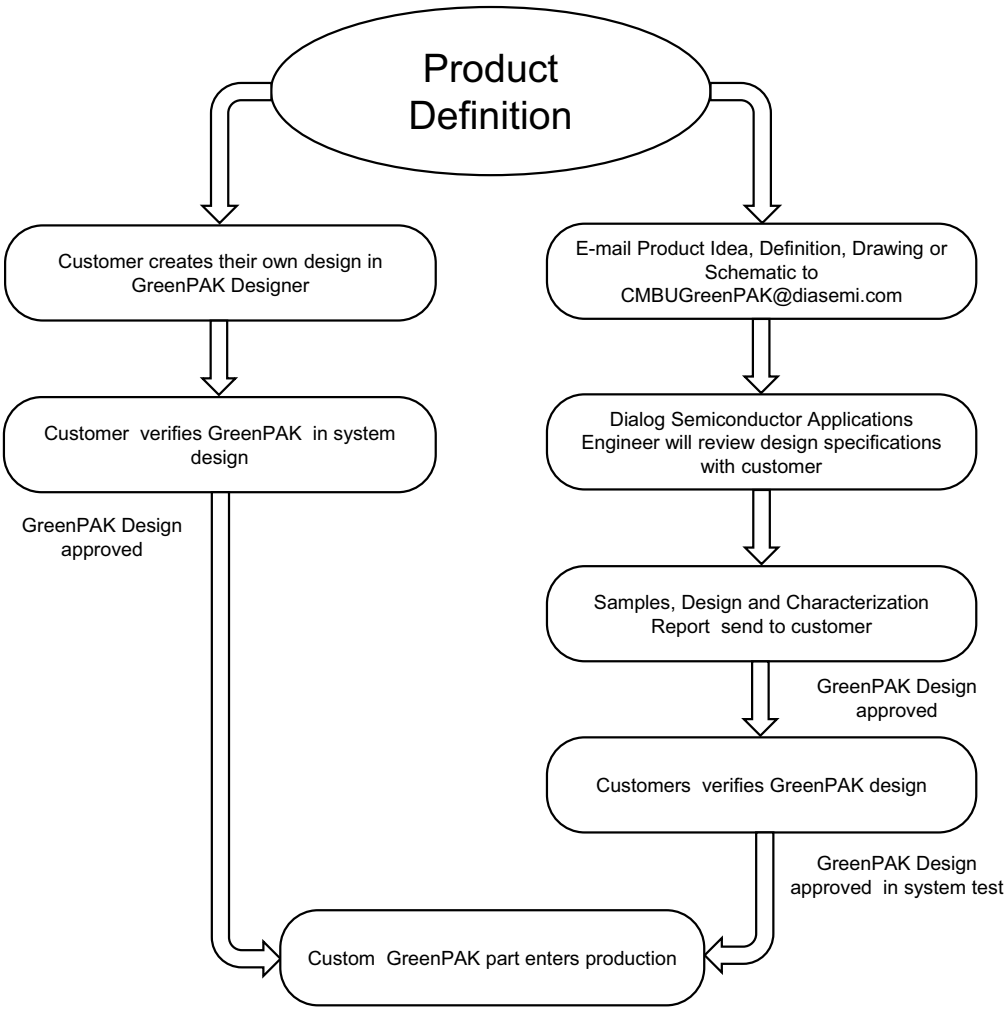



**Figure 2: Steps to Create a Custom GreenPAK Device**

# 5 IO Pins

The SLG46867 has a total of 10 GPIO, 1 GPI, and 1 GPO Pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

## 5.1 GPIO PINS

GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, and GPIO9 serve as General Purpose IO Pins.

## 5.2 GPI PINS

GPI0 serves as a General Purpose Input Pin.

## 5.3 GPO PINS

GPO0 serves as a General Purpose Output Pin.

## 5.4 PULL UP/DOWN RESISTORS

All IO Pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

## 5.5 FAST PULL-UP/DOWN DURING POWER UP

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [778].

## 5.6 GPI STRUCTURE

### 5.6.1 GPI Structure (for GPI0)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en=1, OE=0
01: Digital In with Schmitt Trigger, smt_en=1, OE=0
10: Low Voltage Digital In mode, lv_en = 1, OE=0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

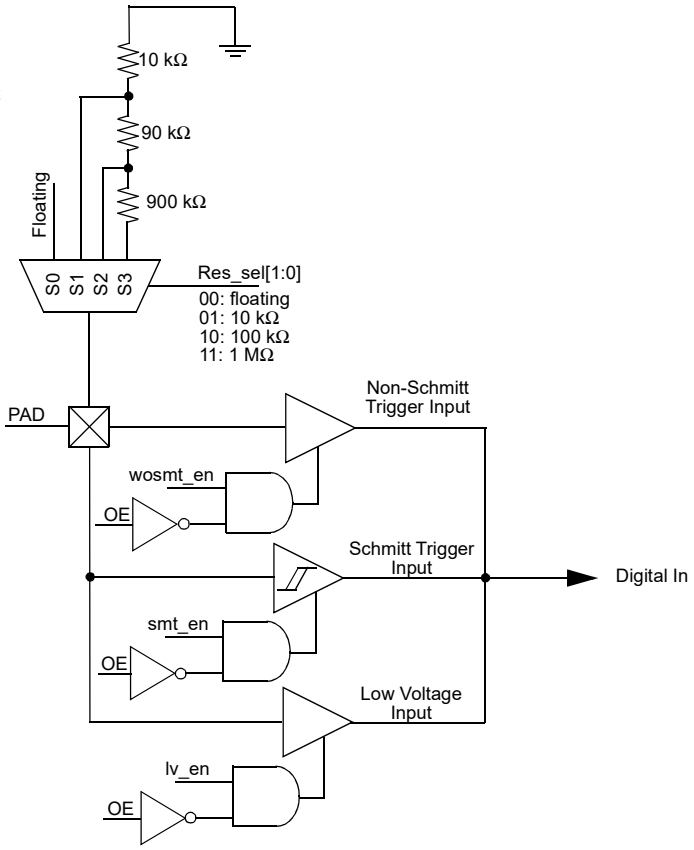



**Figure 3: IO0 GPI Structure Diagram**

## 5.7 GPIO WITH I²C MODE IO STRUCTURE

### 5.7.1 GPIO with I²C Mode Structure (for GPIO0 and GPIO1)

IO6, IO7 Mode [2:0]
000: Digital Input without Schmitt Trigger
001: Digital Input with Schmitt Trigger
010: Low Voltage Digital Input
011: Reserved
100: Reserved
101: Open Drain NMOS
110: Reserved
111: Reserved

Note 1: OE cannot be selected by user and is controlled by register. Digital In is Matrix input.
Note 2: GPIO0 and GPIO1 do not support Push Pull and PMOS Open drain modes.
Note 3: It is possible to apply an input voltage higher than VDD to GPIO0 and GPIO1. However, this voltage should not exceed 5.5 V.

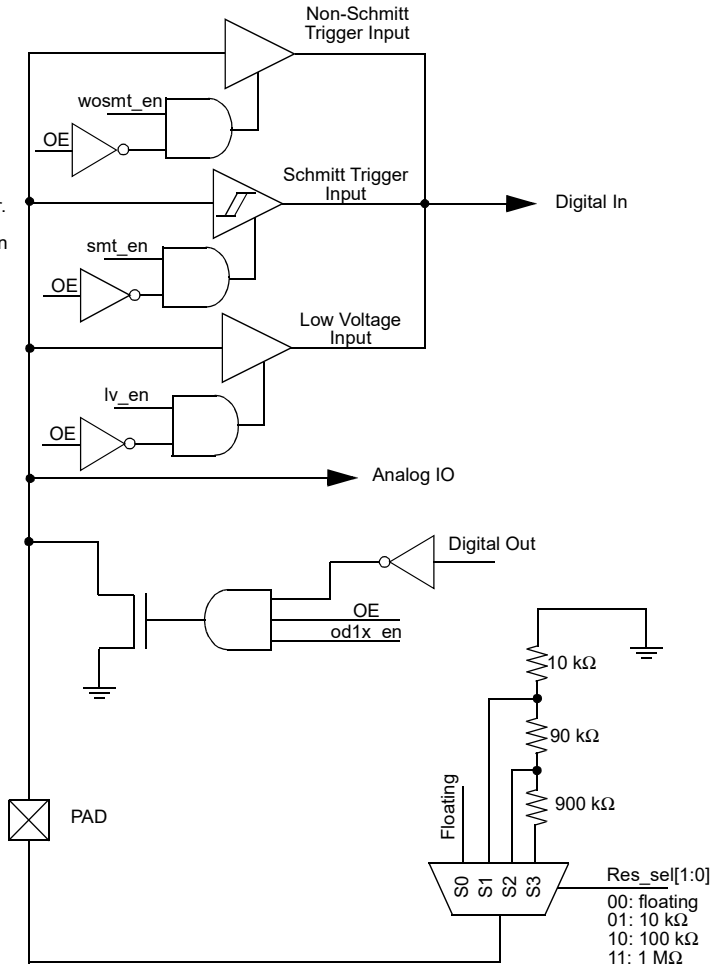



**Figure 4: GPIO with I²C Mode IO Structure Diagram**

### 5.8 MATRIX OE IO STRUCTURE

#### 5.8.1 Matrix OE IO Structure (for GPIO2, GPIO3, GPIO5, GPIO6. GPIO7, GPIO8, and GPIO9)

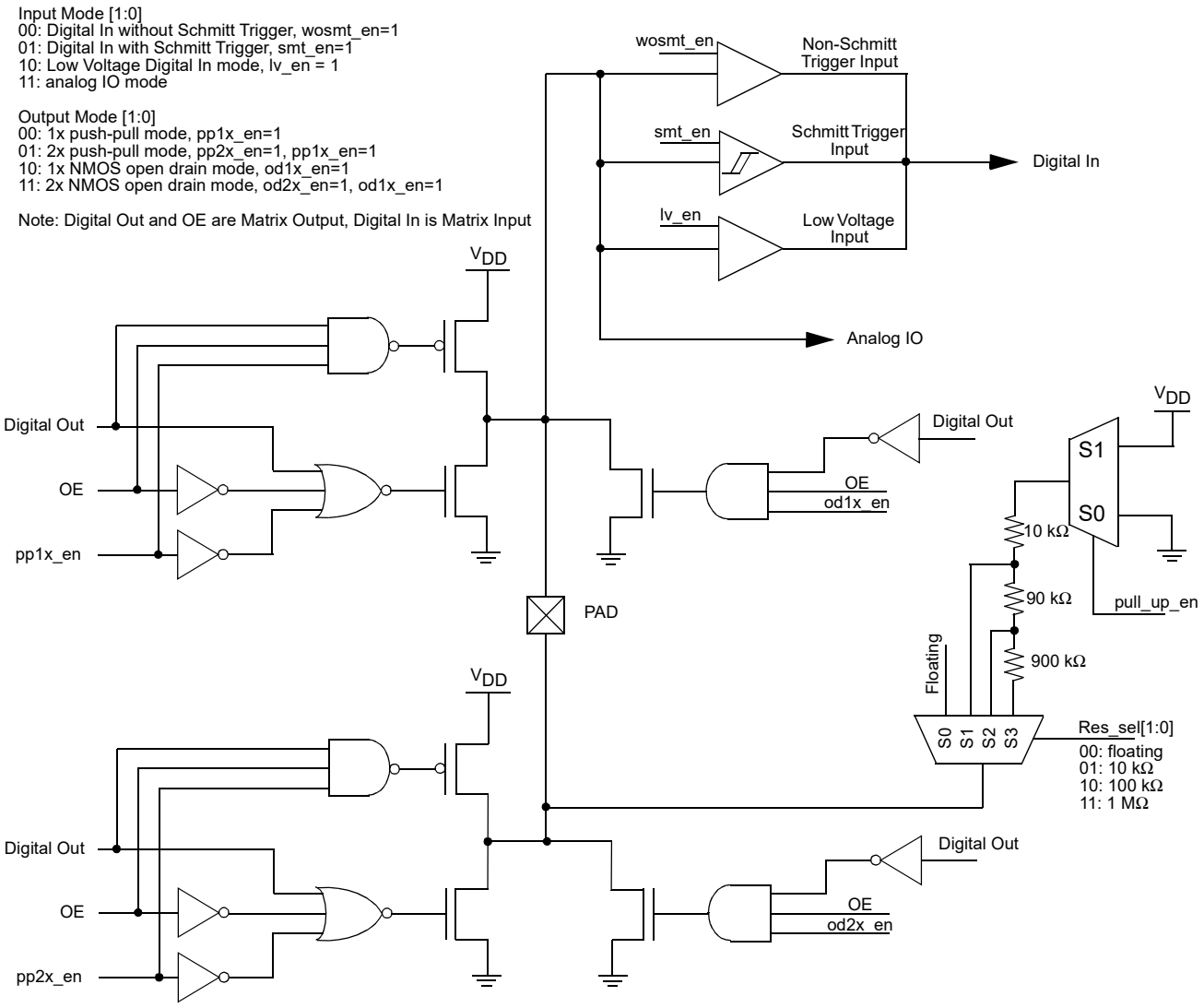



**Figure 5: Matrix OE IO Structure Diagram**

### 5.8.2 Matrix OE 4X Drive Structure (for GPIO4)

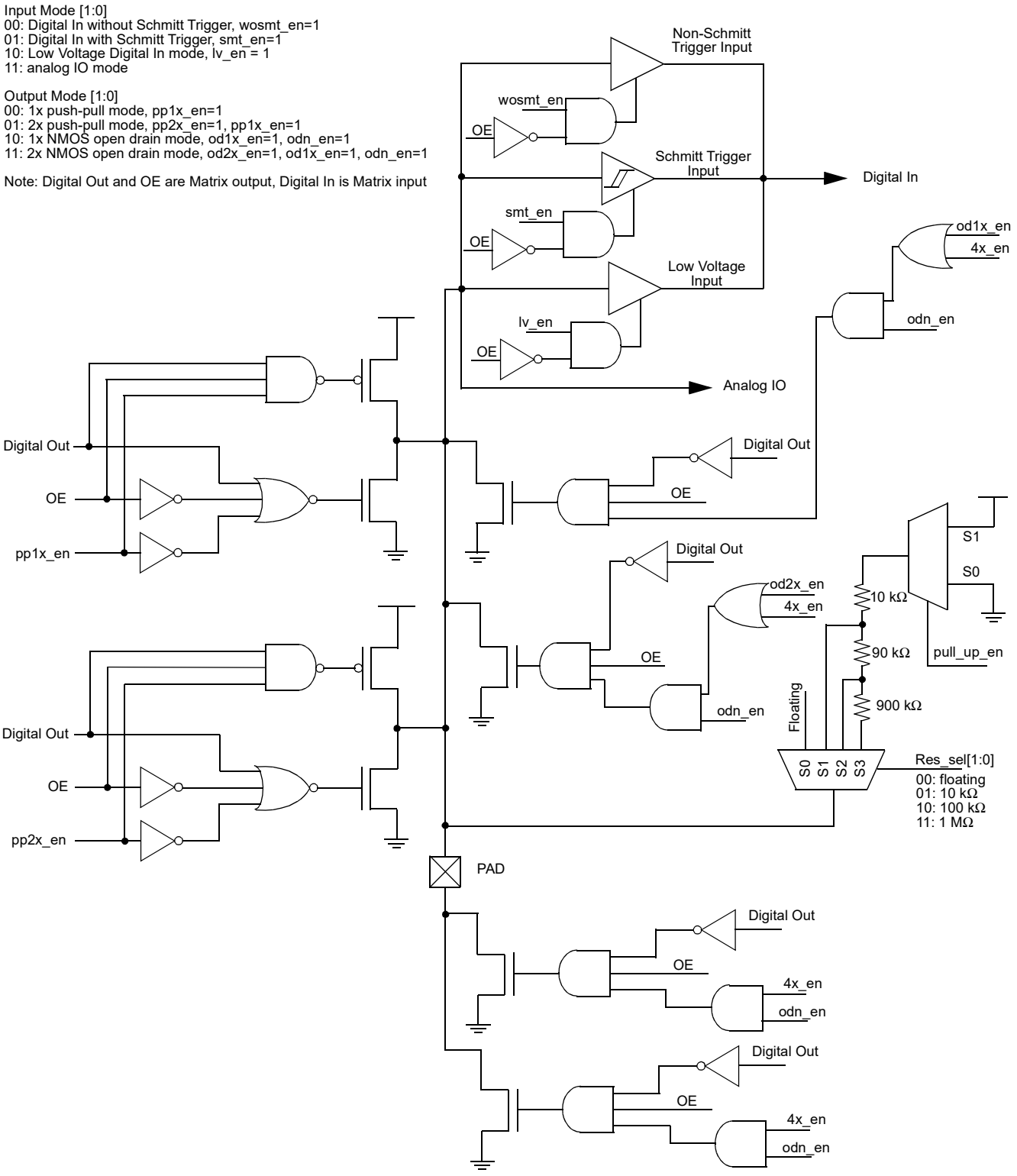



**Figure 6. Matrix OE IO 4X Drive Structure Diagram**

## 5.9 GPO STRUCTURE

### 5.9.1 GPO Register OE Structure (for GPO0)

Output Mode [1:0]
00: 1x push-pull mode, pp1x_en=1
01: 2x push-pull mode, pp2x_en=1, pp1x_en=1
10: 1x NMOS open drain mode, od1x_en=1
11: 2x NMOS open drain mode, od2x_en=1, od1x_en=1

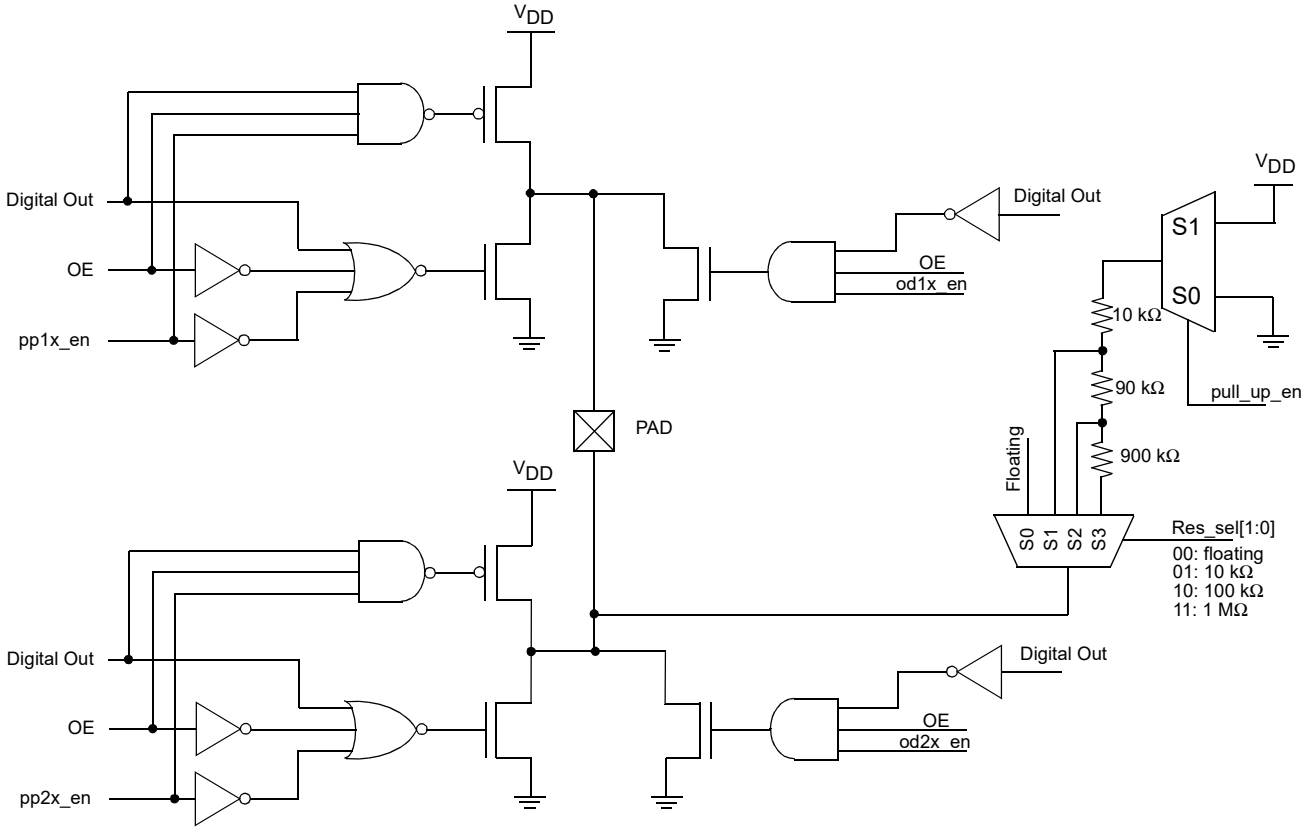



**Figure 7: GPO Register OE Structure Diagram**

# 6 Connection Matrix

The Connection Matrix in the SLG46867 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46867 has a specific digital bit code assigned to it that is either set to active "High" or inactive "Low" based on the design that is created. Once the 2048 register bits within the SLG46867 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources and $V_{DD}$ and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46867's register table, see Section 18.

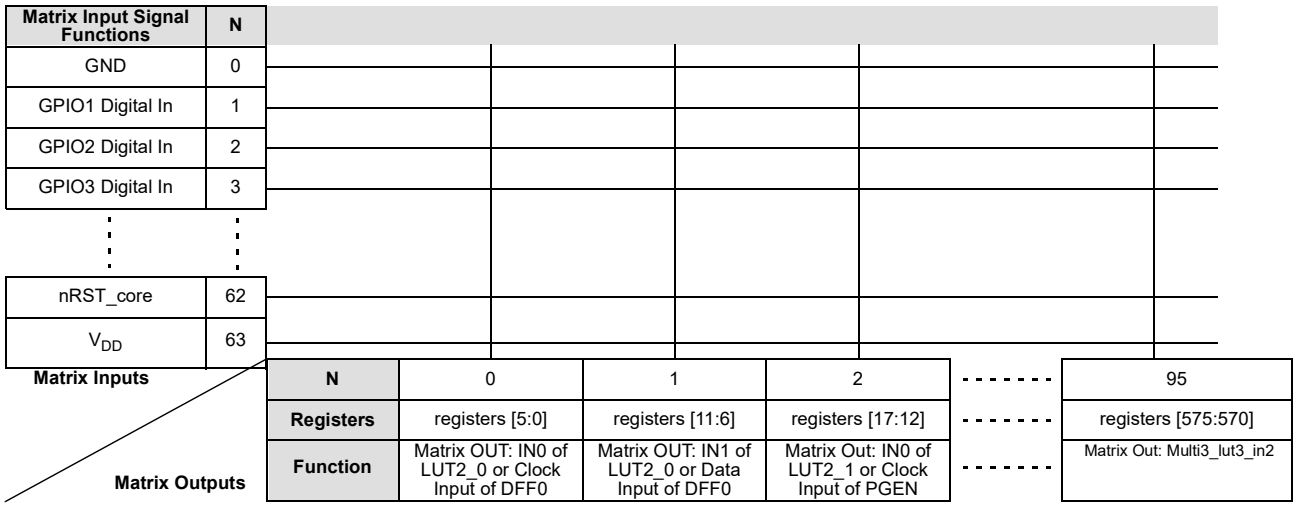



**Figure 8: Connection Matrix**

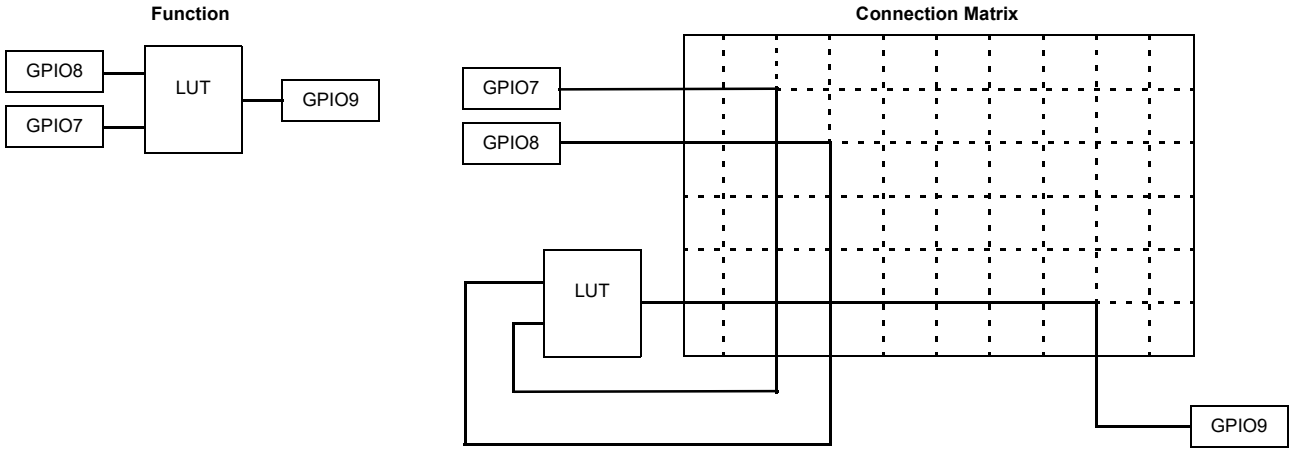



**Figure 9: Connection Matrix Example**

### 6.1 MATRIX INPUT TABLE

**Table 20: Matrix Input Table**

| Matrix Input Number | Matrix Input Signal Function | Matrix Decode | | | | | |
|---|---|---|---|---|---|---|---|
| | | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | GND | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | LUT2_0/DFF0 output | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | LUT2_1/DFF1 output | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | LUT2_2/DFF2 output | 0 | 0 | 0 | 0 | 1 | 1 |
| 4 | LUT2_3/PGEN output | 0 | 0 | 0 | 1 | 0 | 0 |
| 5 | LUT3_0/DFF3 output | 0 | 0 | 0 | 1 | 0 | 1 |
| 6 | LUT3_1/DFF4 output | 0 | 0 | 0 | 1 | 1 | 0 |
| 7 | LUT3_2/DFF5 output | 0 | 0 | 0 | 1 | 1 | 1 |
| 8 | LUT3_3/DFF6 output | 0 | 0 | 1 | 0 | 0 | 0 |
| 9 | LUT3_4/DFF7 output | 0 | 0 | 1 | 0 | 0 | 1 |
| 10 | LUT3_5/DFF8 output | 0 | 0 | 1 | 0 | 1 | 0 |
| 11 | LUT3_6/DFF9 output | 0 | 0 | 1 | 0 | 1 | 1 |
| 12 | LUT3_7/DFF10 output | 0 | 0 | 1 | 1 | 0 | 0 |
| 13 | LUT3_8/DFF11 output | 0 | 0 | 1 | 1 | 0 | 1 |
| 14 | CNT0 output | 0 | 0 | 1 | 1 | 1 | 0 |
| 15 | MLT0_LUT4/DFF_OUT | 0 | 0 | 1 | 1 | 1 | 1 |
| 16 | CNT1 output | 0 | 1 | 0 | 0 | 0 | 0 |
| 17 | MLT1_LUT3/DFF_OUT | 0 | 1 | 0 | 0 | 0 | 1 |
| 18 | CNT2 output | 0 | 1 | 0 | 0 | 1 | 0 |
| 19 | MLT2_LUT3/DFF_OUT | 0 | 1 | 0 | 0 | 1 | 1 |
| 20 | CNT3 output | 0 | 1 | 0 | 1 | 0 | 0 |
| 21 | MLT3_LUT3/DFF_OUT | 0 | 1 | 0 | 1 | 0 | 1 |
| 22 | CNT4 output | 0 | 1 | 0 | 1 | 1 | 0 |
| 23 | MLT4_LUT3/DFF_OUT | 0 | 1 | 0 | 1 | 1 | 1 |
| 24 | CNT5 output | 0 | 1 | 1 | 0 | 0 | 0 |
| 25 | MLT5_LUT3/DFF_OUT | 0 | 1 | 1 | 0 | 0 | 1 |
| 26 | CNT6 output | 0 | 1 | 1 | 0 | 1 | 0 |
| 27 | MLT6_LUT3/DFF_OUT | 0 | 1 | 1 | 0 | 1 | 1 |
| 28 | CNT7 output | 0 | 1 | 1 | 1 | 0 | 0 |
| 29 | MLT7_LUT3/DFF_OUT | 0 | 1 | 1 | 1 | 0 | 1 |
| 30 | LUT3_16/Ripple CNT/Pipe Delay_out0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 31 | Ripple CNT/Pipe Delay_out1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 32 | GPIO0 digital input or $I^2C$_virtual_0 Input | 1 | 0 | 0 | 0 | 0 | 0 |
| 33 | GPIO1 digital input or $I^2C$_virtual_1 Input | 1 | 0 | 0 | 0 | 0 | 1 |
| 34 | $I^2C$_virtual_2 Input | 1 | 0 | 0 | 0 | 1 | 0 |
| 35 | $I^2C$_virtual_3 Input | 1 | 0 | 0 | 0 | 1 | 1 |
| 36 | $I^2C$_virtual_4 Input | 1 | 0 | 0 | 1 | 0 | 0 |
| 37 | $I^2C$_virtual_5 Input | 1 | 0 | 0 | 1 | 0 | 1 |

**Table 20: Matrix Input Table** (continued)

| Matrix Input Number | Matrix Input Signal Function | Matrix Decode | | | | | |
|---|---|---|---|---|---|---|---|
| | | 5 | 4 | 3 | 2 | 1 | 0 |
| 38 | $I^2C$_virtual_6 Input | 1 | 0 | 0 | 1 | 1 | 0 |
| 39 | $I^2C$_virtual_7 Input | 1 | 0 | 0 | 1 | 1 | 1 |
| 40 | Tipple CNT_out2 | 1 | 0 | 1 | 0 | 0 | 0 |
| 41 | LUT4_0/DFF12 output | 1 | 0 | 1 | 0 | 0 | 1 |
| 42 | Programmable Delay Edge Detect Output | 1 | 0 | 1 | 0 | 1 | 0 |
| 43 | Edge Detect Filter Output | 1 | 0 | 1 | 0 | 1 | 1 |
| 44 | GPI0 Digital Input | 1 | 0 | 1 | 1 | 0 | 0 |
| 45 | GPIO2 Digital Input | 1 | 0 | 1 | 1 | 0 | 1 |
| 46 | Power Switch ON0, Digital Input | 1 | 0 | 1 | 1 | 1 | 0 |
| 47 | GPIO4 Digital Input | 1 | 0 | 1 | 1 | 1 | 1 |
| 48 | GPIO5 Digital Input | 1 | 1 | 0 | 0 | 0 | 0 |
| 49 | GPIO6 Digital Input | 1 | 1 | 0 | 0 | 0 | 1 |
| 50 | GPIO7 Digital Input | 1 | 1 | 0 | 0 | 1 | 0 |
| 51 | GPIO8 Digital Input | 1 | 1 | 0 | 0 | 1 | 1 |
| 52 | GPIO9 Digital Input | 1 | 1 | 0 | 1 | 0 | 0 |
| 53 | Oscillator0 output 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 54 | Oscillator1 output 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 55 | Oscillator2 output | 1 | 1 | 0 | 1 | 1 | 1 |
| 56 | ACMP0H Output (normal speed) | 1 | 1 | 1 | 0 | 0 | 0 |
| 57 | ACMP1H Output (normal speed) | 1 | 1 | 1 | 0 | 0 | 1 |
| 58 | ACMP0L Output (low speed) | 1 | 1 | 1 | 0 | 1 | 0 |
| 59 | ACMP1L output (low speed) | 1 | 1 | 1 | 0 | 1 | 1 |
| 60 | Oscillator0 output 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 61 | Oscillator1 output 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 62 | Matrix nRST | 1 | 1 | 1 | 1 | 1 | 0 |
| 63 | $V_{DD}$ | 1 | 1 | 1 | 1 | 1 | 1 |

## 6.2 MATRIX OUTPUT TABLE

**Table 21: Matrix Output Table**

| Register Bit Address | Matrix Output Signal Function | Matrix Output Number |
|---|---|---|
| [5:0] | IN0 of LUT2_0 or Clock Input of DFF0 | 0 |
| [11:6] | IN1 of LUT2_0 or Data Input of DFF0 | 1 |
| [17:12] | IN0 of LUT2_1 or Clock Input of DFF1 | 2 |
| [23:18] | IN1 of LUT2_1 or Data Input of DFF1 | 3 |
| [29:24] | IN0 of LUT2_2 or Clock Input of DFF2 | 4 |
| [35:30] | IN1 of LUT2_2 or Data Input of DFF2 | 5 |
| [41:36] | IN0 of LUT2_3 or Clock Input of PGEN | 6 |
| [47:42] | IN1 of LUT2_3 or nRST of PGEN | 7 |
| [53:48] | IN0 of LUT3_0 or CLK Input of DFF3 | 8 |
| [59:54] | IN1 of LUT3_0 or Data of DFF3 | 9 |
| [65:60] | IN2 of LUT3_0 or nRST (nSET) of DFF3 | 10 |
| [71:66] | IN0 of LUT3_1 or CLK Input of DFF4 | 11 |
| [77:72] | IN1 of LUT3_1 or Data of DFF4 | 12 |
| [83:78] | IN2 of LUT3_1 or nRST (nSET) of DFF4 | 13 |
| [89:84] | IN0 of LUT3_2 or CLK Input of DFF5 | 14 |
| [95:90] | IN1 of LUT3_2 or Data of DFF5 | 15 |
| [101:96] | IN2 of LUT3_2 or nRST (nSET) of DFF5 | 16 |
| [107:102] | IN0 of LUT3_3 or CLK Input of DFF6 | 17 |
| [113:108] | IN1 of LUT3_3 or Data of DFF6 | 18 |
| [119:114] | IN2 of LUT3_3 or nRST (nSET) of DFF6 | 19 |
| [125:120] | IN0 of LUT3_4 or CLK Input of DFF7 | 20 |
| [131:126] | IN1 of LUT3_4 or Data of DFF7 | 21 |
| [137:132] | IN1 of LUT3_4 or Data of DFF7 | 22 |
| [143:138] | IN0 of LUT3_5 or CLK Input of DFF8 | 23 |
| [149:144] | IN1 of LUT3_5 or Data of DFF8 | 24 |
| [155:150] | IN2 of LUT3_5 or nRST (nSET) of DFF8 | 25 |
| [161:156] | IN0 of LUT3_6 or CLK Input of DFF9 | 26 |
| [167:162] | IN1 of LUT3_6 or Data of DFF9 | 27 |
| [173:168] | IN2 of LUT3_6 or nRST (nSET) of DFF9 | 28 |
| [179:174] | IN0 of LUT3_7 or CLK Input of DFF10 | 29 |
| [185:180] | IN1 of LUT3_7 or Data of DFF10 | 30 |
| [191:186] | IN2 of LUT3_7 or nRST (nSET) of DFF10 | 31 |
| [197:192] | IN0 of LUT3_8 or CLK Input of DFF11 | 32 |
| [203:198] | IN0 of LUT3_8 or CLK Input of DFF11 | 33 |
| [209:204] | IN2 of LUT3_8 or nRST (nSET) of DFF11 | 34 |
| [215:210] | IN0 of LUT3_12 or CLK Input of DFF16<br>Delay4 Input (or Counter4 nRST Input) | 35 |
| [221:216] | IN1 of LUT3_12 or nRST (nSET) of DFF16<br>Delay4 Input (or Counter4 nRST Input) | 36 |

**Table 21: Matrix Output Table** (continued)

| Register Bit Address | Matrix Output Signal Function | Matrix Output Number |
|---|---|---|
| [227:222] | IN2 of LUT3_12 or Data of DFF16<br>Delay4 Input (or Counter4 nRST Input) | 37 |
| [233:228] | IN0 of LUT3_13 or CLK Input of DFF17<br>Delay5 Input (or Counter5 nRST Input) | 38 |
| [239:234] | IN1 of LUT3_13 or nRST (nSET) of DFF17<br>Delay5 Input (or Counter5 nRST Input) | 39 |
| [245:240] | IN2 of LUT3_13 or Data of DFF17<br>Delay5 Input (or Counter5 nRST Input) | 40 |
| [251:246] | IN0 of LUT3_14 or CLK Input of DFF18<br>Delay6 Input (or Counter6 nRST Input) | 41 |
| [257:252] | IN1 of LUT3_14 or nRST (nSET) of DFF18<br>Delay6 Input (or Counter6 nRST Input) | 42 |
| [263:258] | IN2 of LUT3_14 or Data of DFF18<br>Delay6 Input (or Counter6 nRST Input) | 43 |
| [269:264] | IN0 of LUT3_15 or CLK Input of DFF19<br>Delay7 Input (or Counter7 nRST Input) | 44 |
| [275:270] | IN1 of LUT3_15 or nRST (nSET) of DFF19<br>Delay7 Input (or Counter7 nRST Input) | 45 |
| [281:276] | IN2 of LUT3_15 or Data of DFF19<br>Delay7 Input (or Counter7 nRST Input) | 46 |
| [287:282] | IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT | 47 |
| [293:288] | IN1 of LUT3_16 or nRST of Pipe Delay or STB of RIPP CNT | 48 |
| [299:294] | IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT | 49 |
| [305:300] | IN0 of LUT4_0 or CLK Input of DFF12 | 50 |
| [311:306] | IN1 of LUT4_0 or Data of DFF12 | 51 |
| [317:312] | IN2 of LUT4_0 or nRST (nSET) of DFF12 | 52 |
| [323:318] | IN3 of LUT4_0 | 53 |
| [329:324] | Programmable delay/edge detect input | 54 |
| [335:330] | Filter/Edge detect input | 55 |
| [341:336] | GPIO0 Digital Output | 56 |
| [347:342] | GPIO1 Digital Output | 57 |
| [353:348] | GPIO2 Digital Output | 58 |
| [359:354] | GPIO2 Output Enable | 59 |
| [365:360] | Power Switch ON0, Digital Output | 60 |
| [371:366] | Reserved | 61 |
| [377:372] | Power Switch ON1, Digital Output | 62 |
| [383:378] | GPIO4 Digital Output | 63 |
| [389:384] | GPIO4 Output Enable | 64 |
| [395:390] | GPIO5 Digital Output | 65 |
| [401:396] | GPIO5 Output Enable | 66 |
| [407:402] | GPIO6 Digital Output | 67 |
| [413:408] | GPIO6 Output Enable | 68 |

**Table 21: Matrix Output Table** (continued)

| Register Bit Address | Matrix Output Signal Function | Matrix Output Number |
|---|---|---|
| [419:414] | GPIO7 Digital Output | 69 |
| [425:420] | GPIO7 Output Enable | 70 |
| [431:426] | GPIO8 Digital Output | 71 |
| [437:432] | GPIO8 Output Enable | 72 |
| [443:438] | GPIO9 Digital Output | 73 |
| [449:444] | GPIO9 Output Enable | 74 |
| [455:450] | pdb of ACMP0H | 75 |
| [461:456] | pdb of ACMP1H | 76 |
| [467:462] | pdb of ACMP2L | 77 |
| [473:468] | pdb of ACMP3L | 78 |
| [479:474] | pdb of Temp sensor | 79 |
| [485:480] | Oscillator0 ENABLE | 80 |
| [491:486] | Oscillator1 ENABLE | 81 |
| [497:492] | Oscillator2 ENABLE | 82 |
| [503:498] | IN0 of LUT4_1 or CLK Input of DFF20<br>Delay0 Input (or Counter0 nRST Input) | 83 |
| [509:504] | IN1 of LUT4_1 or nRST of DFF20<br>Delay0 Input (or Counter0 nRST Input) | 84 |
| [515:510] | IN2 of LUT4_1 or nSET of DFF20<br>Delay0 Input (or Counter0 nRST Input) | 85 |
| [521:516] | IN3 of LUT4_1 or Data of DFF20<br>Delay0 Input (or Counter0 nRST Input) | 86 |
| [527:522] | IN0 of LUT3_9 or CLK Input of DFF13<br>Delay1 Input (or Counter1 nRST Input) | 87 |
| [533:528] | IN1 of LUT3_9 or nRST (nSET) of DFF13<br>Delay1 Input (or Counter1 nRST Input) | 88 |
| [539:534] | IN2 of LUT3_9 or Data of DFF13<br>Delay1 Input (or Counter1 nRST Input) | 89 |
| [545:540] | IN0 of LUT3_10 or CLK Input of DFF14<br>Delay2 Input (or Counter2 nRST Input) | 90 |
| [551:546] | IN1 of LUT3_10 or nRST (nSET) of DFF14<br>Delay2 Input (or Counter2 nRST Input) | 91 |
| [557:552] | IN2 of LUT3_10 or Data of DFF14<br>Delay2 Input (or Counter2 nRST Input) | 92 |
| [563:558] | IN0 of LUT3_11 or CLK Input of DFF15<br>Delay3 Input (or Counter3 nRST Input) | 93 |
| [569:564] | IN1 of LUT3_11 or nRST (nSET) of DFF15<br>Delay3 Input (or Counter3 nRST Input) | 94 |
| [575:570] | IN2 of LUT3_11 or Data of DFF15<br>Delay3 Input (or Counter3 nRST Input) | 95 |

**Note 1** For each Address, the two most significant bits are unused.

### 6.3 CONNECTION MATRIX VIRTUAL INPUTS

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via $I^2C$. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The $I^2C$ address for reading and writing these register values is at byte 0x4C (076).

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An $I^2C$ write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs (GPIO0Digital or $I^2C$_virtual_0 Input), and (GPIO1 Digital or $I^2C$_virtual_1 Input). If the virtual input mode is selected, an $I^2C$ write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The $I^2C$ disable/enable register bit [2032] selects whether the Connection Matrix input comes from the Pin input or from the virtual register:

- Select SCL & Virtual Input 0 or GPIO0
- Select SDA & Virtual Input 1 or GPIO1

See Table 22 for Connection Matrix Virtual Inputs.

**Table 22: Connection Matrix Virtual Inputs**

| Matrix Input Number | Matrix Input Signal Function | Register Bit Addresses (d) |
|---|---|---|
| 32 | $I^2C$_virtual_0 Input | [608] |
| 33 | $I^2C$_virtual_1 Input | [609] |
| 34 | $I^2C$_virtual_2 Input | [610] |
| 35 | $I^2C$_virtual_3 Input | [611] |
| 36 | $I^2C$_virtual_4 Input | [612] |
| 37 | $I^2C$_virtual_5 Input | [613] |
| 38 | $I^2C$_virtual_6 Input | [614] |
| 39 | $I^2C$_virtual_7 Input | [615] |

### 6.4 CONNECTION MATRIX VIRTUAL OUTPUTS

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via $I^2C$. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The $I^2C$ addresses for reading these register values are bytes 0x48 (072) to 0x4F (079). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x4C (076)).

# 7 Combination Function Macrocells

The SLG46867 has 15 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGEN)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

## 7.1 2-BIT LUT OR D FLIP-FLOP MACROCELLS

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

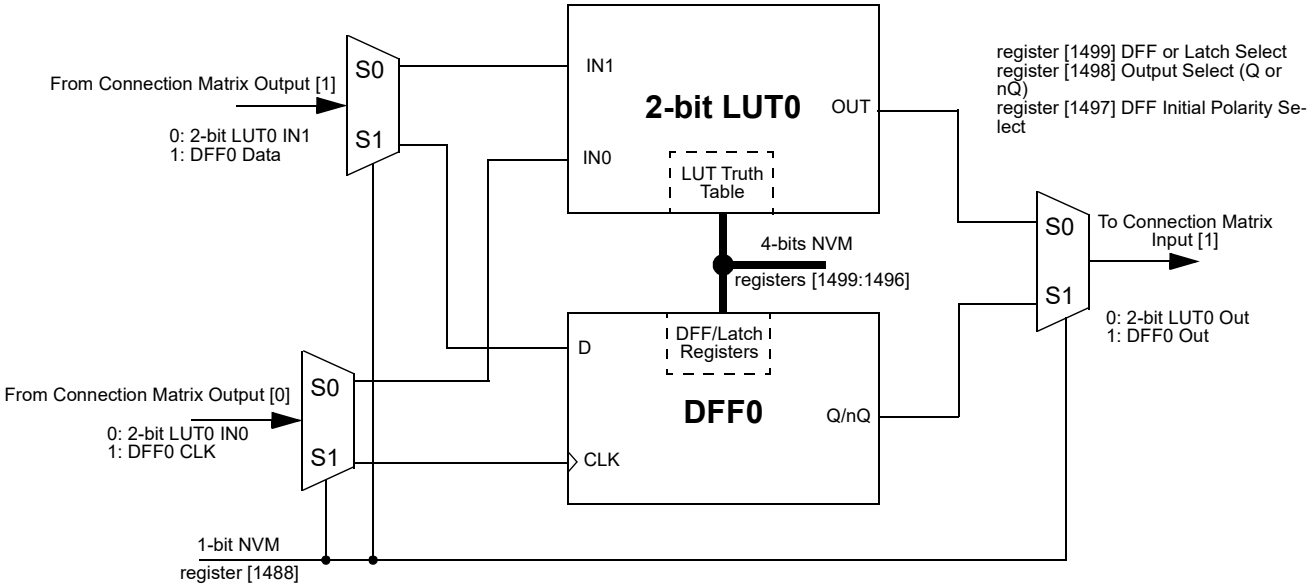



**Figure 10: 2-bit LUT0 or DFF0**

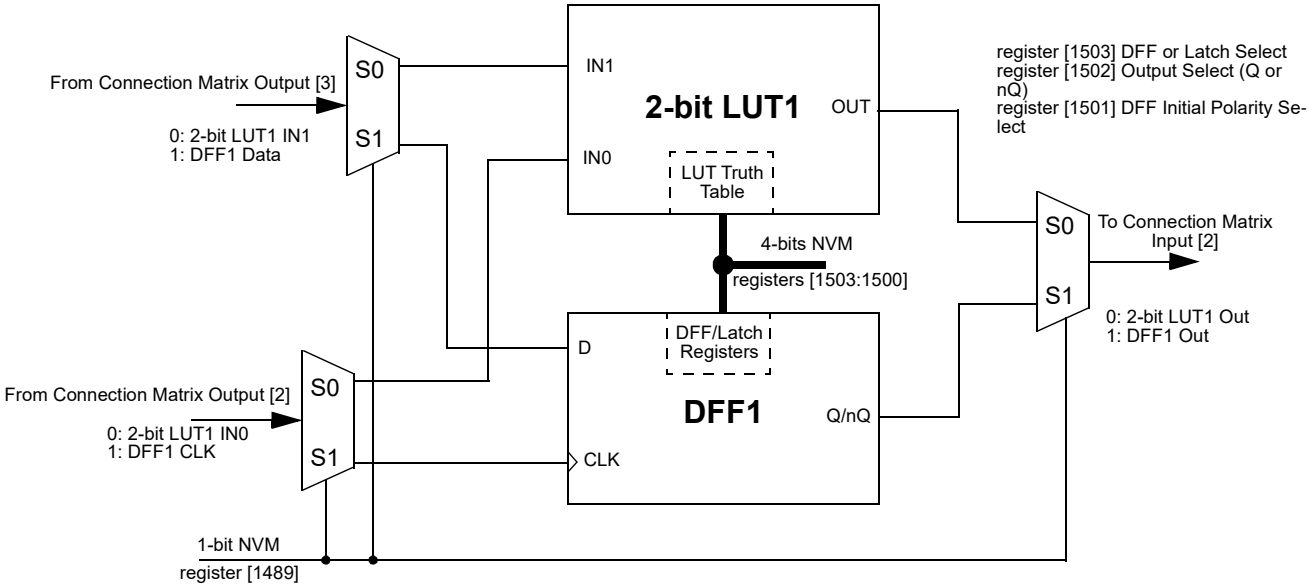



**Figure 11: 2-bit LUT1 or DFF1**

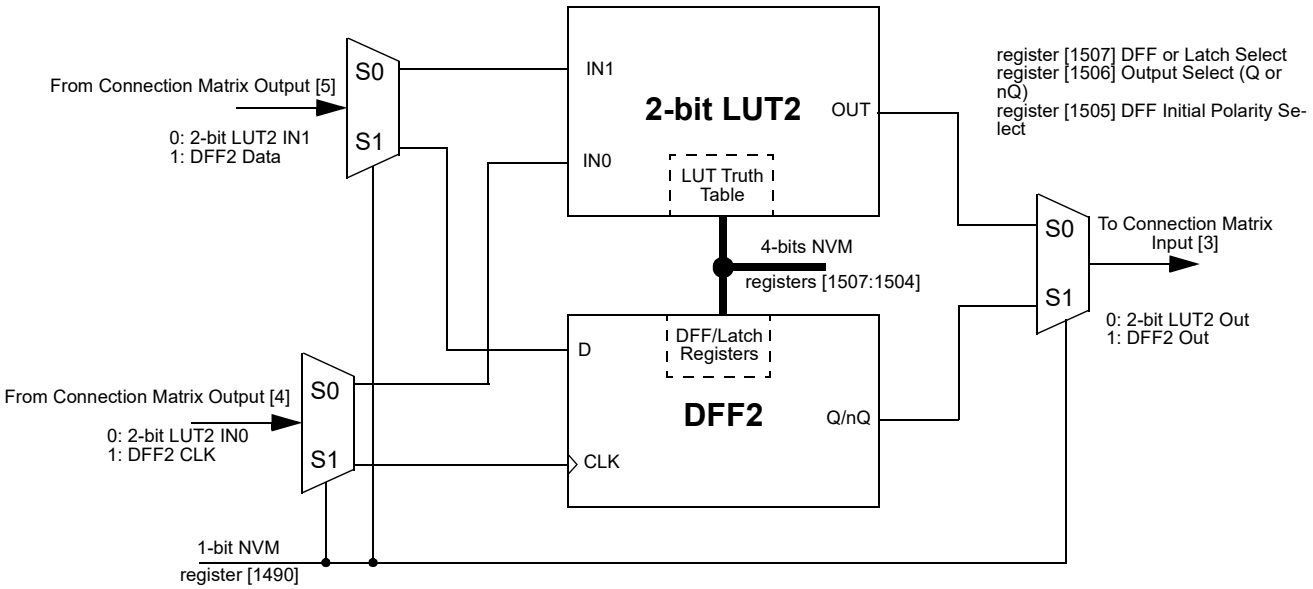



**Figure 12: 2-bit LUT2 or DFF2**

### 7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

**Table 23: 2-bit LUT0 Truth Table**

| IN1 | IN0 | OUT | |
|---|---|---|---|
| 0 | 0 | register [1496] | LSB |
| 0 | 1 | register [1497] | |
| 1 | 0 | register [1498] | |
| 1 | 1 | register [1499] | MSB |

**Table 24: 2-bit LUT1 Truth Table**

| IN1 | IN0 | OUT | |
|---|---|---|---|
| 0 | 0 | register [1500] | LSB |
| 0 | 1 | register [1501] | |
| 1 | 0 | register [1502] | |
| 1 | 1 | register [1503] | MSB |

**Table 25: 2-bit LUT2 Truth Table**

| IN1 | IN0 | OUT | |
|---|---|---|---|
| 0 | 0 | register [1504] | LSB |
| 0 | 1 | register [1505] | |
| 1 | 0 | register [1506] | |
| 1 | 1 | register [1507] | MSB |

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

*2-Bit LUT0 is defined by registers [1499:1496]*

*2-Bit LUT1 is defined by registers [1503:1500]*

*2-Bit LUT2 is defined by registers [1507:1504]*

The Table 26 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells

**Table 26: 2-bit LUT Standard Digital Functions**

| Function | MSB | | | LSB |
|---|---|---|---|---|
| AND-2 | 1 | 0 | 0 | 0 |
| NAND-2 | 0 | 1 | 1 | 1 |
| OR-2 | 1 | 1 | 1 | 0 |
| NOR-2 | 0 | 0 | 0 | 1 |
| XOR-2 | 0 | 1 | 1 | 0 |
| XNOR-2 | 1 | 0 | 0 | 1 |

### 7.1.2 Initial Polarity Operations

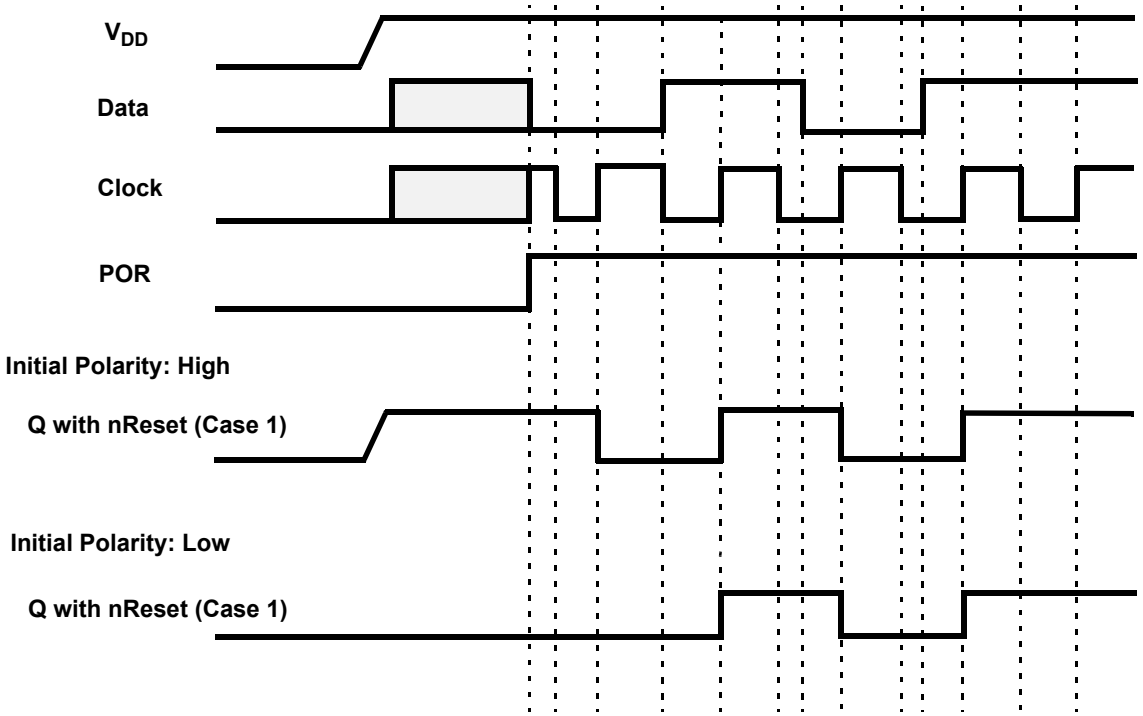



**Figure 13: DFF Polarity Operations**

## 7.2 2-BIT LUT OR PROGRAMMABLE PATTERN GENERATOR

The SLG46867 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGEN).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function. It is possible to define the RST level for the PGEN macrocell. There are both high level reset (RST) and a low level reset (nRST) options available which are selected by register [1409].

When operating as a Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

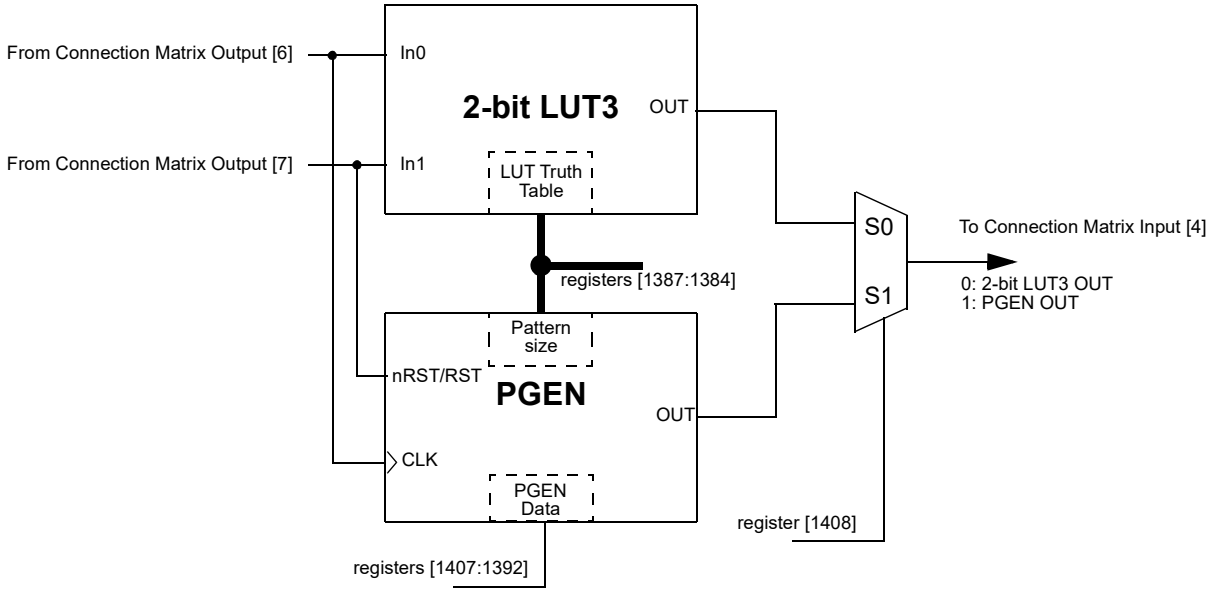



**Figure 14: 2-bit LUT3 or PGEN**

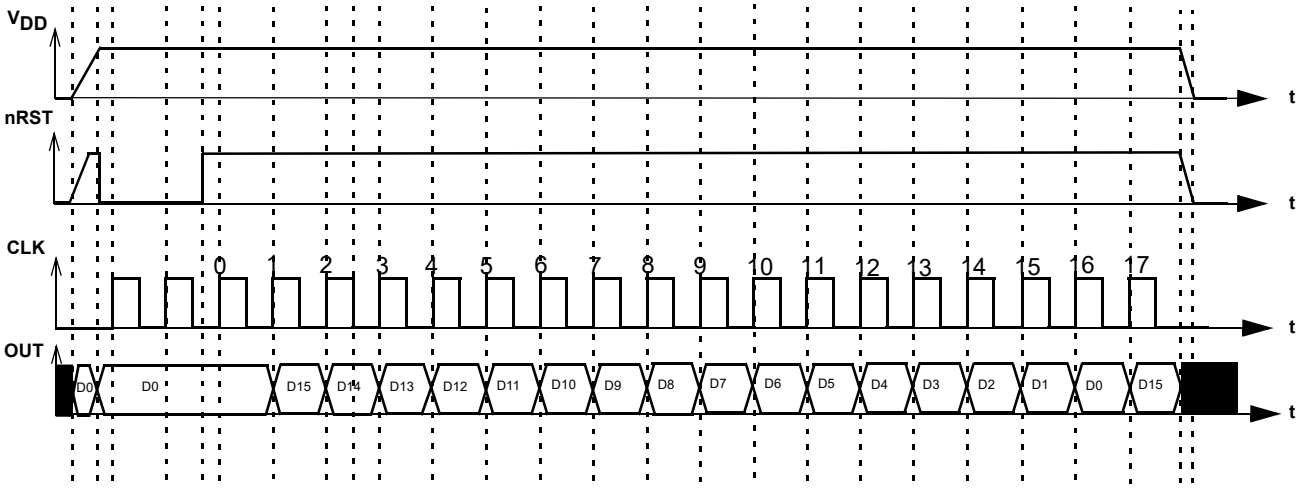



**Figure 15: PGEN Timing Diagram**

### 7.2.1 2-Bit LUT or PGEN Macrocell Used as 2-Bit LUT

**Table 27: 2-bit LUT1 Truth Table**

| IN1 | IN0 | OUT | |
|---|---|---|---|
| 0 | 0 | register [1384] | LSB |
| 0 | 1 | register [1385] | |
| 1 | 0 | register [1386] | |
| 1 | 1 | register [1387] | MSB |

This Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

*2-Bit LUT3 is defined by registers [1387:1384]*

The Table 28 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

**Table 28: 2-bit LUT Standard Digital Functions**

| Function | MSB | | | LSB |
|---|---|---|---|---|
| AND-2 | 1 | 0 | 0 | 0 |
| NAND-2 | 0 | 1 | 1 | 1 |
| OR-2 | 1 | 1 | 1 | 0 |
| NOR-2 | 0 | 0 | 0 | 1 |
| XOR-2 | 0 | 1 | 1 | 0 |
| XNOR-2 | 1 | 0 | 0 | 1 |

## 7.3 3-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELLS

There are nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/Latch macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1442].

- If register [1444] = 0, and the CLK is rising edge triggered, then Q=D, otherwise Q will not change.
- If register [1444] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

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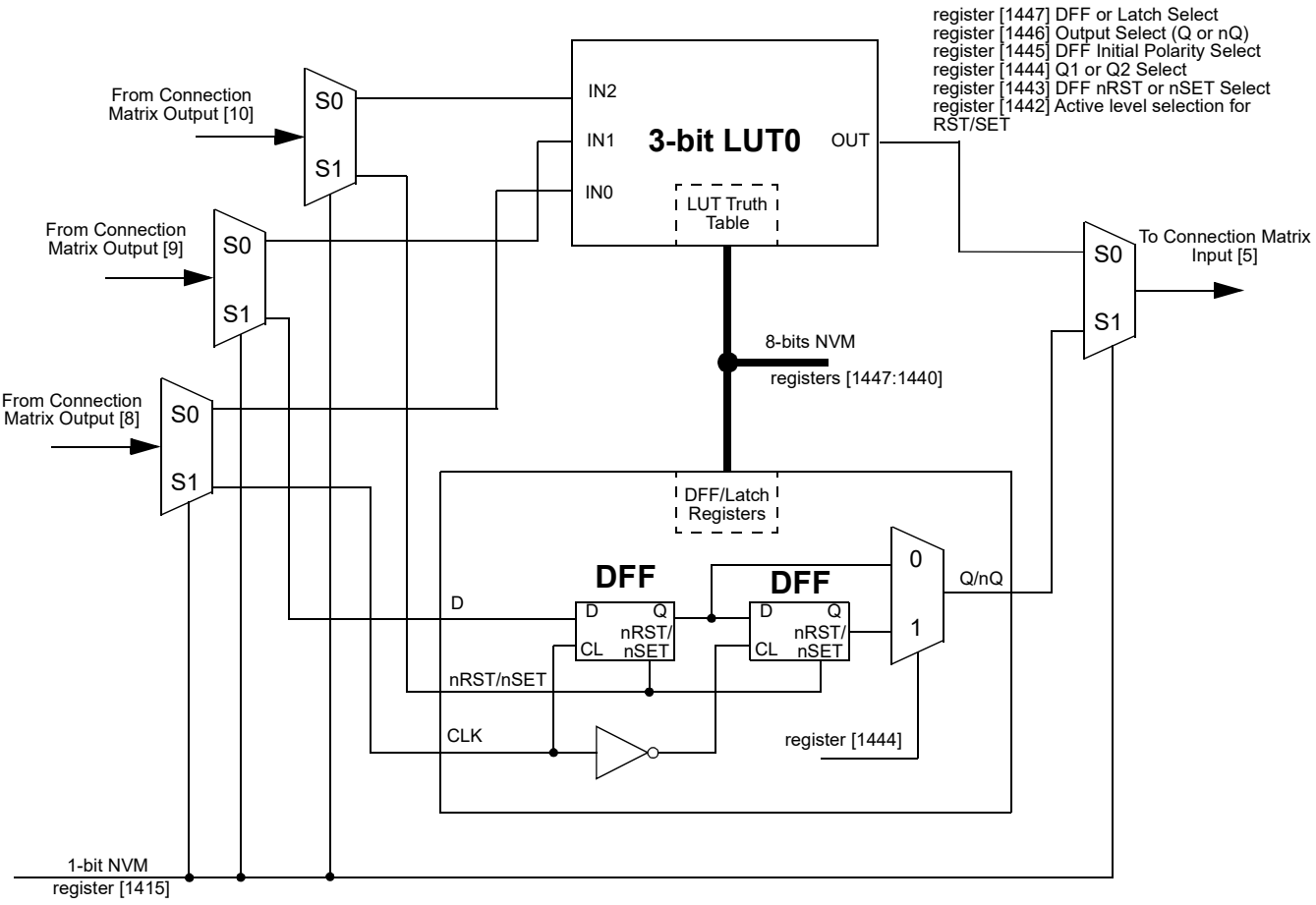



**Figure 16: 3-bit LUT0 or DFF3**

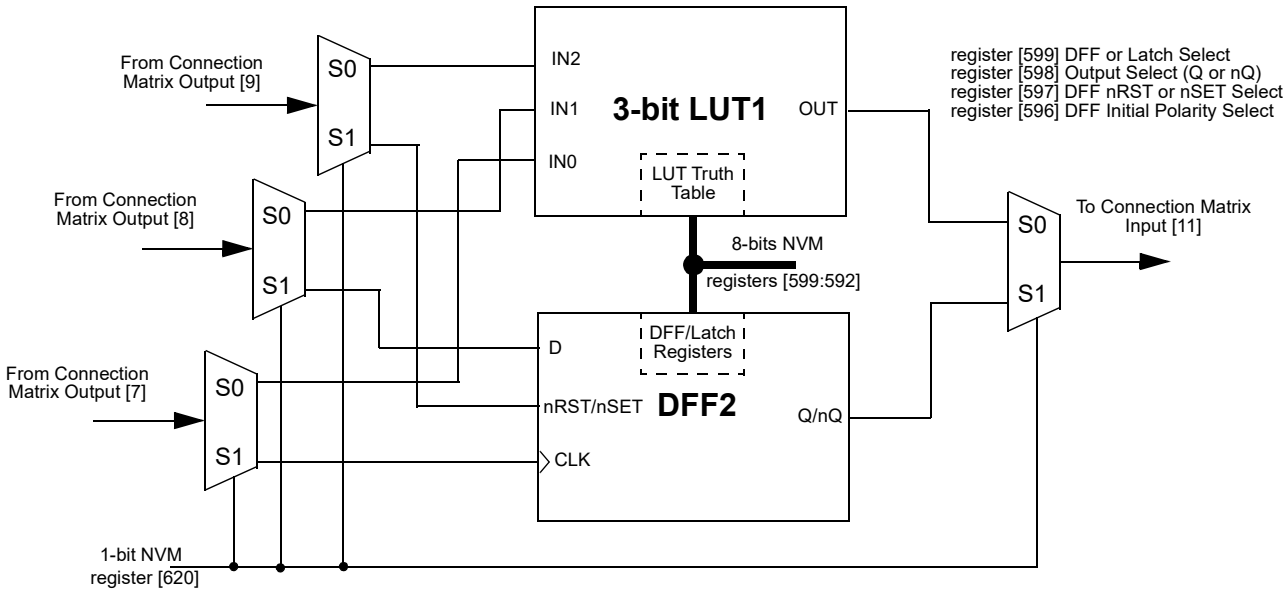



**Figure 17: 3-bit LUT1 or DFF2**

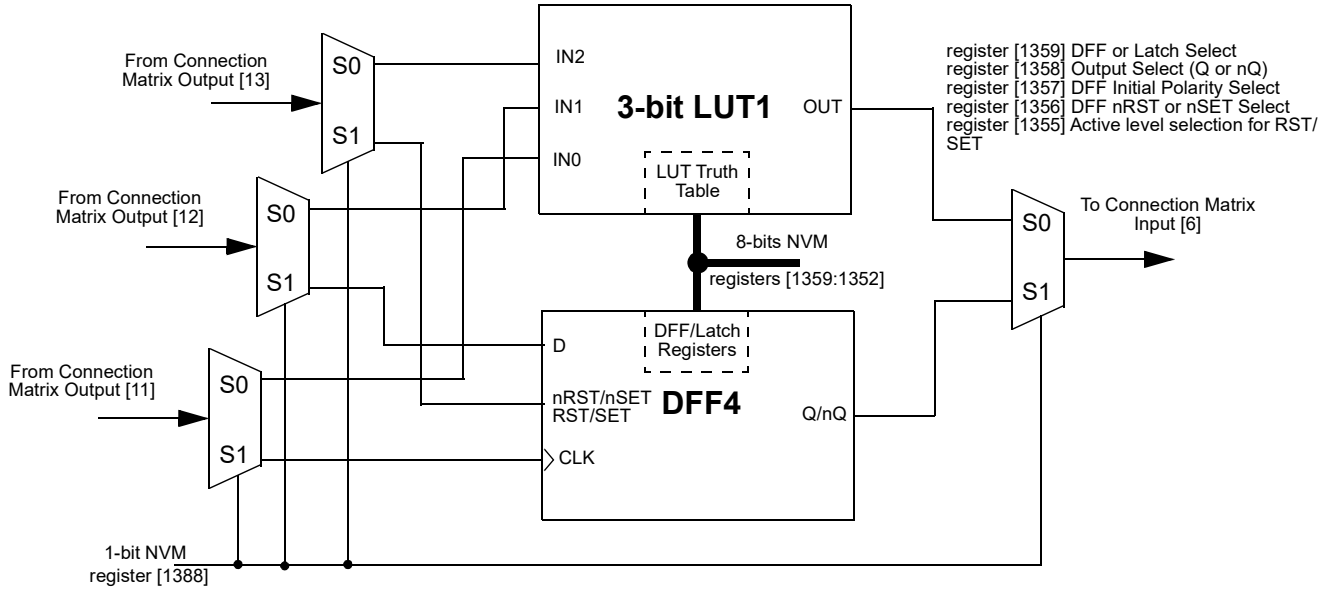



**Figure 18: 3-bit LUT1 or DFF4**

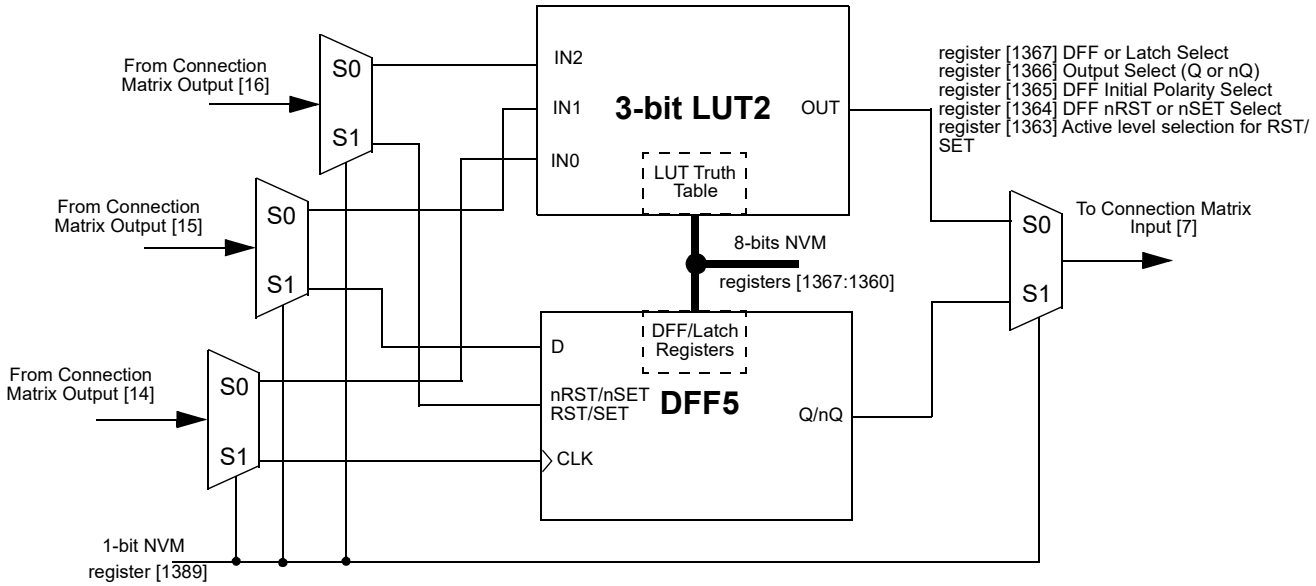



**Figure 19: 3-bit LUT2 or DFF5**

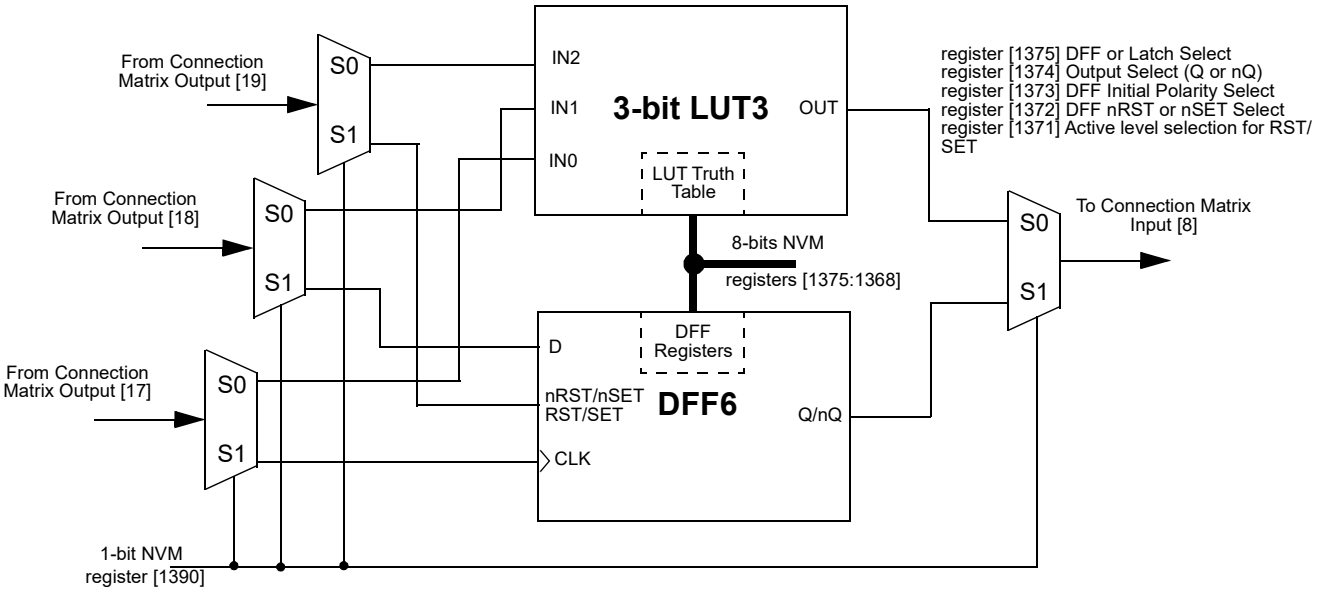



**Figure 20: 3-bit LUT3 or DFF6**

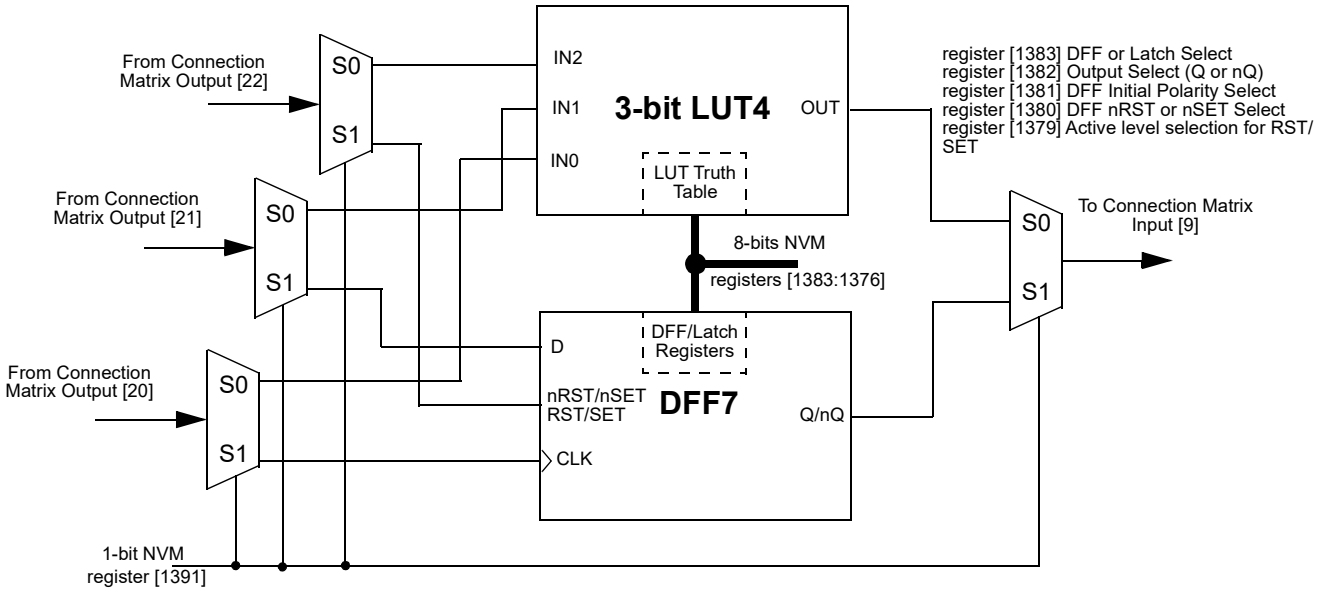



**Figure 21: 3-bit LUT4 or DFF7**

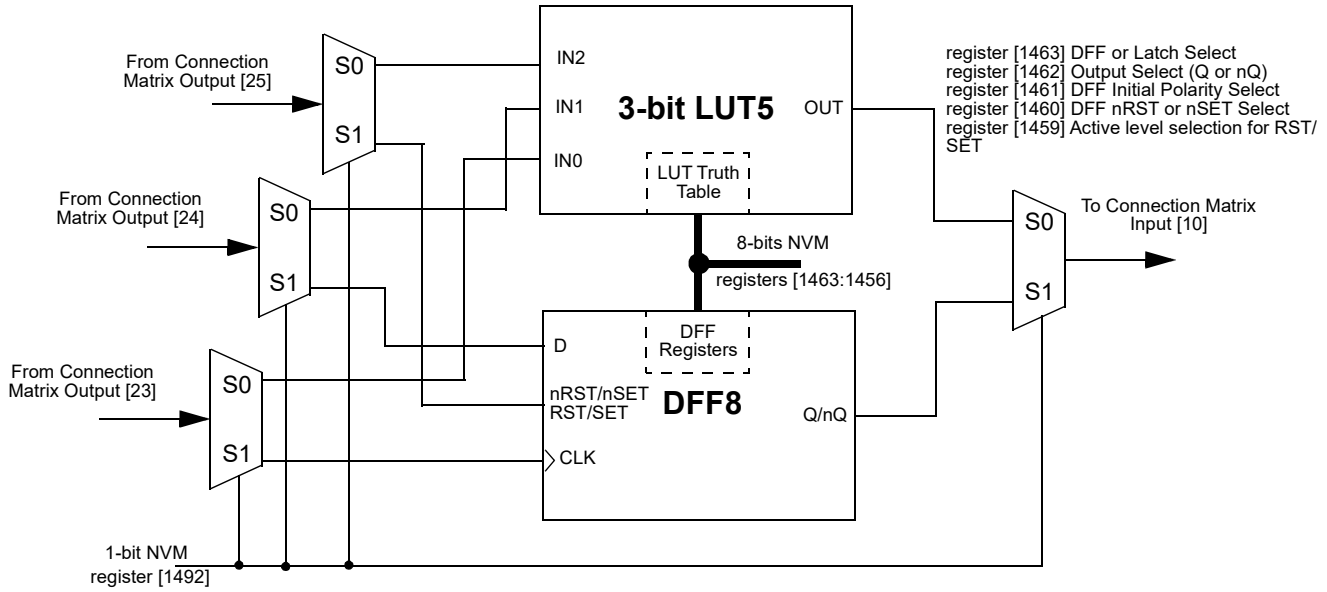



**Figure 22: 3-bit LUT5 or DFF8**

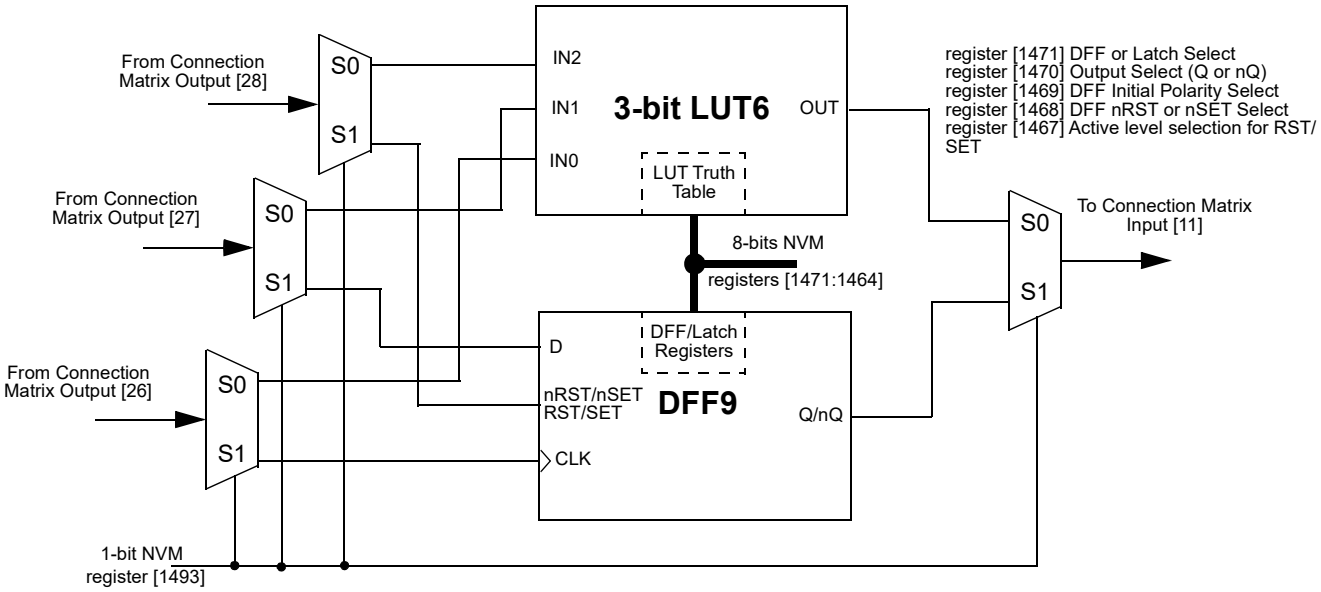



**Figure 23: 3-bit LUT8 or DFF9**

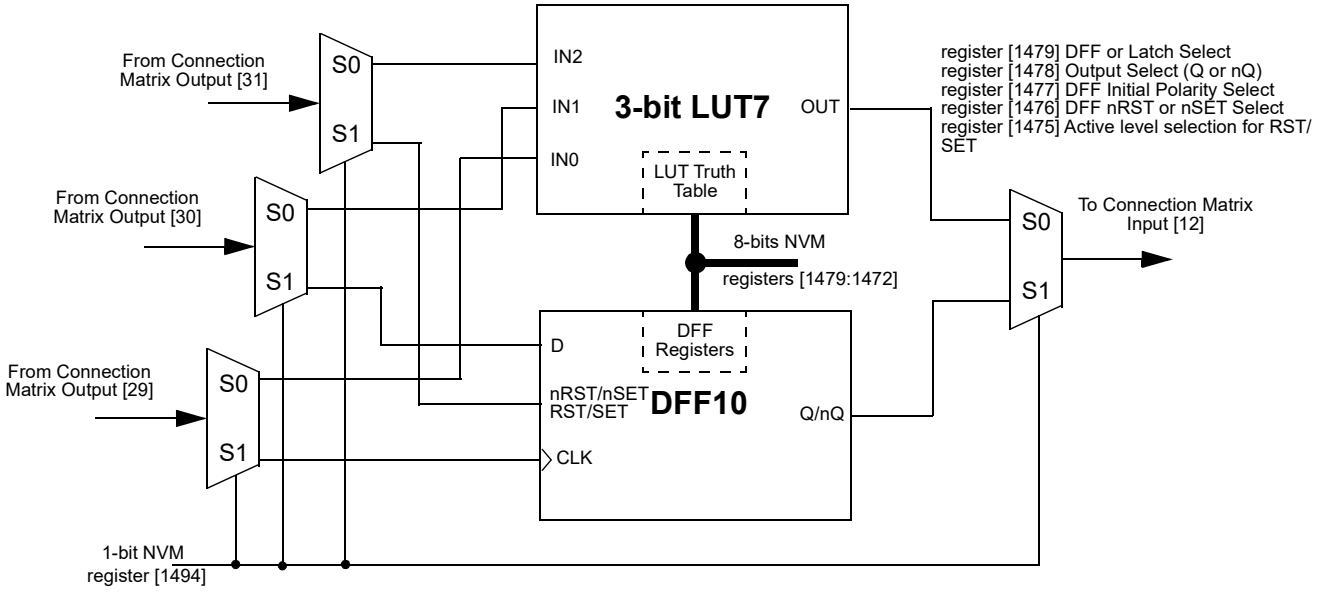



**Figure 24: 3-bit LUT7 or DFF10**

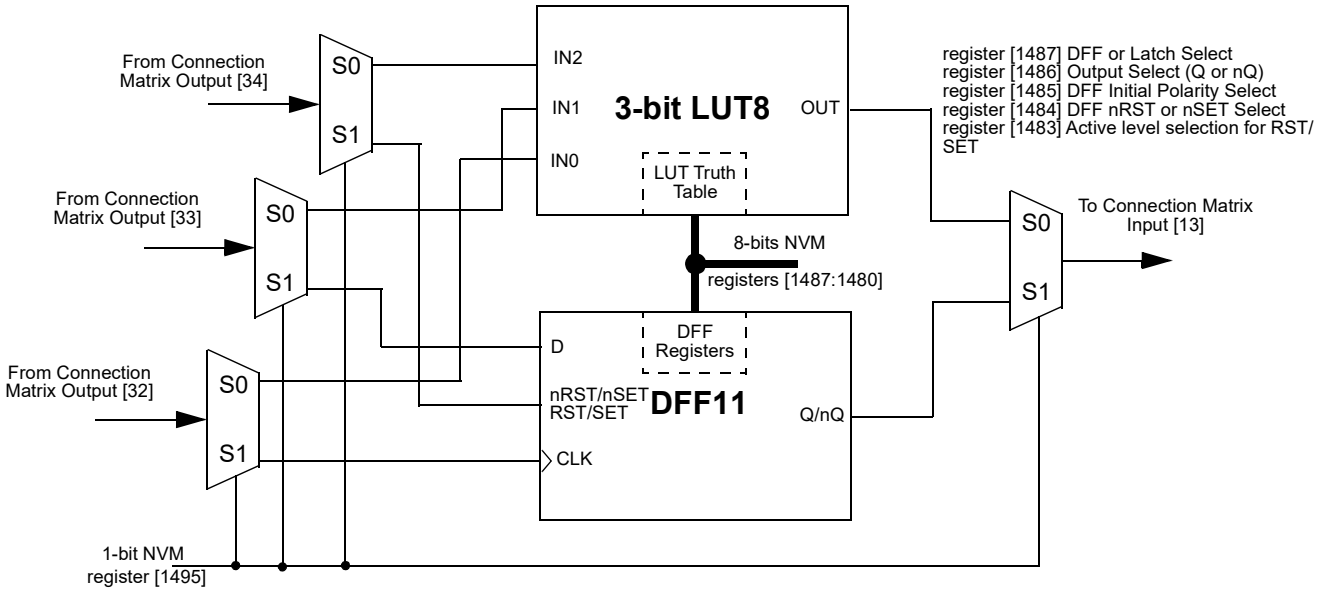



**Figure 25: 3-bit LUT8 or DFF11**

### 7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

**Table 29: 3-bit LUT0 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1440] | LSB |
| 0 | 0 | 1 | register [1441] | |
| 0 | 1 | 0 | register [1442] | |
| 0 | 1 | 1 | register [1443] | |
| 1 | 0 | 0 | register [1444] | |
| 1 | 0 | 1 | register [1445] | |
| 1 | 1 | 0 | register [1446] | |
| 1 | 1 | 1 | register [1447] | MSB |

**Table 30: 3-bit LUT1 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1352] | LSB |
| 0 | 0 | 1 | register [1353] | |
| 0 | 1 | 0 | register [1354] | |
| 0 | 1 | 1 | register [1355] | |
| 1 | 0 | 0 | register [1356] | |
| 1 | 0 | 1 | register [1357] | |
| 1 | 1 | 0 | register [1358] | |
| 1 | 1 | 1 | register [1359] | MSB |

**Table 31: 3-bit LUT2 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1360] | LSB |
| 0 | 0 | 1 | register [1361] | |
| 0 | 1 | 0 | register [1362] | |
| 0 | 1 | 1 | register [1363] | |
| 1 | 0 | 0 | register [1364] | |
| 1 | 0 | 1 | register [1365] | |
| 1 | 1 | 0 | register [1366] | |
| 1 | 1 | 1 | register [1367] | MSB |

**Table 32: 3-bit LUT3 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1368] | LSB |
| 0 | 0 | 1 | register [1369] | |
| 0 | 1 | 0 | register [1370] | |
| 0 | 1 | 1 | register [1371] | |
| 1 | 0 | 0 | register [1372] | |
| 1 | 0 | 1 | register [1373] | |
| 1 | 1 | 0 | register [1374] | |
| 1 | 1 | 1 | register [1375] | MSB |

**Table 33: 3-bit LUT4 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1376] | LSB |
| 0 | 0 | 1 | register [1377] | |
| 0 | 1 | 0 | register [1378] | |
| 0 | 1 | 1 | register [1379] | |
| 1 | 0 | 0 | register [1380] | |
| 1 | 0 | 1 | register [1481] | |
| 1 | 1 | 0 | register [1382] | |
| 1 | 1 | 1 | register [1383] | MSB |

**Table 34: 3-bit LUT5 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1356] | LSB |
| 0 | 0 | 1 | register [1357] | |
| 0 | 1 | 0 | register [1358] | |
| 0 | 1 | 1 | register [1359] | |
| 1 | 0 | 0 | register [1360] | |
| 1 | 0 | 1 | register [1361] | |
| 1 | 1 | 0 | register [1361] | |
| 1 | 1 | 1 | register [1363] | MSB |

**Table 35: 3-bit LUT6 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1364] | LSB |
| 0 | 0 | 1 | register [1365] | |
| 0 | 1 | 0 | register [1366] | |
| 0 | 1 | 1 | register [1367] | |
| 1 | 0 | 0 | register [1368] | |
| 1 | 0 | 1 | register [1369] | |
| 1 | 1 | 0 | register [1370] | |
| 1 | 1 | 1 | register [1371] | MSB |

**Table 36: 3-bit LUT7 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1472] | LSB |
| 0 | 0 | 1 | register [1473] | |
| 0 | 1 | 0 | register [1474] | |
| 0 | 1 | 1 | register [1475] | |
| 1 | 0 | 0 | register [1476] | |
| 1 | 0 | 1 | register [1477] | |
| 1 | 1 | 0 | register [1478] | |
| 1 | 1 | 1 | register [1479] | MSB |

**Table 37: 3-bit LUT8 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1480] | LSB |
| 0 | 0 | 1 | register [1481] | |
| 0 | 1 | 0 | register [1482] | |
| 0 | 1 | 1 | register [1483] | |
| 1 | 0 | 0 | register [1484] | |
| 1 | 0 | 1 | register [1485] | |
| 1 | 1 | 0 | register [1486] | |
| 1 | 1 | 1 | register [1487] | MSB |

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT0 is defined by registers [1447:1440]*

*3-Bit LUT1 is defined by registers [1359:1352]*

*3-Bit LUT2 is defined by registers [1367:1360]*

*3-Bit LUT3 is defined by registers [1375:1368]*

*3-Bit LUT4 is defined by registers [1383:1376]*

*3-Bit LUT5 is defined by registers [1463:1456]*

*3-Bit LUT6 is defined by registers [1471:1464]*

*3-Bit LUT7 is defined by registers [1479:1472]*

*3-Bit LUT8 is defined by registers [1487:1480]*

The Table 38 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

**Table 38: 3-bit LUT Standard Digital Functions**

| Function | MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|
| AND-3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NAND-3 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| OR-3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| NOR-3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOR-3 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| XNOR-3 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 7.3.2 Initial Polarity Operations

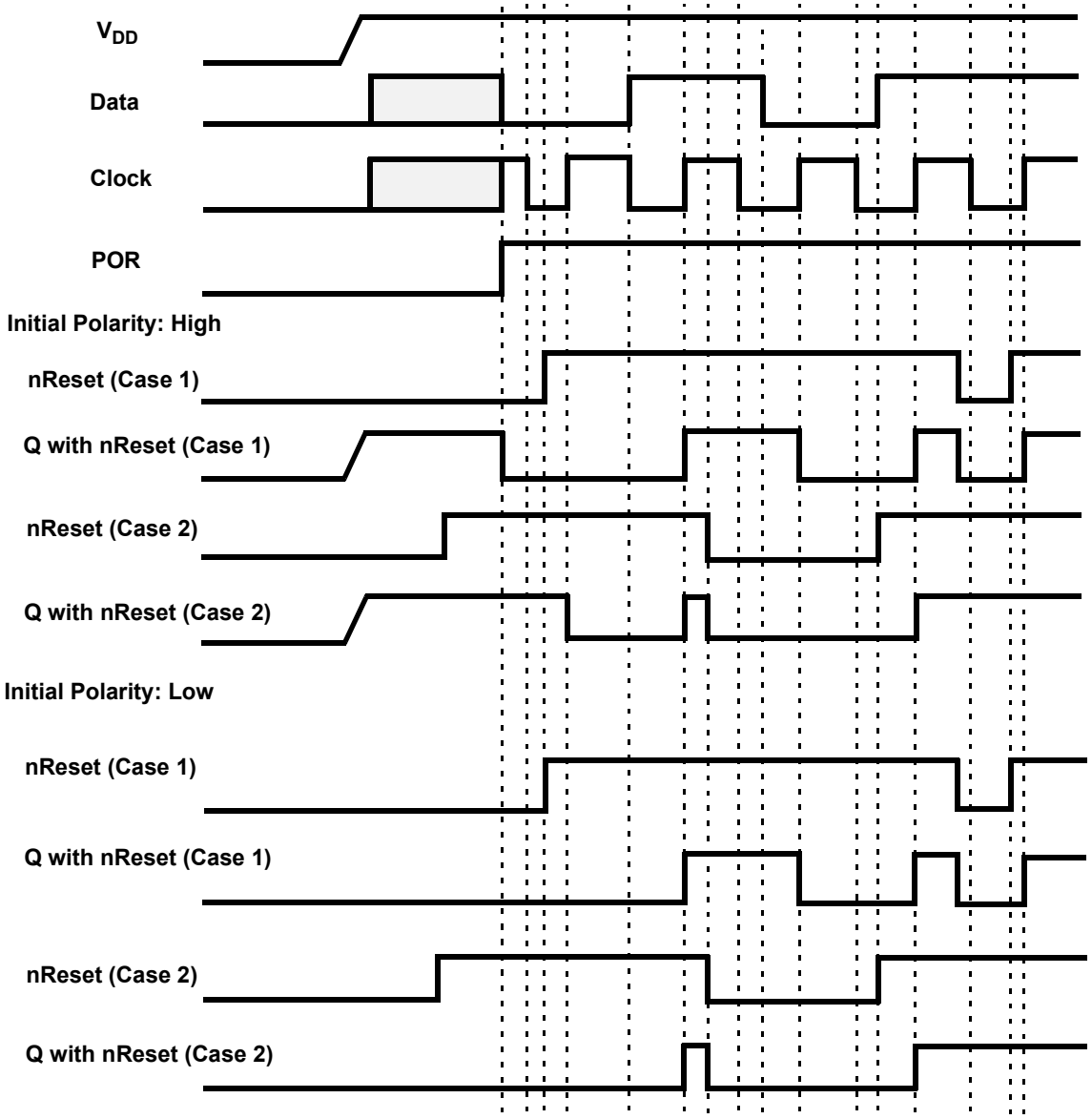



**Figure 26: DFF Polarity Operations with nReset**

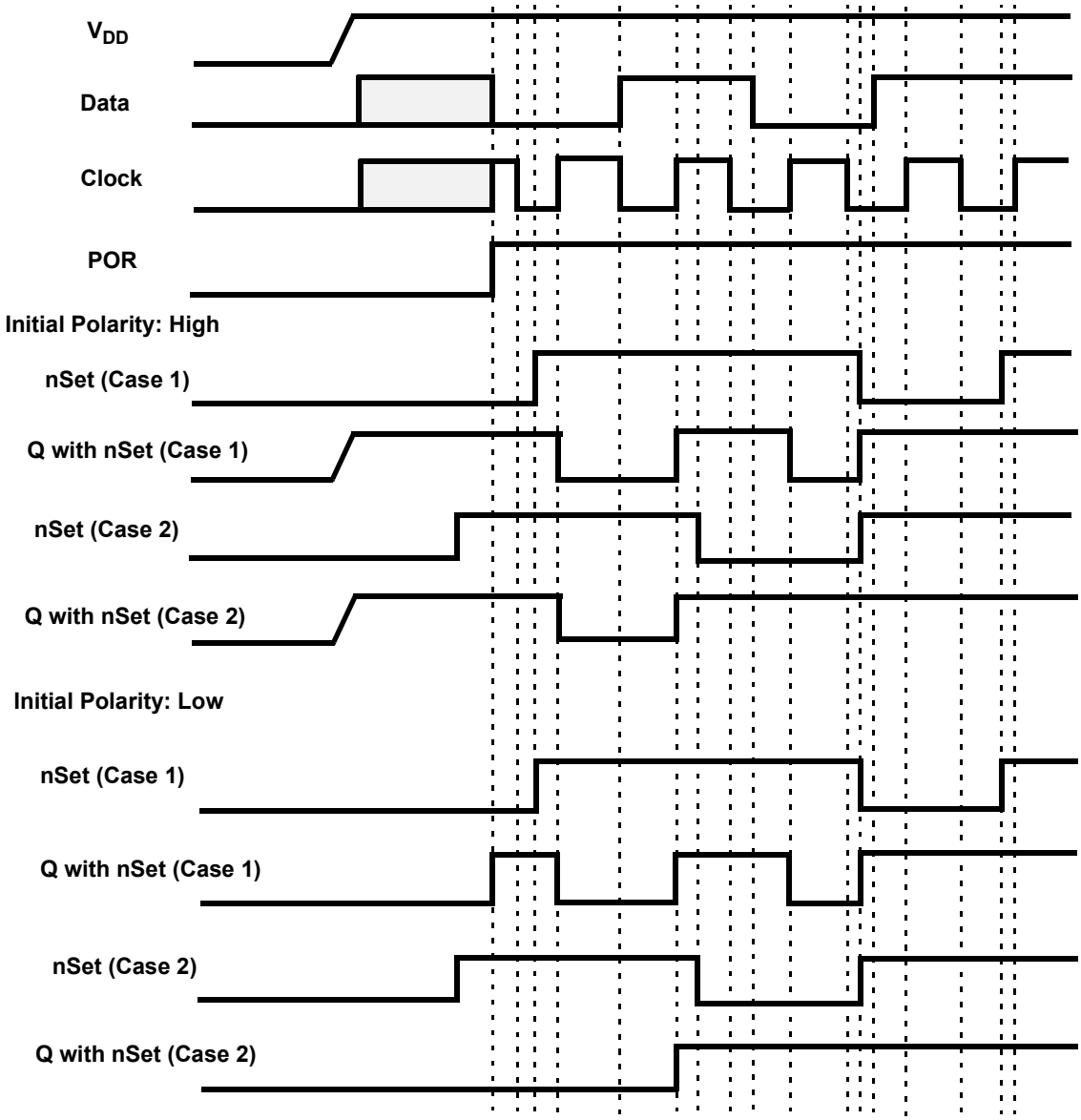



**Figure 27: DFF Polarity Operations with nSet**

### 7.4 4-BIT LUT OR D FLIP-FLOP WITH SET/RESET MACROCELL

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

- If register [1436] = 0, and the CLK is rising edge triggered, then Q=D, otherwise Q will not change.
- If register [1436] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

It is possible to define the active level for the reset/set input of DFF/Latch macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1434].

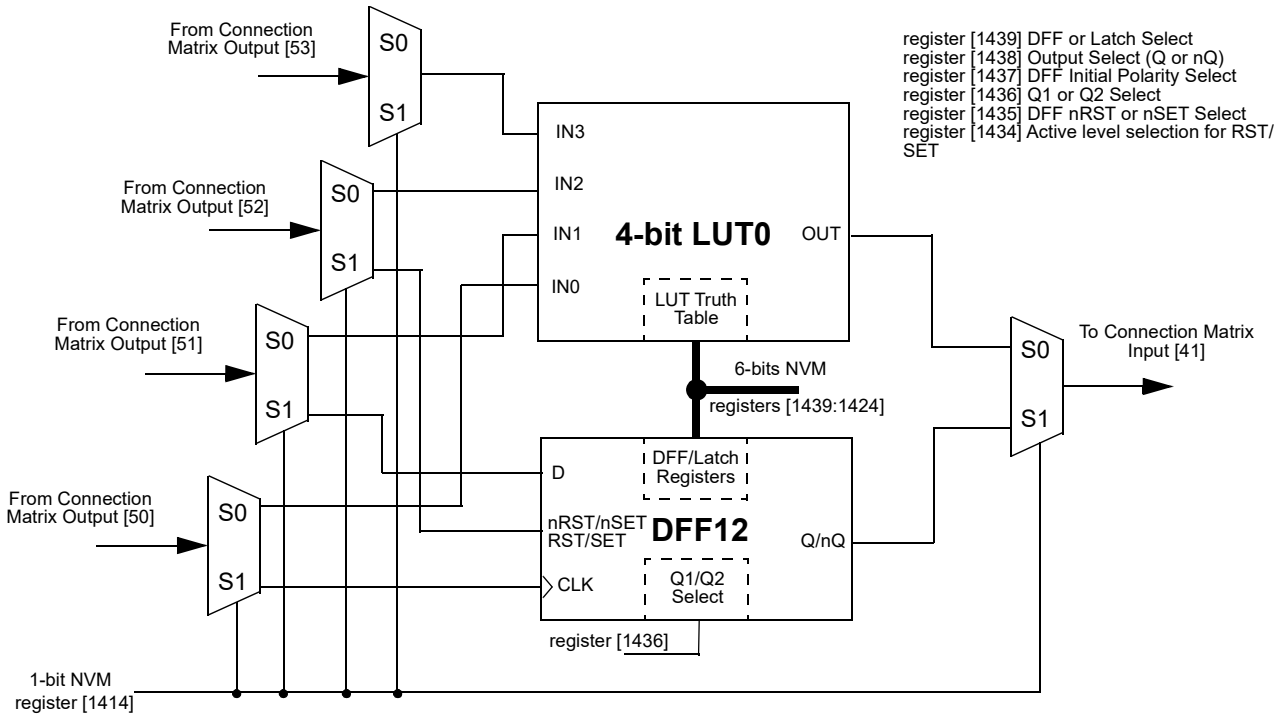



**Figure 28: 4-bit LUT0 or DFF12**

### 7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

**Table 39: 4-bit LUT0 Truth Table**

| IN3 | IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | register [1424] | LSB |
| 0 | 0 | 0 | 1 | register [1425] | |
| 0 | 0 | 1 | 0 | register [1426] | |
| 0 | 0 | 1 | 1 | register [1427] | |
| 0 | 1 | 0 | 0 | register [1428] | |
| 0 | 1 | 0 | 1 | register [1429] | |
| 0 | 1 | 1 | 0 | register [1430] | |
| 0 | 1 | 1 | 1 | register [1431] | |
| 1 | 0 | 0 | 0 | register [1432] | |
| 1 | 0 | 0 | 1 | register [1433] | |
| 1 | 0 | 1 | 0 | register [1434] | |
| 1 | 0 | 1 | 1 | register [1435] | |
| 1 | 1 | 0 | 0 | register [1436] | |
| 1 | 1 | 0 | 1 | register [1437] | |
| 1 | 1 | 1 | 0 | register [1438] | |
| 1 | 1 | 1 | 1 | register [1439] | MSB |

This Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

*4-Bit LUT0 is defined by registers [1439:1424]*

**Table 40: 4-bit LUT Standard Digital Functions**

| Function | MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AND-4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NAND-4 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| OR-4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| NOR-4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOR-4 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| XNOR-4 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

### 7.5 3-BIT LUT OR PIPE DELAY/RIPPLE COUNTER MACROCELL

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (nRST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by registers [1419:1416] for OUT0 and registers [1423:1420] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46867 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG46867). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1413]).

In the Ripple Counter mode there are 3 options for setting which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. This value will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting output code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1….SV+1→SV etc (if SV is smaller than EV) or SV→SV-1….EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV etc.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV etc. see Ripple counter functionality example in Figure 30.

Every step is executed by the rising edge on CLK input.

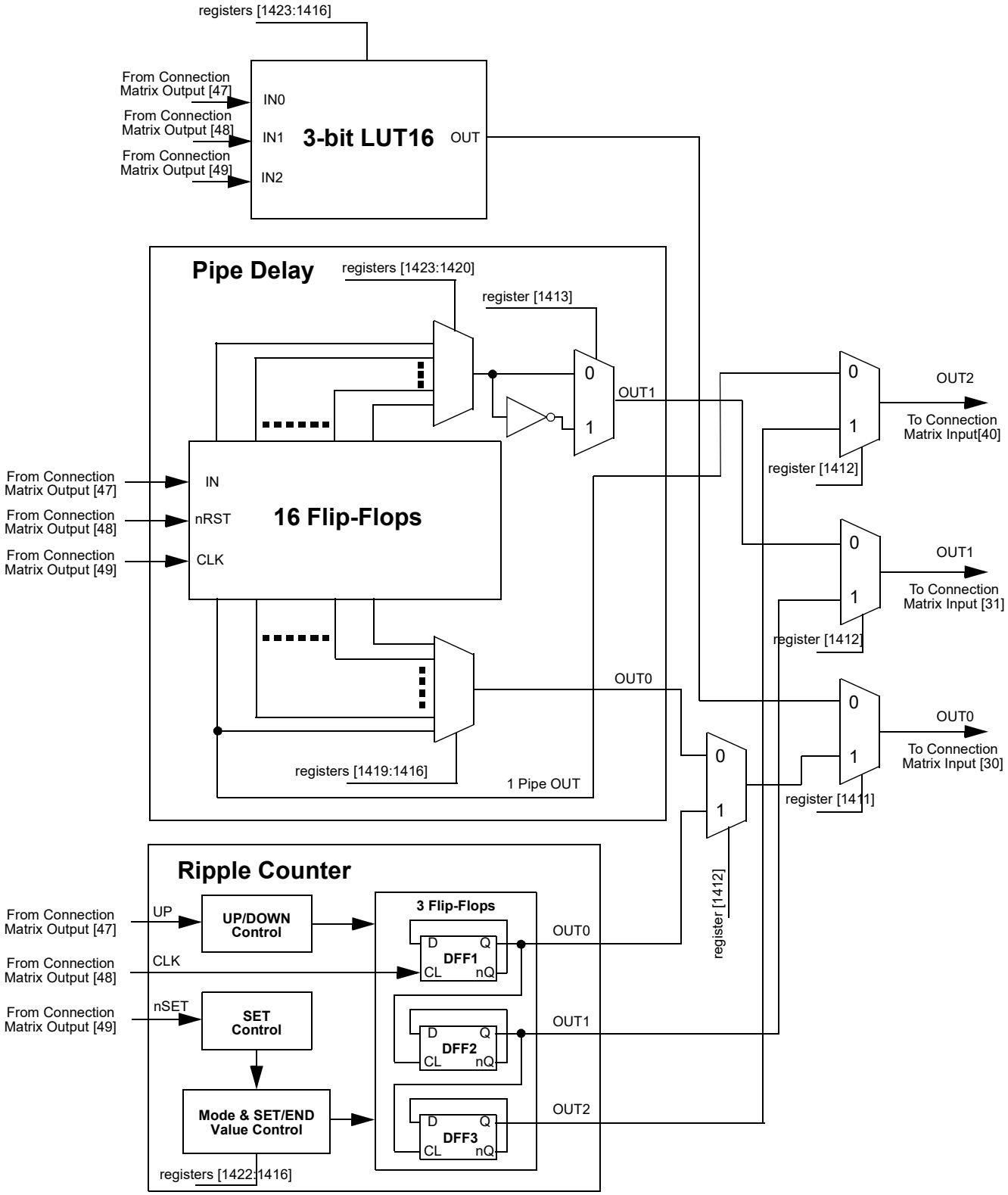



**Figure 29: 3-bit LUT16/Pipe Delay/Ripple Counter**

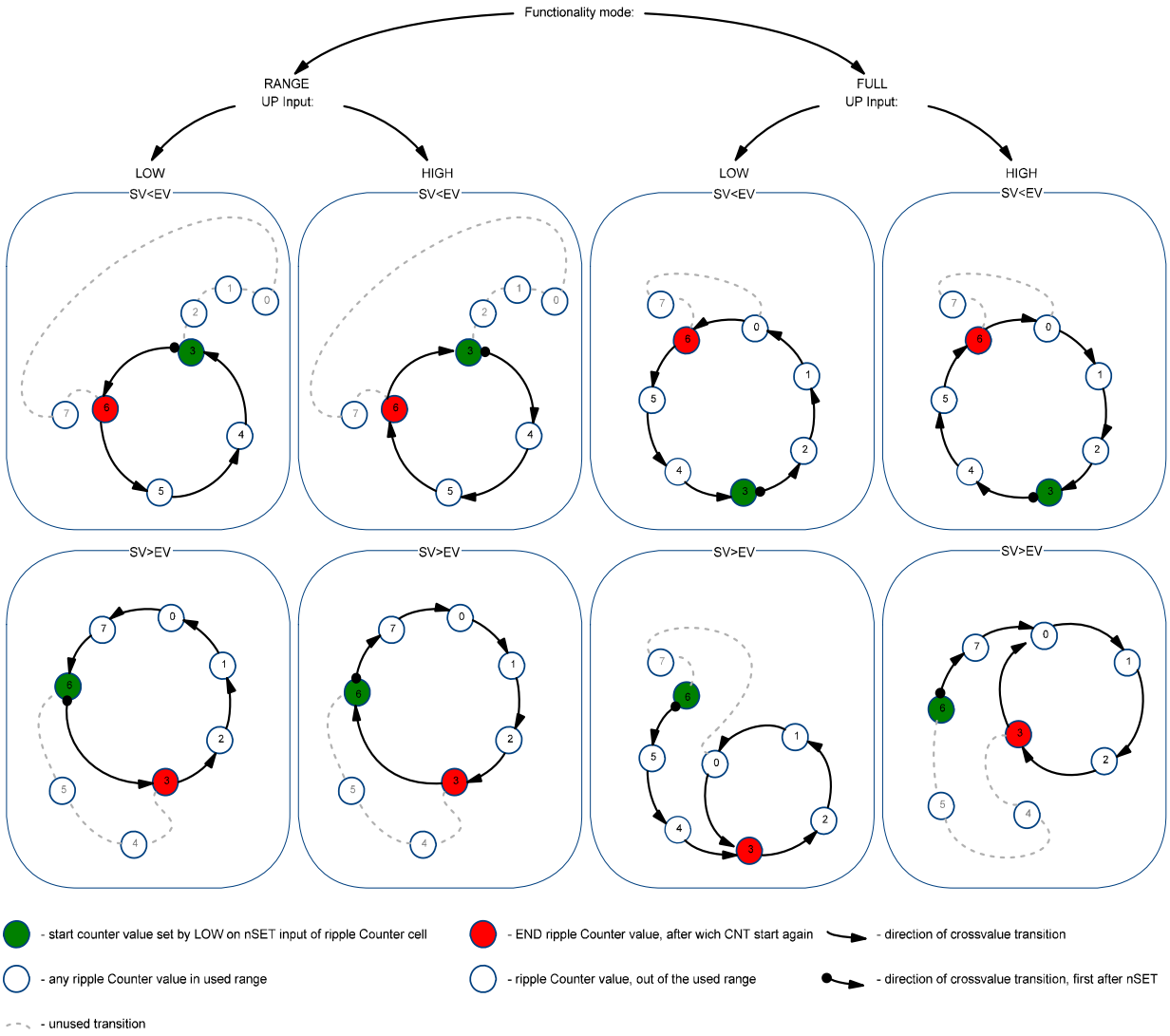



**Figure 30: Example: Ripple Counter Functionality**

### 7.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

**Table 41: 3-bit LUT16 Truth Table**

| IN2 | IN1 | IN0 | OUT |
|---|---|---|---|
| 0 | 0 | 0 | register [1416] |
| 0 | 0 | 1 | register [1417] |
| 0 | 1 | 0 | register [1418] |
| 0 | 1 | 1 | register [1419] |
| 1 | 0 | 0 | register [1420] |
| 1 | 0 | 1 | register [1421] |
| 1 | 1 | 0 | register [1422] |
| 1 | 1 | 1 | register [1423] |

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT16 is defined by registers [1423:1416]*

# 8 Multi-Function Macrocells

The SLG46867 has 8 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect etc. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 31.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

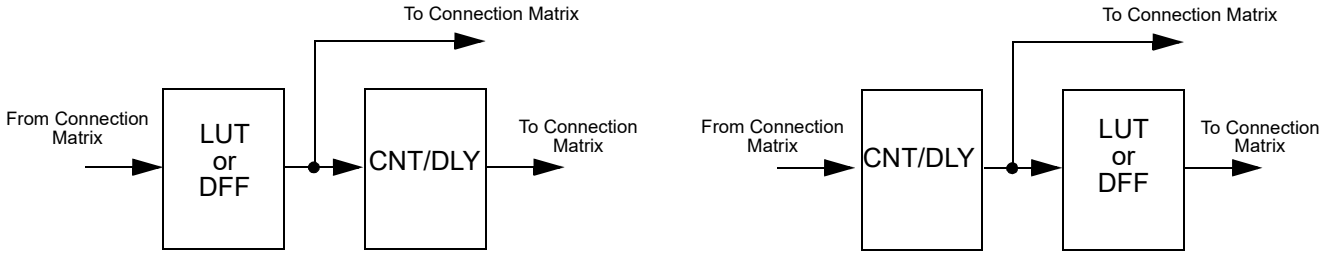



**Figure 31: Possible Connections Inside Multi-Function Macrocell**

Inputs/Outputs for the 8 Multi-Function function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

## 8.1 3-BIT LUT OR DFF/LATCH WITH 8-BIT COUNTER/DELAY MACROCELLS

There are seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Set/Reset (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Sections 7.1.2 and 8.3.

CNT6 and CNT7 active count value can be read via $I^2C$. However, it is possible to change the counter value for any macrocell using $I^2C$ write commands. In this mode, it is possible to load count data immediately (plus two clock cycles) or after counter ends counting. See Section 15.5.4 for further details.

### 8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

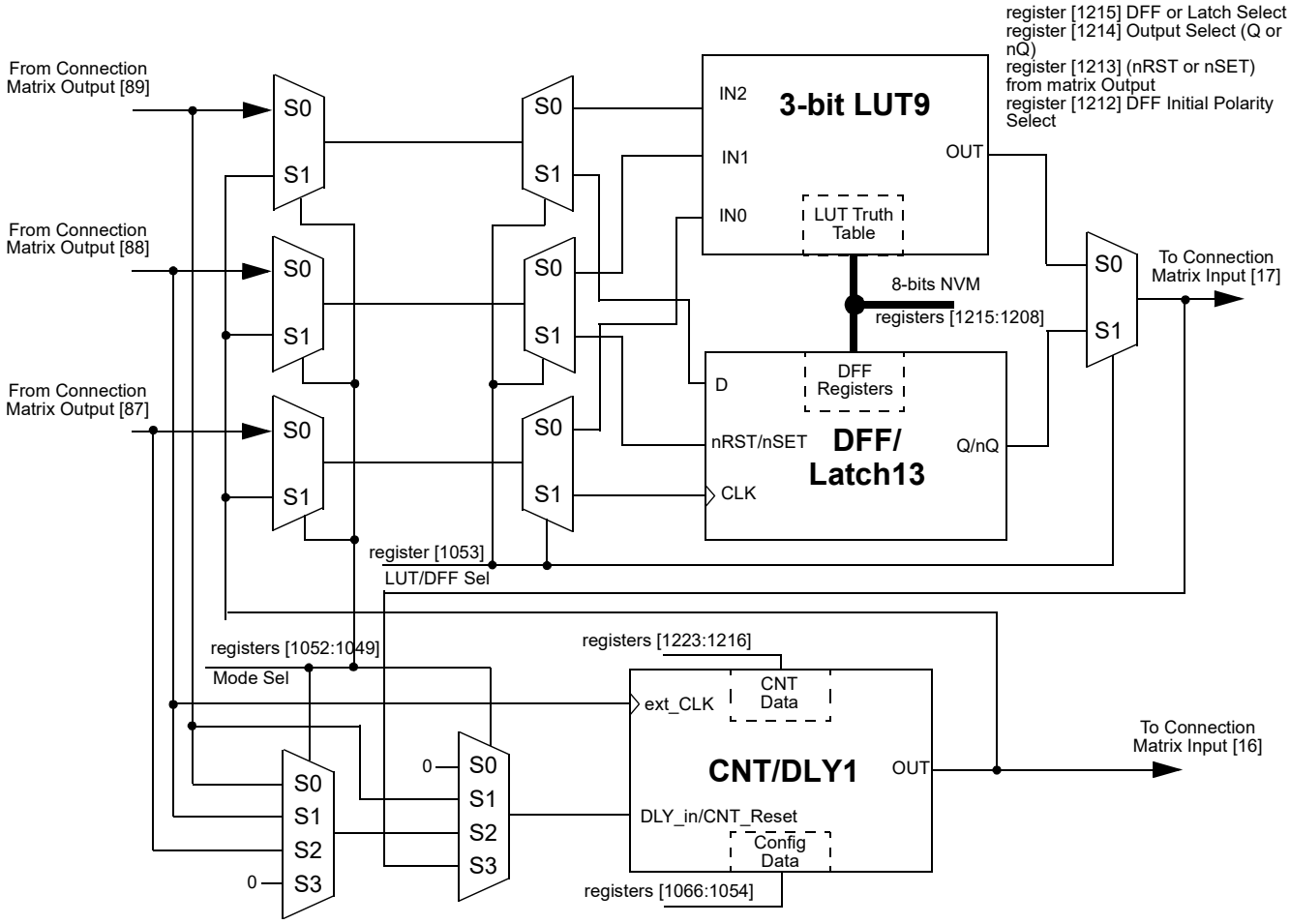



**Figure 32: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY1)**

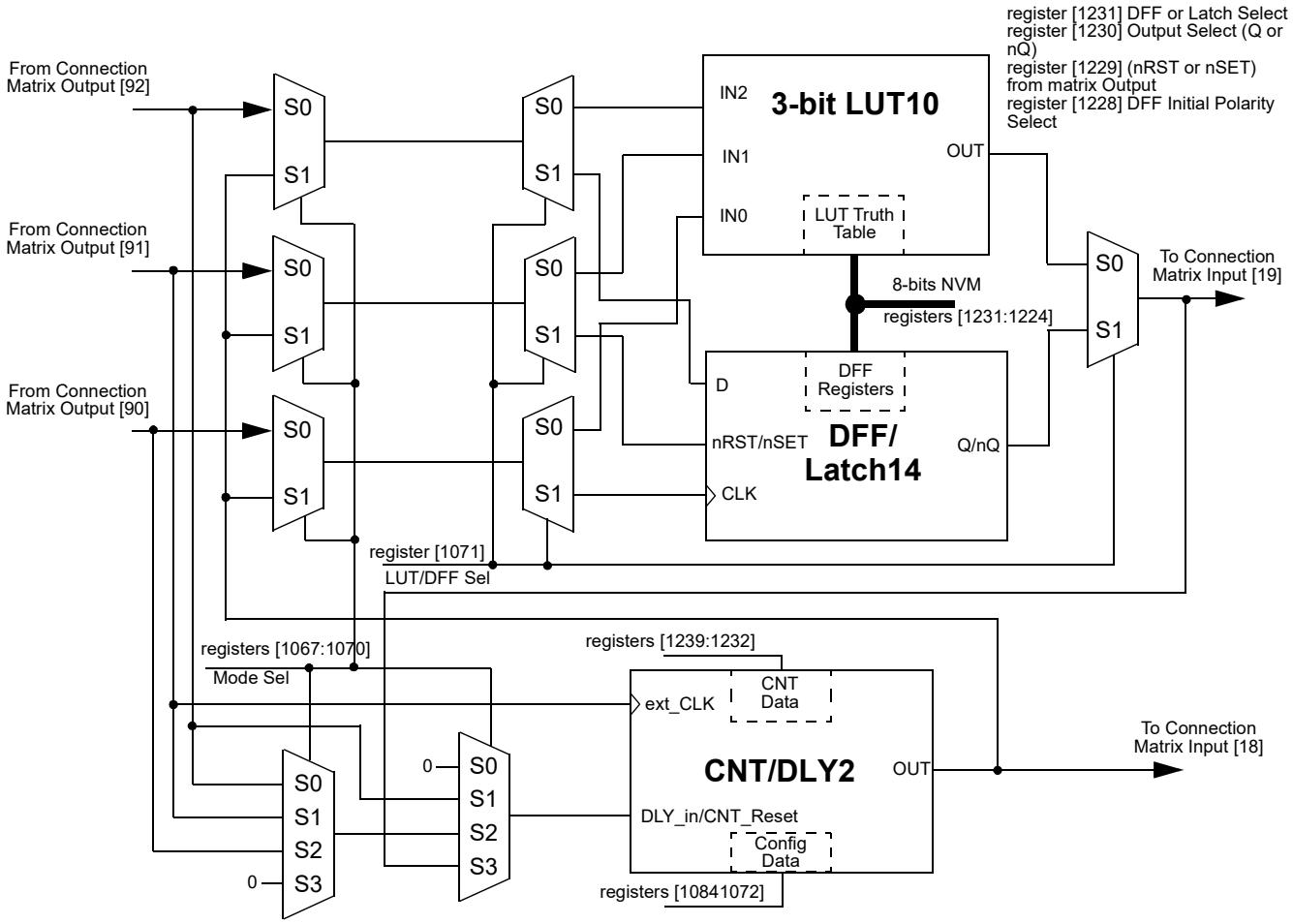



**Figure 33: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY2)**

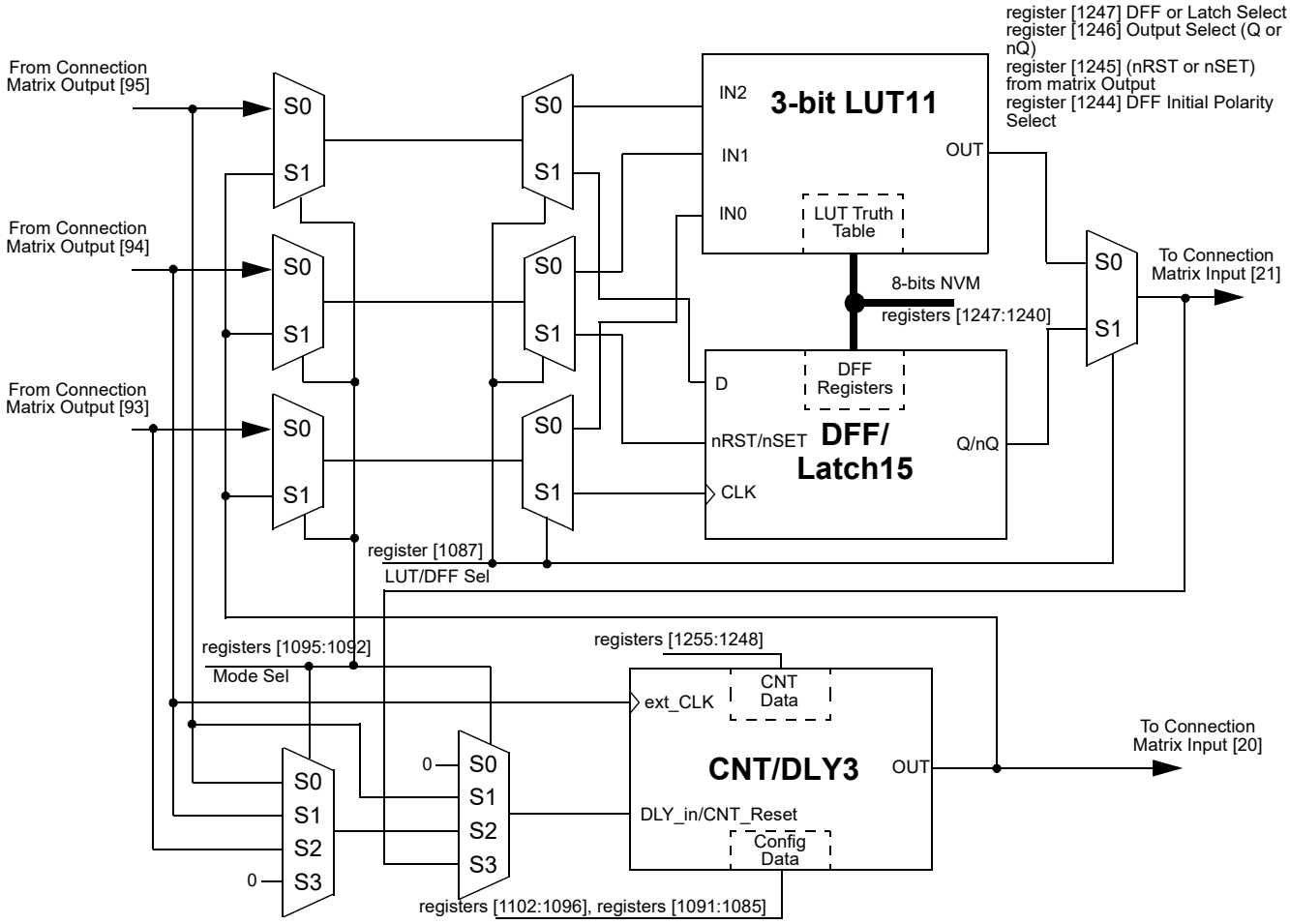



**Figure 34: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY3)**

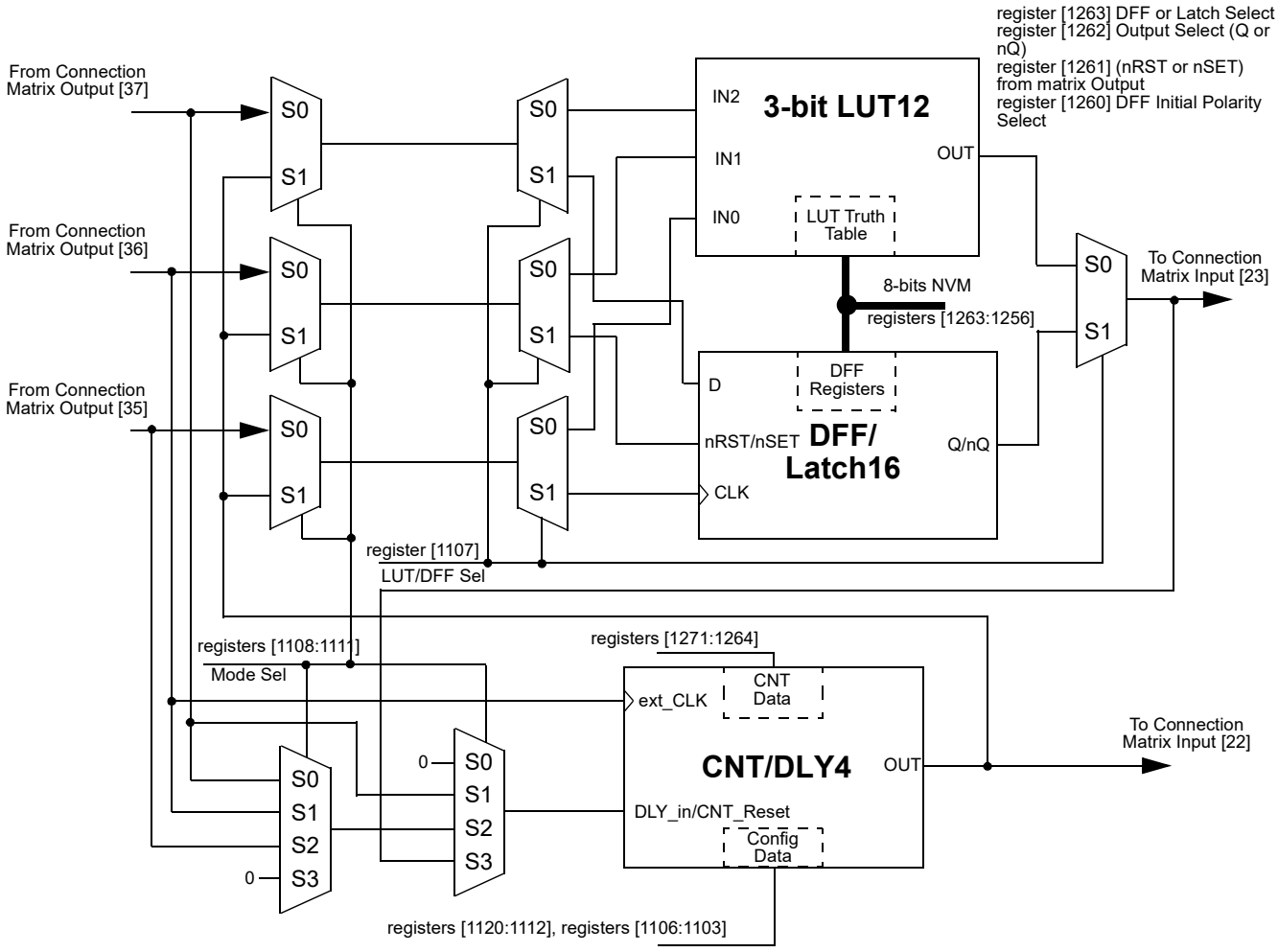



**Figure 35: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY4)**

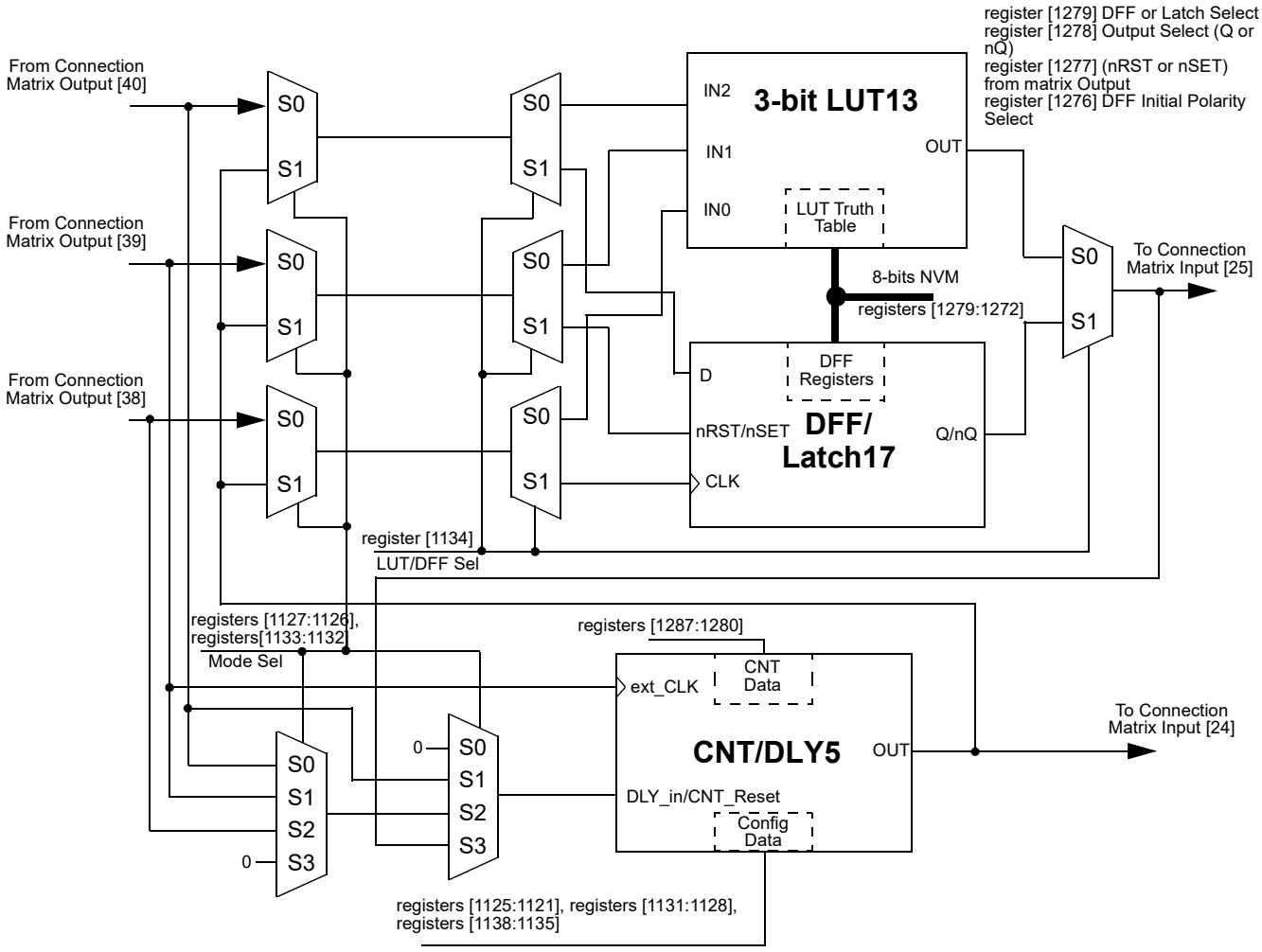



**Figure 36: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF17, CNT/DLY5)**

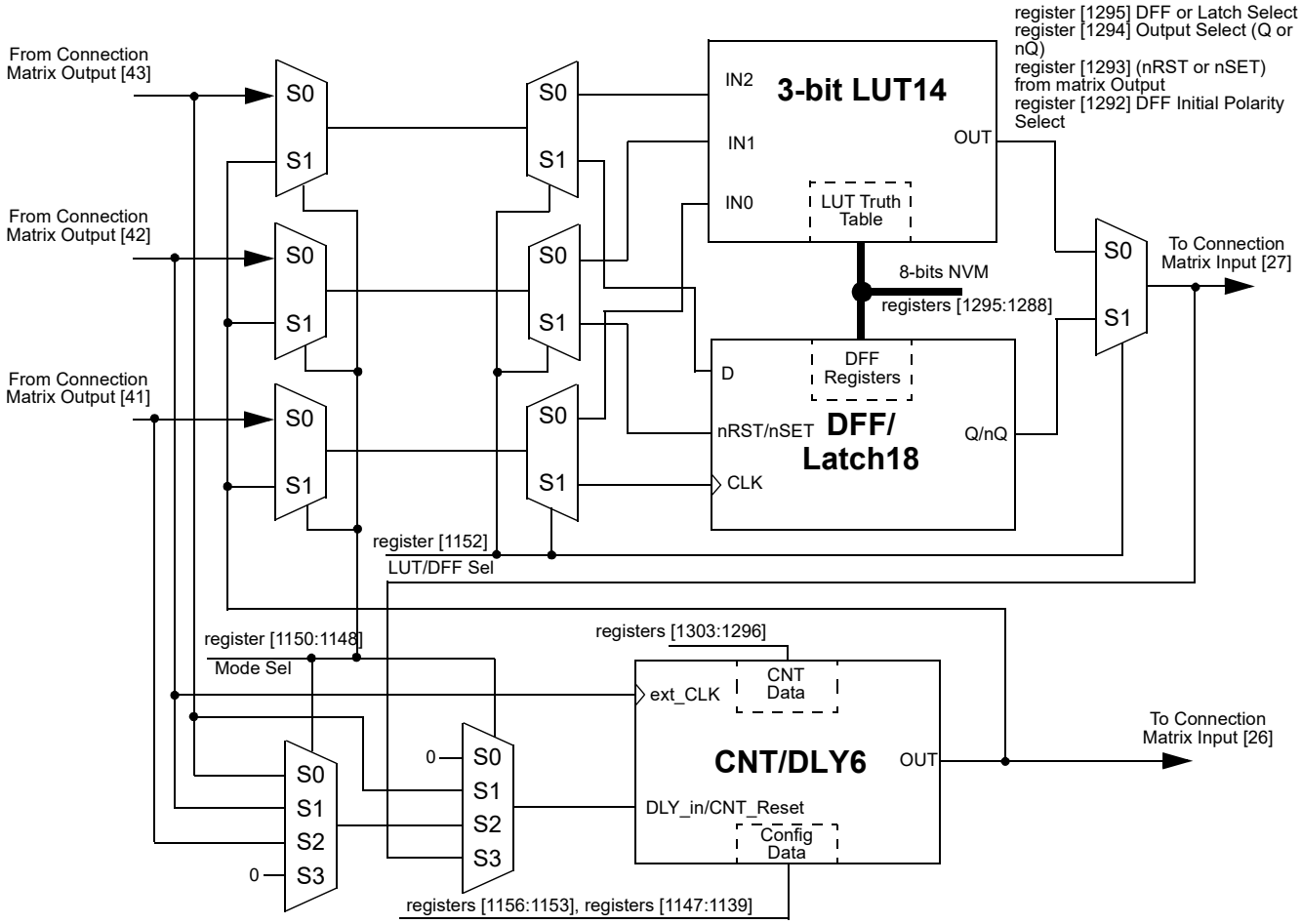



**Figure 37: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT14/DFF18, CNT/DLY6)**

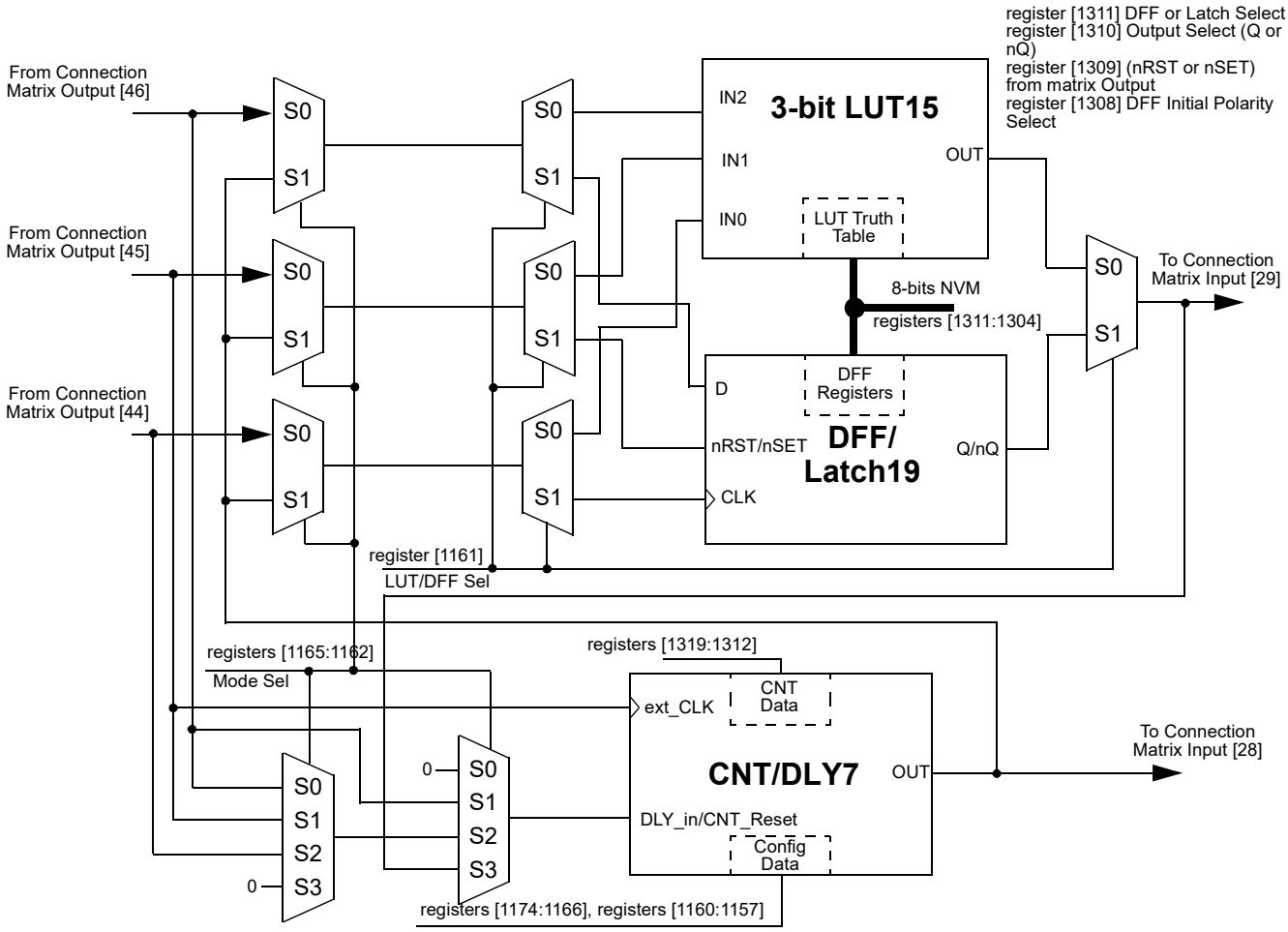



**Figure 38: 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT15/DFF19, CNT/DLY7)**

As shown in Figures 24-30 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

**Note:** It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF Two input signals from the connection matrix go to CND/DLY's inputs (in and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

### 8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

**Table 42: 3-bit LUT9 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1208] | LSB |
| 0 | 0 | 1 | register [1209] | |
| 0 | 1 | 0 | register [1210] | |
| 0 | 1 | 1 | register [1211] | |
| 1 | 0 | 0 | register [1212] | |
| 1 | 0 | 1 | register [1213] | |
| 1 | 1 | 0 | register [1214] | |
| 1 | 1 | 1 | register [1215] | MSB |

**Table 43: 3-bit LUT10 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1224] | LSB |
| 0 | 0 | 1 | register [1225] | |
| 0 | 1 | 0 | register [1226] | |
| 0 | 1 | 1 | register [1227] | |
| 1 | 0 | 0 | register [1228] | |
| 1 | 0 | 1 | register [1229] | |
| 1 | 1 | 0 | register [1230] | |
| 1 | 1 | 1 | register [1231] | MSB |

**Table 44: 3-bit LUT11 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1240] | LSB |
| 0 | 0 | 1 | register [1241] | |
| 0 | 1 | 0 | register [1242] | |
| 0 | 1 | 1 | register [1243] | |
| 1 | 0 | 0 | register [1244] | |
| 1 | 0 | 1 | register [1245] | |
| 1 | 1 | 0 | register [1246] | |
| 1 | 1 | 1 | register [1247] | MSB |

**Table 45: 3-bit LUT12 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1256] | LSB |
| 0 | 0 | 1 | register [1257] | |
| 0 | 1 | 0 | register [1258] | |
| 0 | 1 | 1 | register [1259] | |
| 1 | 0 | 0 | register [1260] | |
| 1 | 0 | 1 | register [1261] | |
| 1 | 1 | 0 | register [1262] | |
| 1 | 1 | 1 | register [1263] | MSB |

**Table 46: 3-bit LUT13 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1272] | LSB |
| 0 | 0 | 1 | register [1273] | |
| 0 | 1 | 0 | register [1274] | |
| 0 | 1 | 1 | register [1275] | |
| 1 | 0 | 0 | register [1276] | |
| 1 | 0 | 1 | register [1277] | |
| 1 | 1 | 0 | register [1278] | |
| 1 | 1 | 1 | register [1280] | MSB |

**Table 47: 3-bit LUT14 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1288] | LSB |
| 0 | 0 | 1 | register [1289] | |
| 0 | 1 | 0 | register [1290] | |
| 0 | 1 | 1 | register [1291] | |
| 1 | 0 | 0 | register [1292] | |
| 1 | 0 | 1 | register [1293] | |
| 1 | 1 | 0 | register [1294] | |
| 1 | 1 | 1 | register [1295] | MSB |

**Table 48: 3-bit LUT15 Truth Table**

| IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | register [1304] | LSB |
| 0 | 0 | 1 | register [1305] | |
| 0 | 1 | 0 | register [1306] | |
| 0 | 1 | 1 | register [1307] | |
| 1 | 0 | 0 | register [1308] | |
| 1 | 0 | 1 | register [1309] | |
| 1 | 1 | 0 | register [1310] | |
| 1 | 1 | 1 | register [1311] | MSB |

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

*3-Bit LUT9 is defined by registers [1215:1208]*

*3-Bit LUT10 is defined by registers [1231:1224]*

*3-Bit LUT11 is defined by registers [1247:1240]*

*3-Bit LUT12 is defined by registers [1263:1256]*

*3-Bit LUT13 is defined by registers [1279:1272]*

*3-Bit LUT14 is defined by registers [1295:1288]*

*3-Bit LUT15 is defined by registers [1311:1304]*

### 8.2 4-BIT LUT OR DFF/LATCH WITH 16-BIT COUNTER/DELAY MACROCELL

There is one macrocell that can serve as either 4-bit LUT or as 16-bit Counter/Delay. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (ext_CLK) and reset (DLY_in/CNT_Reset) for th counter/delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.
This macrocell can also operate in a frequency detection or edge detection mode.
This macrocell can have its active count value read via $I^2C$. See Section 15.5.4 for further details.

### 8.2.1 4-Bit LUT or DFF/Latch with 16-Bit CNT/DLY Block Diagram

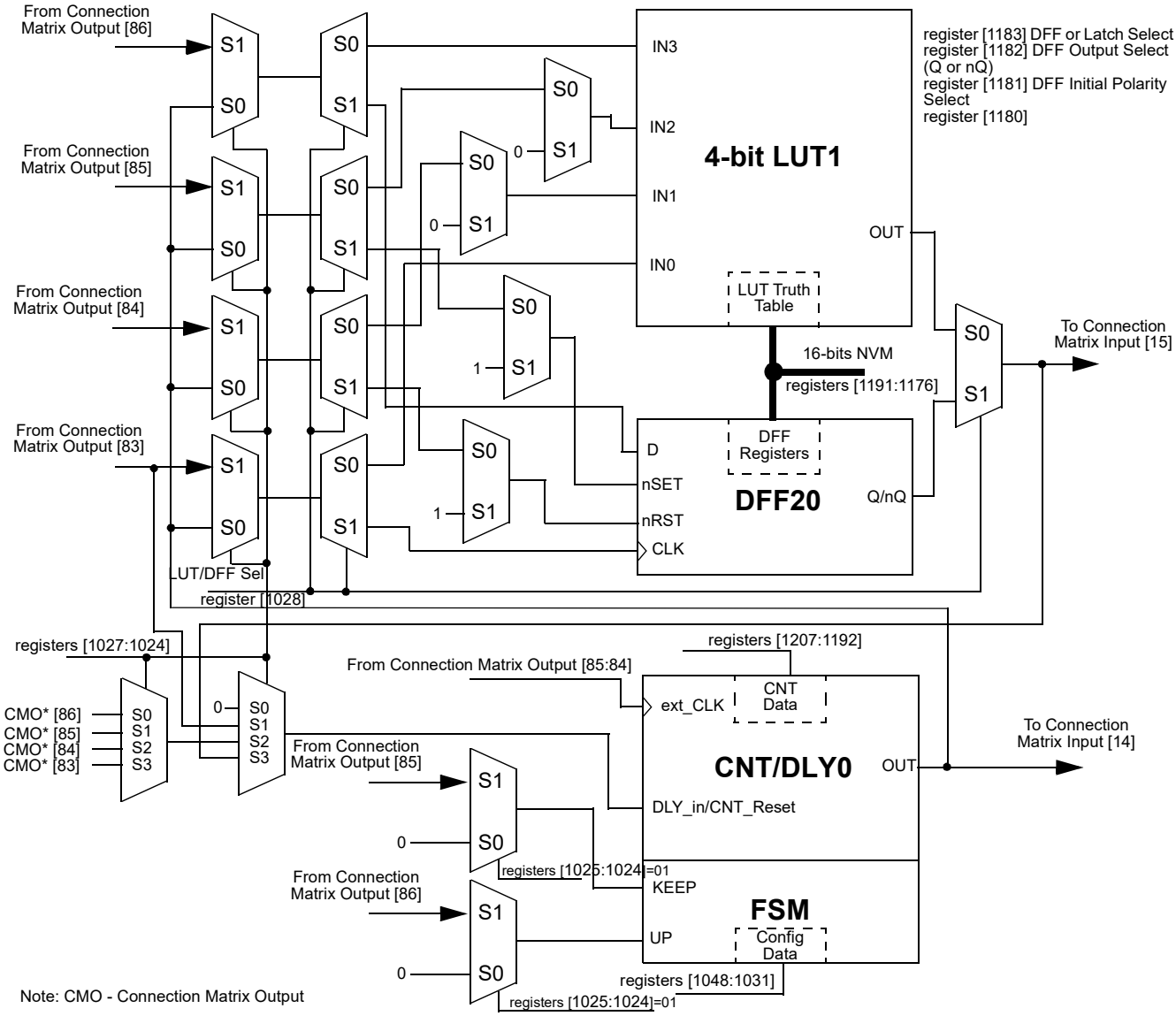



**Figure 39: 4-bit LUT1 or CNT/DLY0**

### 8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

**Table 49: 4-bit LUT1 Truth Table**

| IN3 | IN2 | IN1 | IN0 | OUT | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | register [1176] | LSB |
| 0 | 0 | 0 | 1 | register [1177] | |
| 0 | 0 | 1 | 0 | register [1178] | |
| 0 | 0 | 1 | 1 | register [1179] | |
| 0 | 1 | 0 | 0 | register [1180] | |
| 0 | 1 | 0 | 1 | register [1181] | |
| 0 | 1 | 1 | 0 | register [1182] | |
| 0 | 1 | 1 | 1 | register [1183] | |
| 1 | 0 | 0 | 0 | register [1184] | |
| 1 | 0 | 0 | 1 | register [1185] | |
| 1 | 0 | 1 | 0 | register [1186] | |
| 1 | 0 | 1 | 1 | register [1187] | |
| 1 | 1 | 0 | 0 | register [1188] | |
| 1 | 1 | 0 | 1 | register [1189] | |
| 1 | 1 | 1 | 0 | register [1190] | |
| 1 | 1 | 1 | 1 | register [1191] | MSB |

This Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

*4-Bit LUT1 is defined by registers [1191:1176]*

**Table 50: 4-bit LUT Standard Digital Functions**

| Function | MSB | | | | | | | | | | | | | | | LSB |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AND-4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| NAND-4 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| OR-4 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| NOR-4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOR-4 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| XNOR-4 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

### 8.3 CNT/DLY/FSM TIMING DIAGRAMS

#### 8.3.1 Delay Mode (Edge Select: Both, Counter Data: 3) CNT/DLY2 to CNT/DLY6

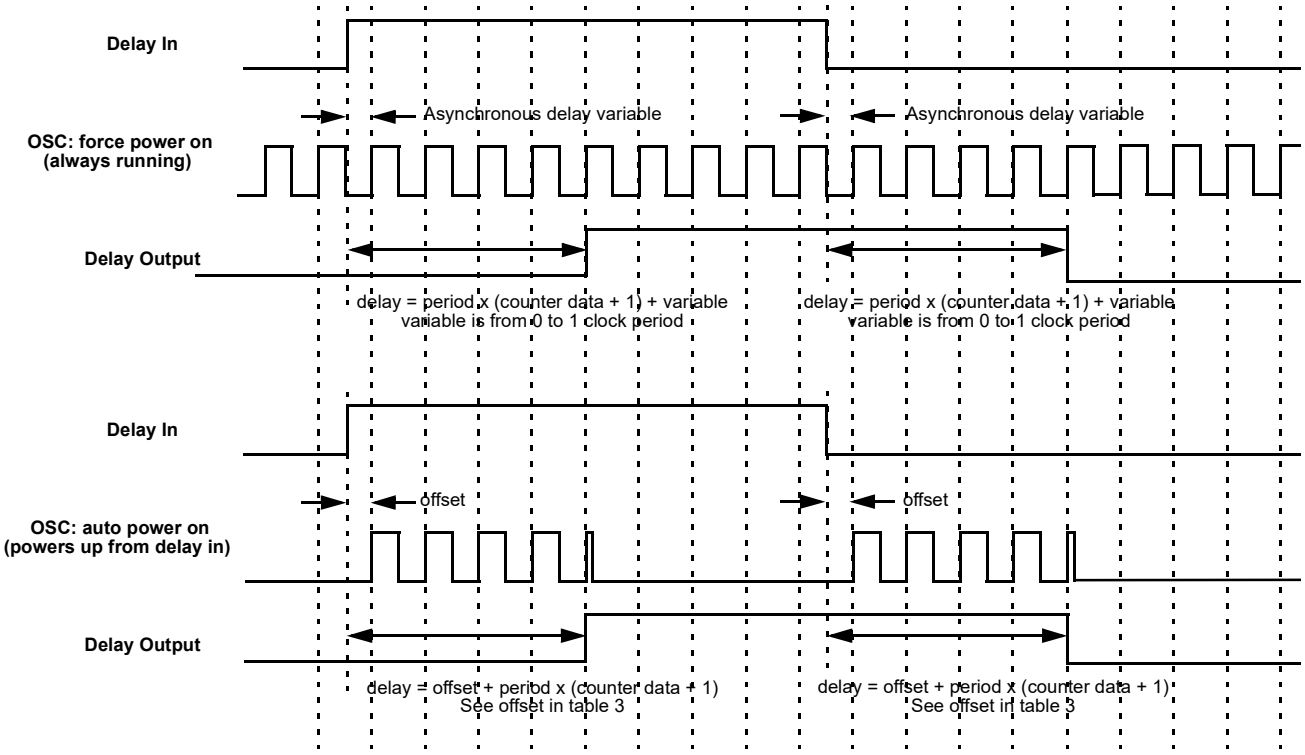



**Figure 40: Delay Mode Timing Diagram**

#### 8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2 to CNT/DLY6

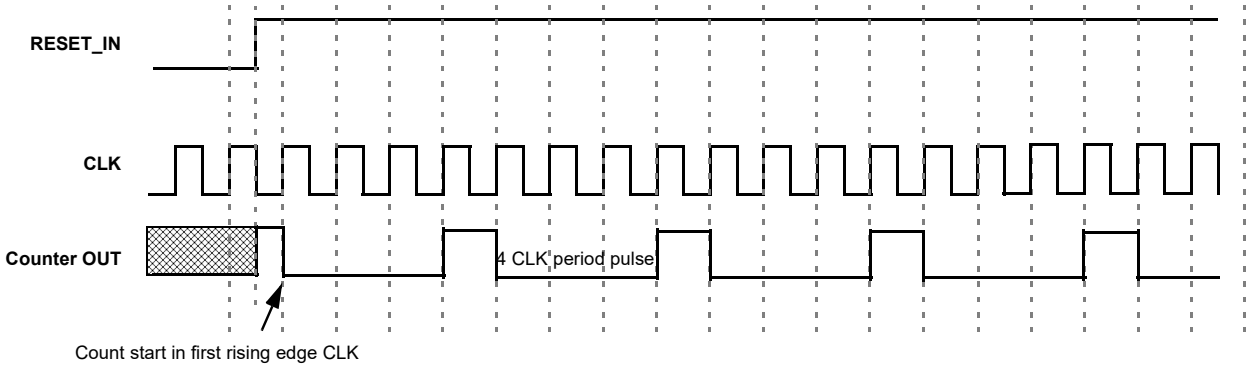



**Figure 41: Counter Mode Timing Diagram without Two DFFs Synced up**

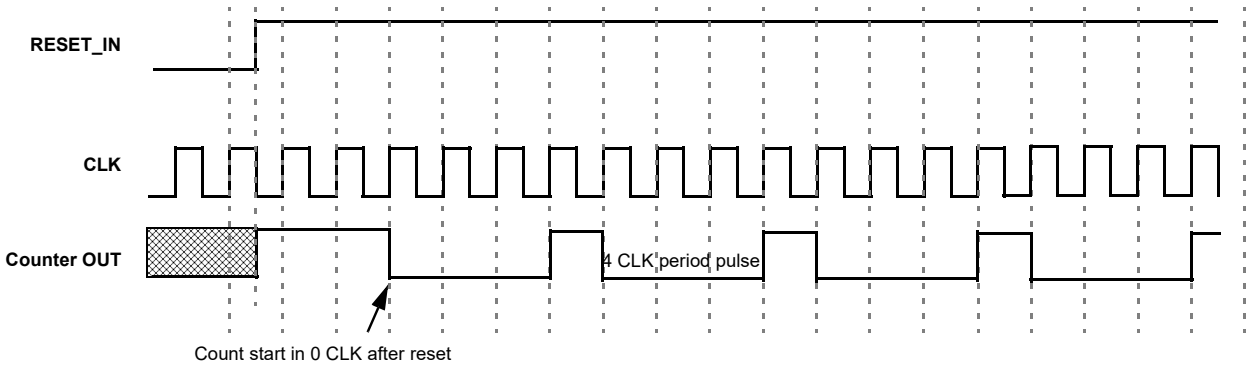



**Figure 42: Counter Mode Timing Diagram with Two DFFs Synced up**

### 8.3.3 One-shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

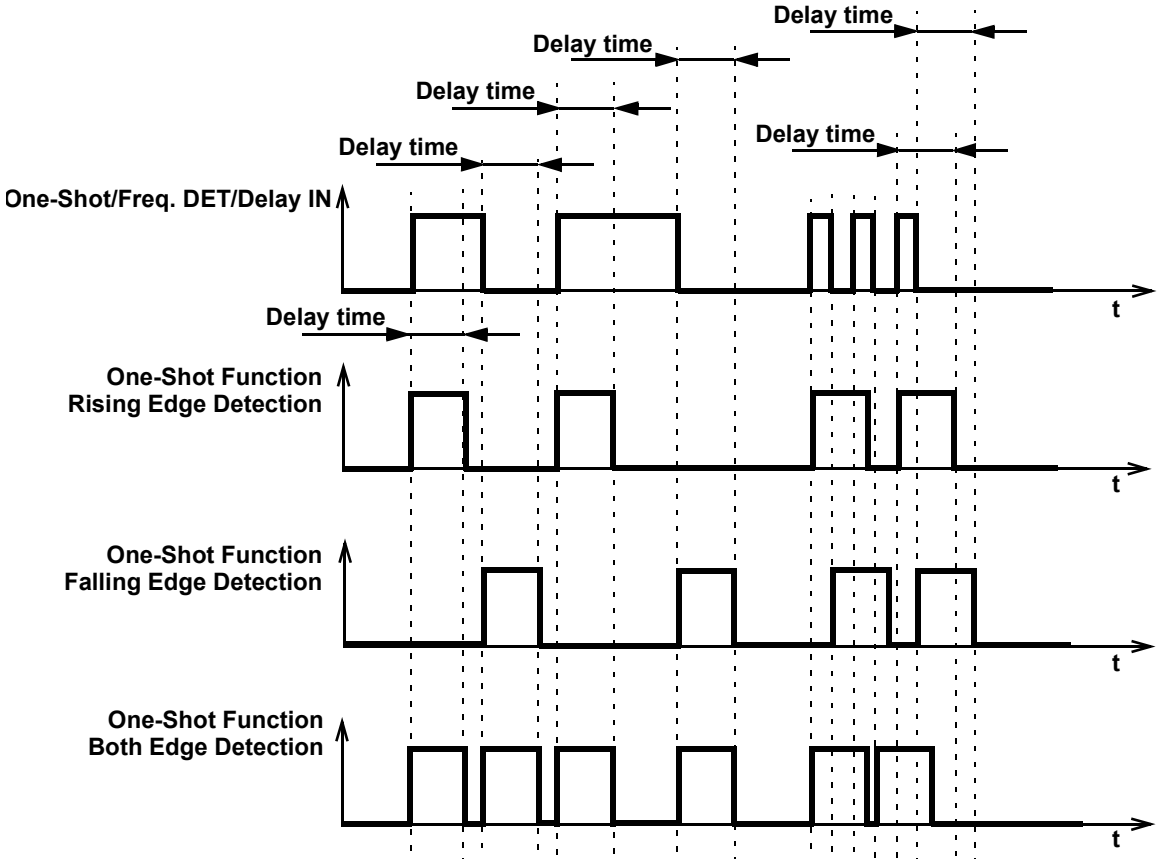



**Figure 43: One-Shot Function Timing Diagram**

This macrocell generates a high level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is high.

### 8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

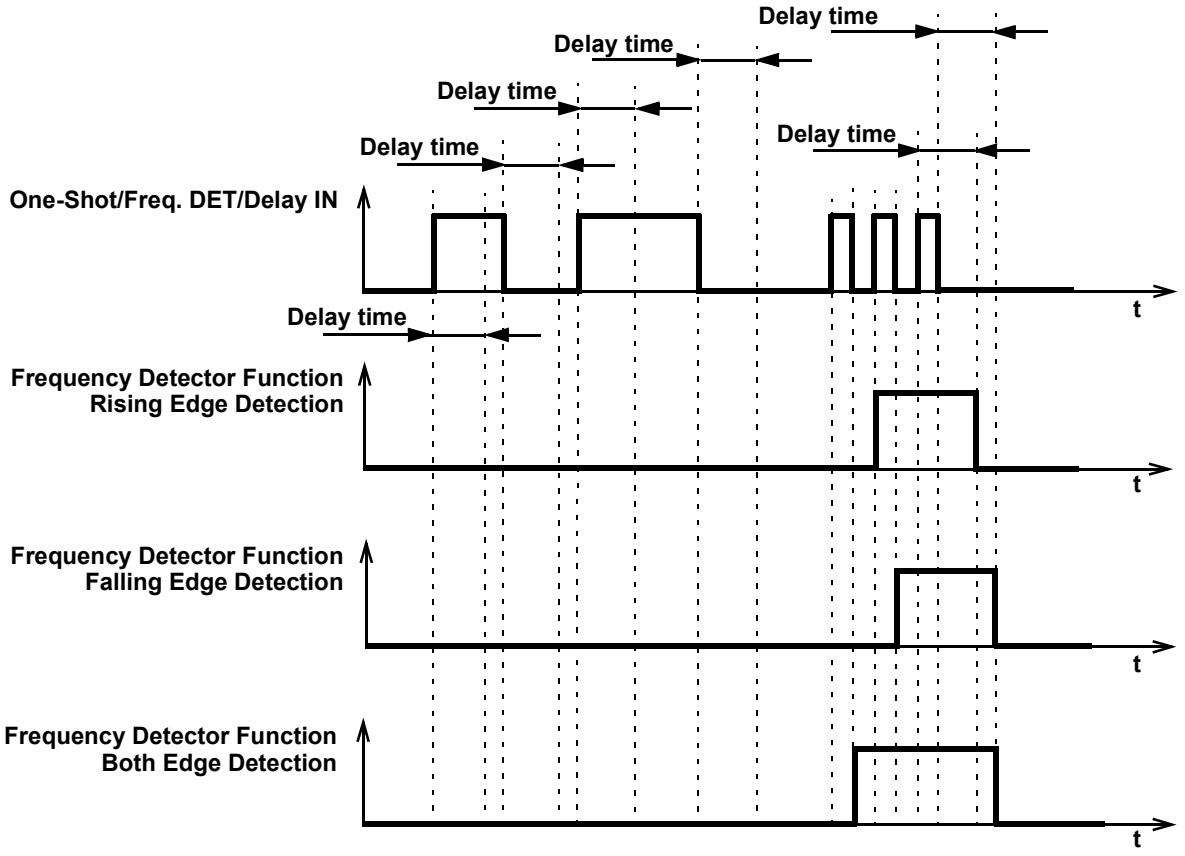



**Figure 44: Frequency Detection Mode Timing Diagram**

### 8.3.5 Edge Detection Mode CNT/DLY2 to CNT/DLY6

The macrocell generates high level short pulse when detecting the respective edge. See Table 9.

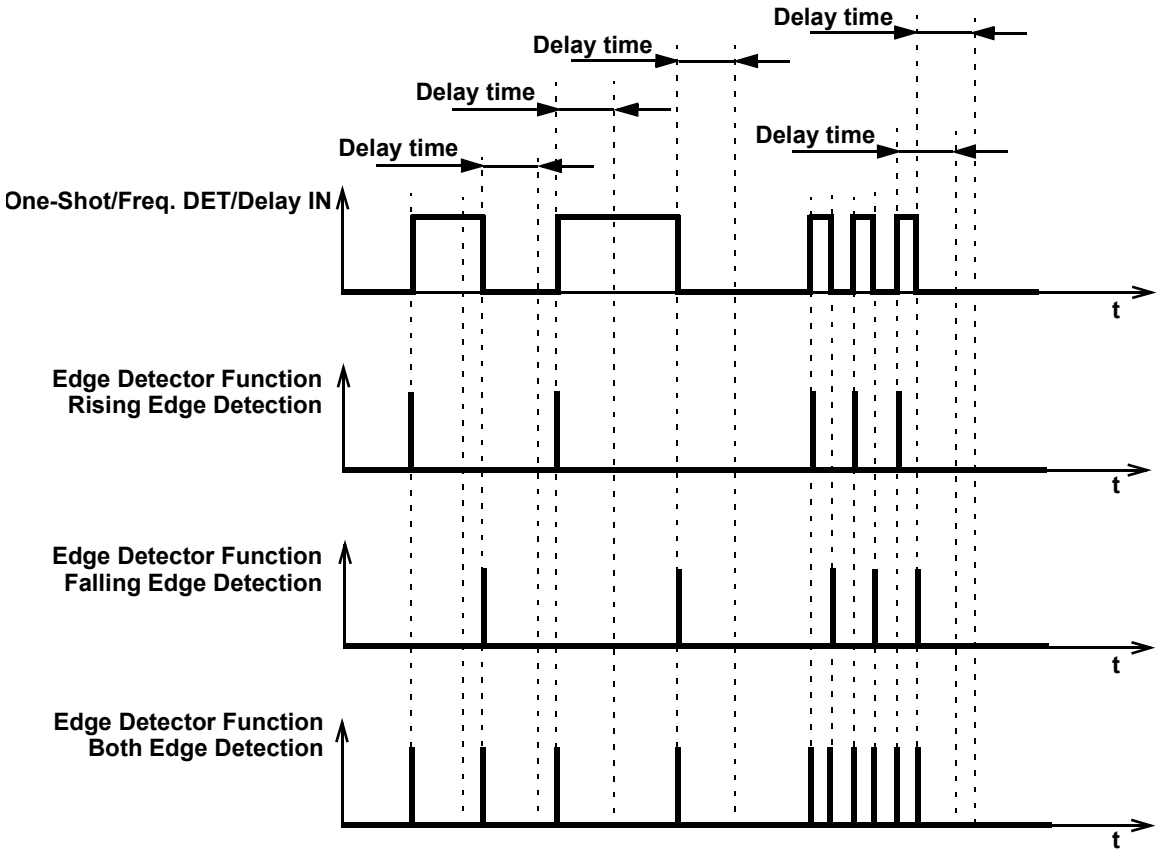



**Figure 45: Edge Detection Mode Timing Diagram**

### 8.3.6 Delayed Edge Detection Mode

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 46.

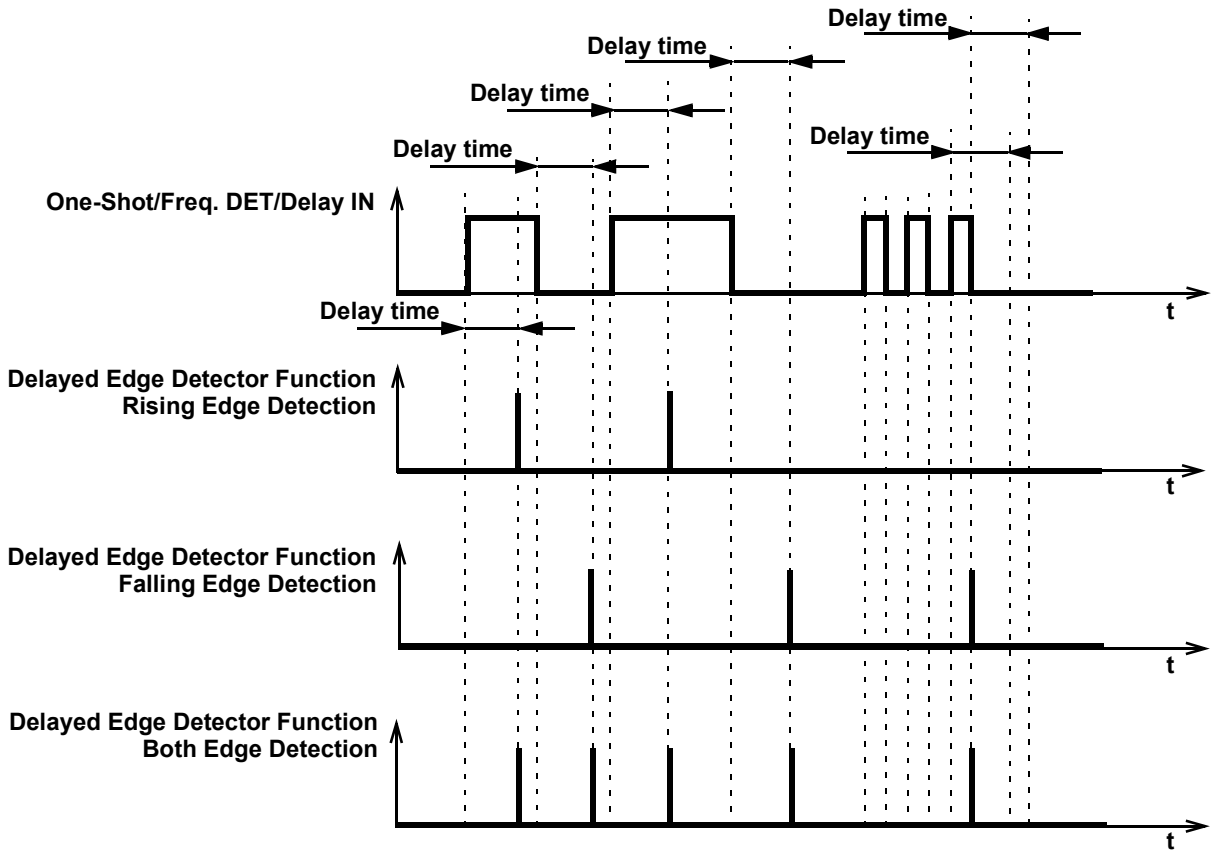



**Figure 46: Delayed Edge Detection Mode**

### 8.3.7 Delay Mode CNT/DLY0 to CNT/DLY6

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

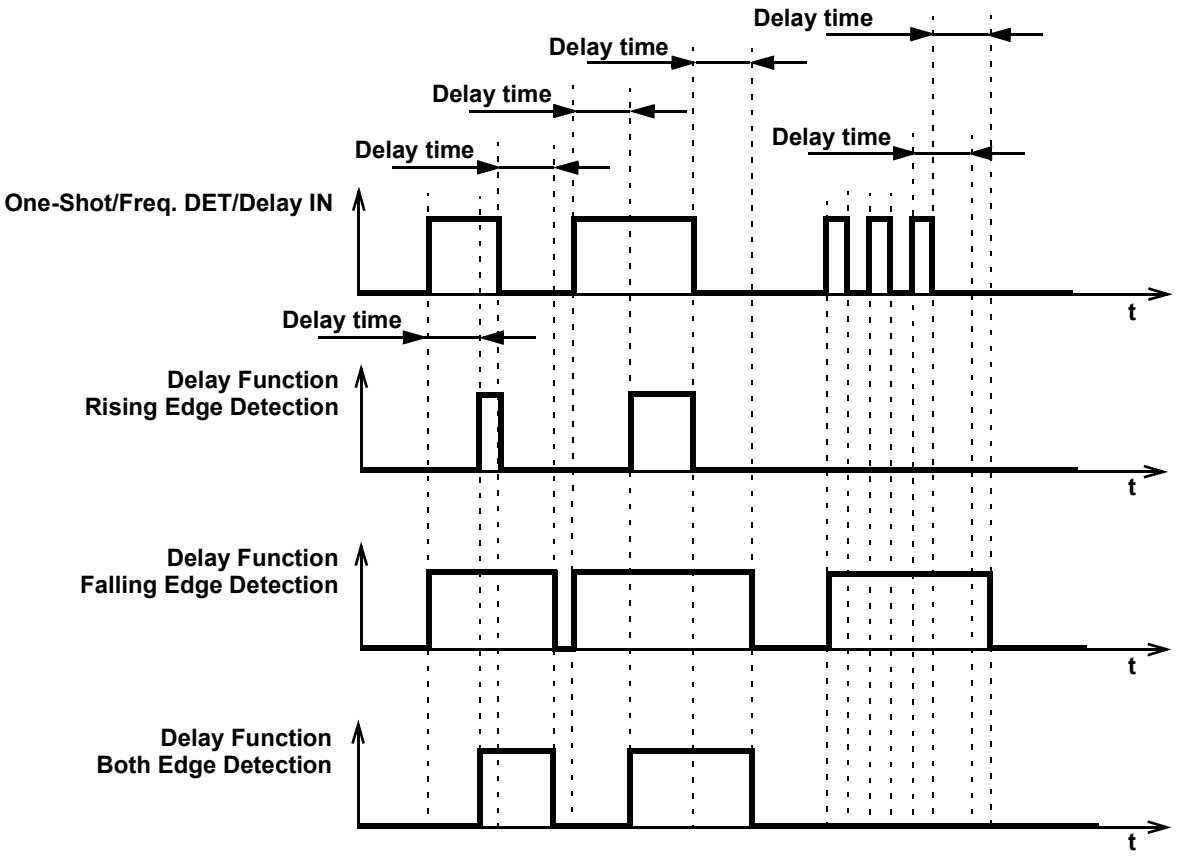



**Figure 47: Delay Mode Timing Diagram**

### 8.3.8 CNT/FSM Mode CNT/DLY0, CNT/DLY1

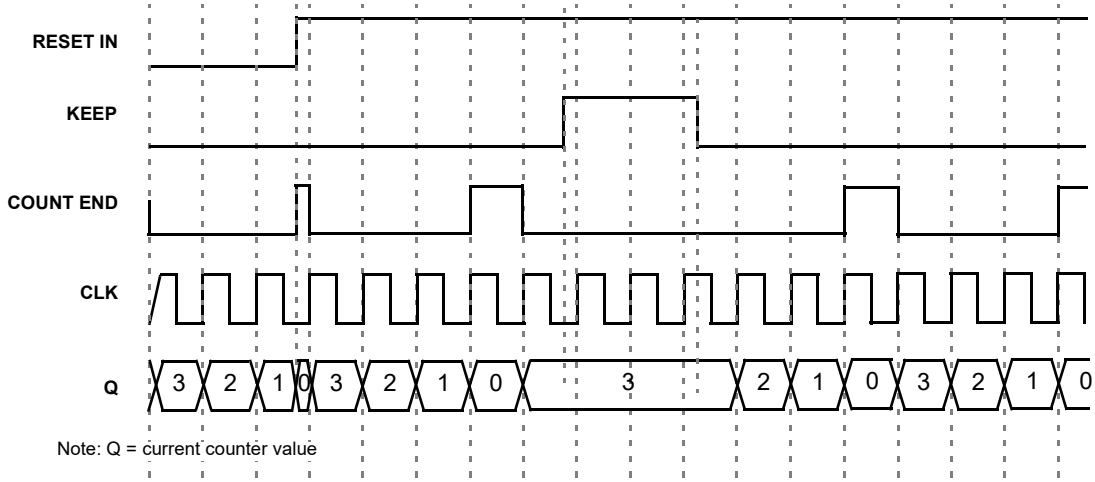



**Figure 48: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced on, UP=0) for Counter Data = 3**

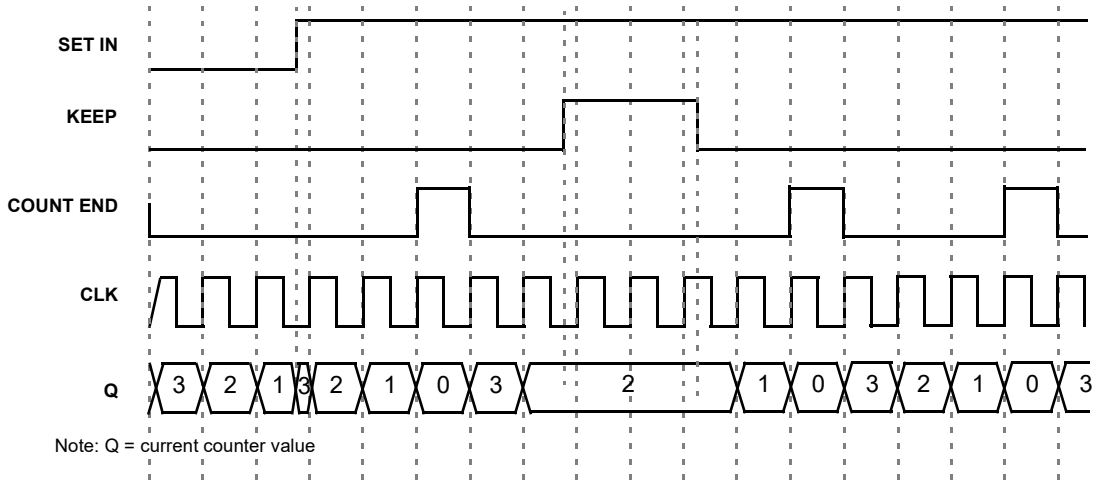



**Figure 49: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced on, UP=0) for Counter Data = 3**

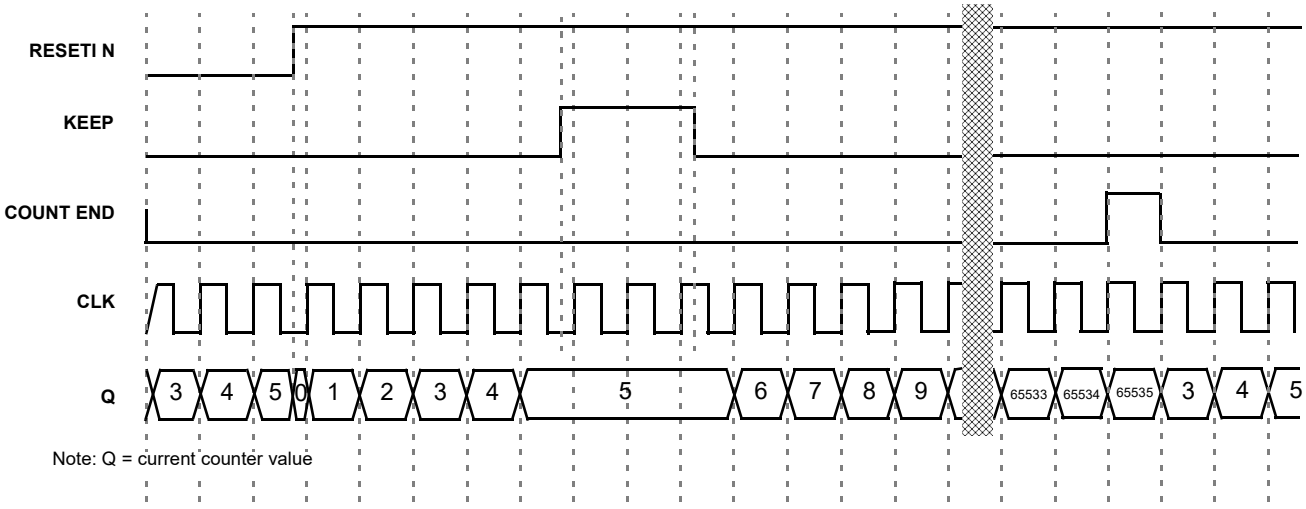



**Figure 50: CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced on, UP=1) for Counter Data = 3**

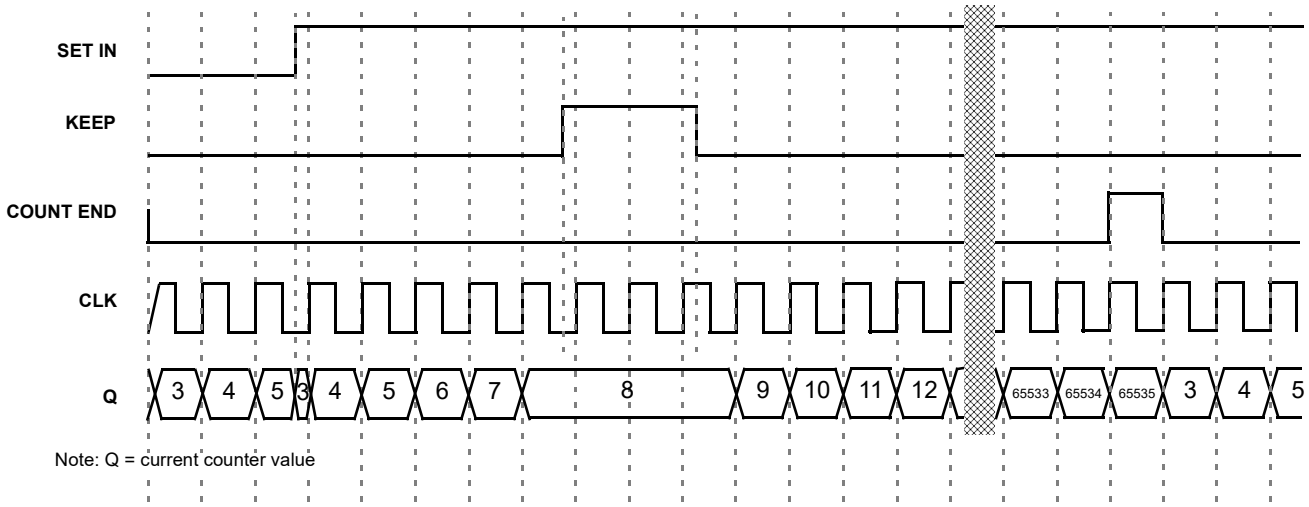



**Figure 51: CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP=1) for Counter Data = 3**

### 8.3.9 Difference in Counter Value for Counter, Delay, One-Shot and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 52.

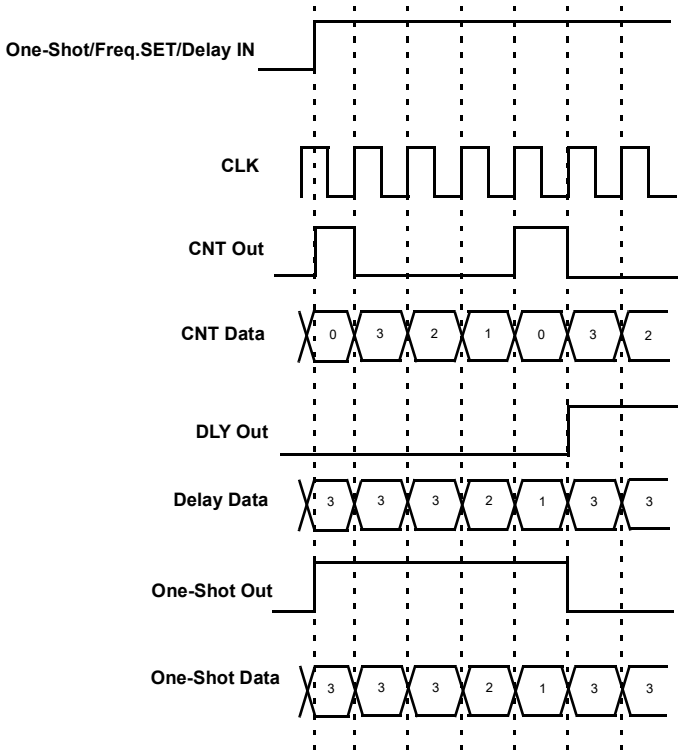



**Figure 52: Counter Value, Counter Data = 3**

### 8.4 WAKE AND SLEEP CONTROLLER

The SLG46867 has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1032:1031]=11 and register [1046]=1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

**Note 1:** BG/Analog_Good time is long and should be considered in wake and sleep timing in case it dynamically powers on/off.

**Note 2:** Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

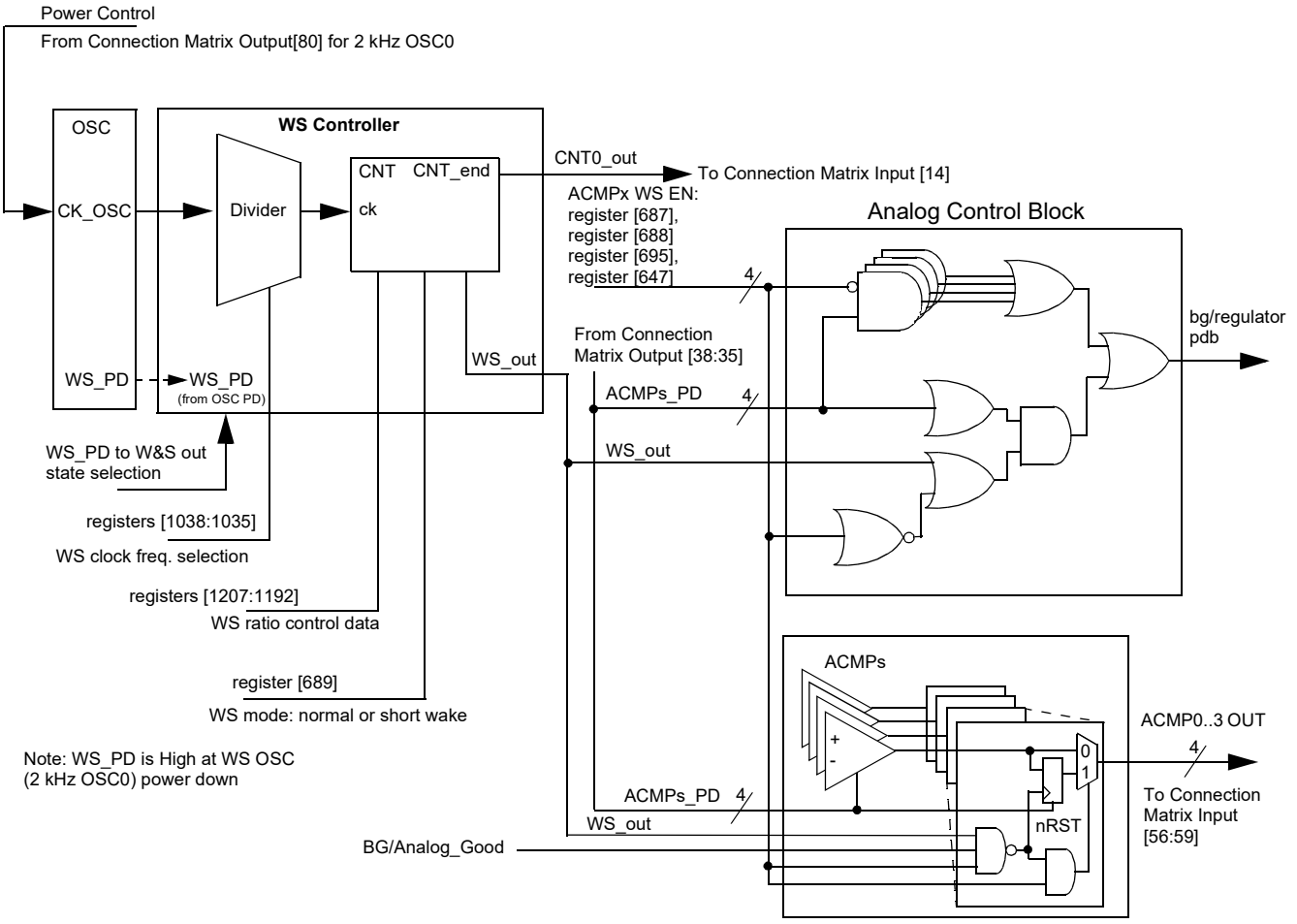
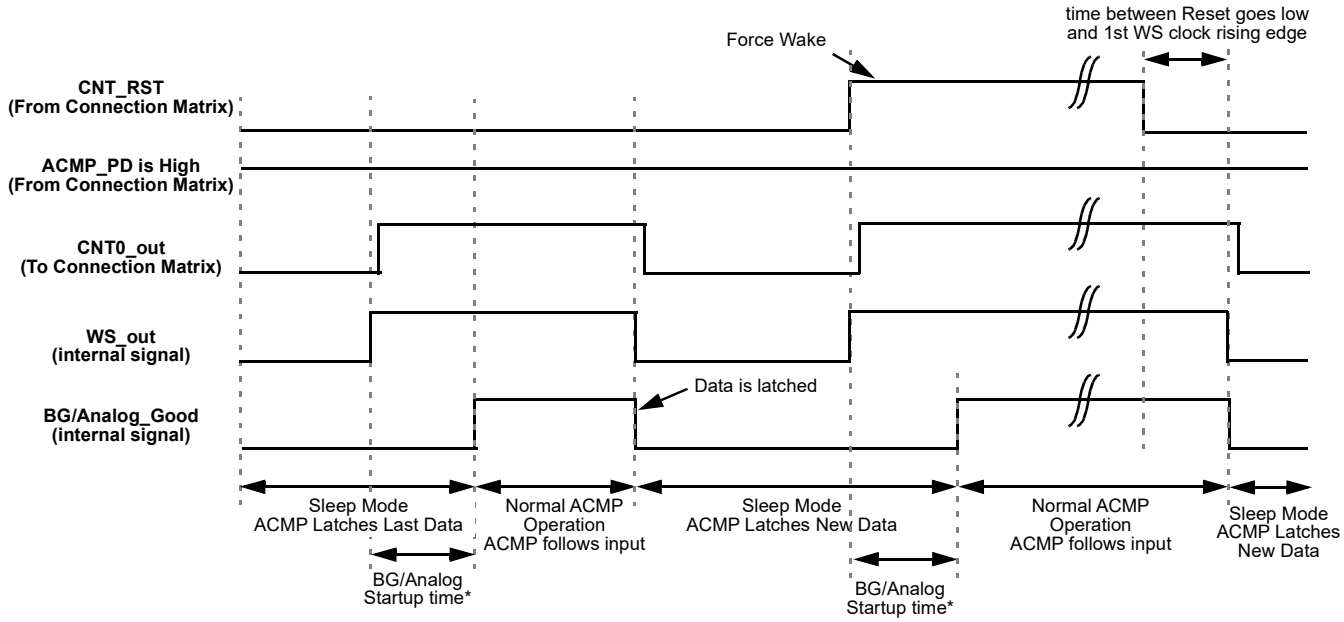
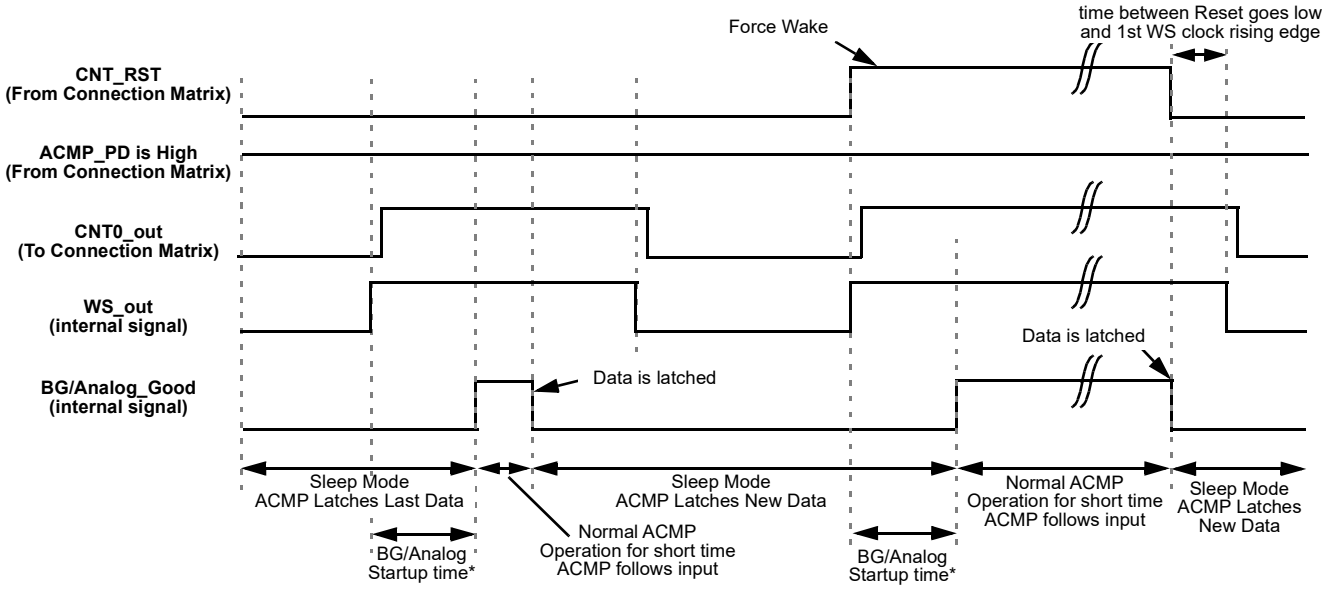



**Figure 53: Wake/Sleep Controller**



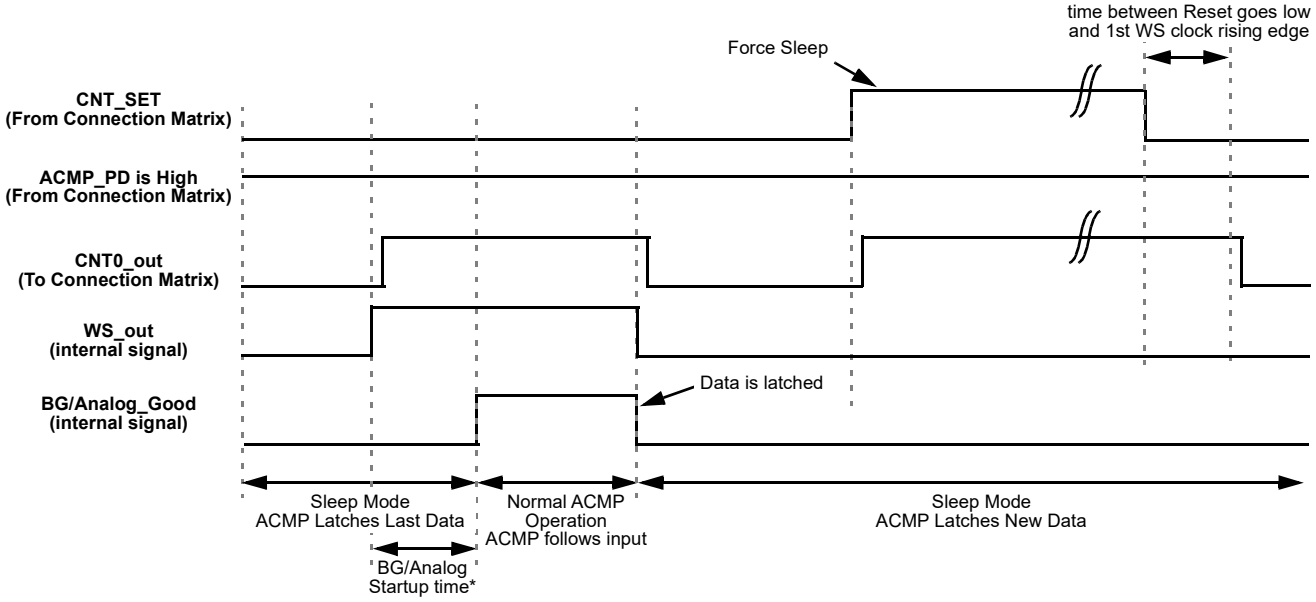

Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during latch.

**Figure 54: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used**



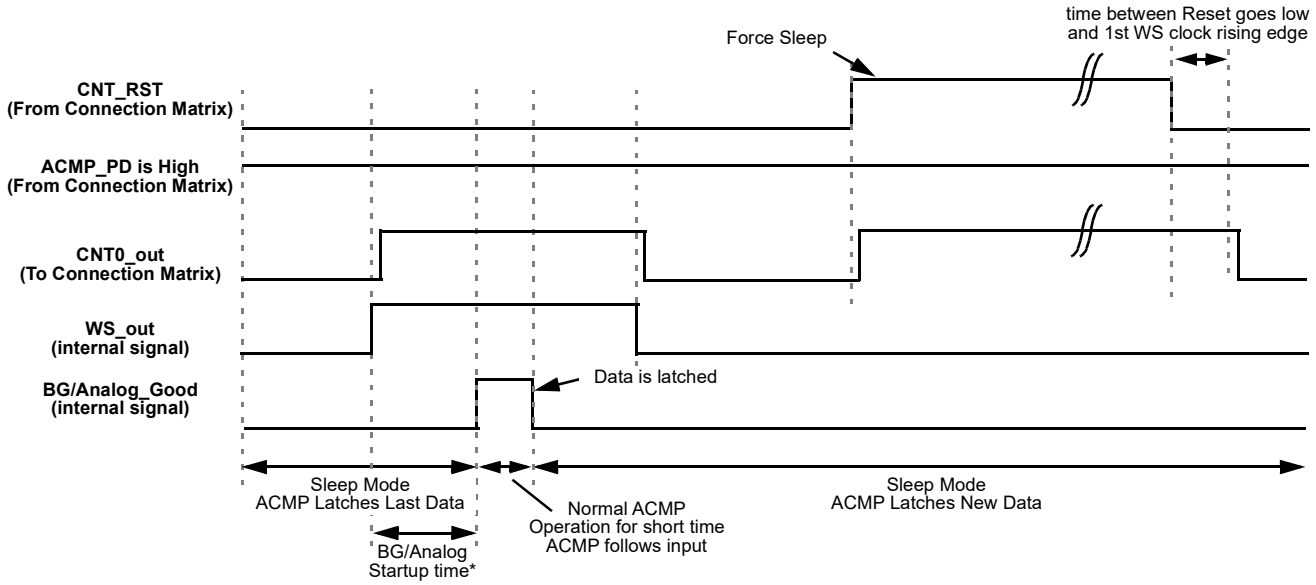

Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during latch.

**Figure 55: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used**




Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during latch.

**Figure 56: Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used**




Note: CNT0_out is a delayed WS_out signal for 1us to make sure the data is correct during latch.

**Figure 57: Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used**

**Note:** If low power BG is powered on/off by w/s, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 is recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The BG/analog start up time will

take maximal 450 us for ACMP0/1 and a shorter time for ACMP2/3. The short wake mode can be used to reduce the current consumption.

To use any ACMP under WS controller, the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMP);
- Register WS → enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMP).

The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.
  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMP until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMP while counter is counting up to the end.

**Note:** The OSC0 matrix power down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High

**Note:** Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

# 9 Analog Comparators

There are two High Speed and two Low Power Rail-to-Rail General Purpose Analog Comparators (ACMP) macrocells in the SLG46867. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H_pdb, ACMP1H_pdb, ACMP2L_pdb and ACMP3L_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

Two of the four General Purpose Analog Comparators are optimized for high speed operation (ACMP0H and ACMP1H), and two other are optimized for low power operation (ACMP2L and ACMP3L).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1X, 0.5X, 0.33X, 0.25X) before connection to the analog comparator. The gain divider is unbuffered and has input resistance of 2 MΩ (typ.) for 0.5X, 0.33X, 0.25X, and 100 MΩ for 1X. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by any external source (GPIO2). Note that the external Vref signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see Figure 58 to Figure 61.

Input bias current < 1 nA (typ).

PWR UP = 1 → ACMP is powered up.

PWR UP = 0 → ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid in 52 µs (max) after power up signal goes high for ACMP0H and ACMP1H, and becomes valid 325 µs (max) after power up signal goes high for ACMP2L and ACMP3L.

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV/32 mV/64 mV/192 mV.

ACMP0H IN+ options are GPIO4, buffered GPIO4, $V_{DD}$, 100 µA Current Source
ACMP1H IN+ options are GPIO5, buffered GPIO5, ACMP0H IN+ MUX output
ACMP2L IN+ options are GPIO6, ACMP0H IN+ MUX output, ACMP1H IN+ MUX output
ACMP3L IN+ options are GPIO7, ACMP2L IN+ MUX output, Temp Sensor OUT

### 9.1 ACMP0H BLOCK DIAGRAM

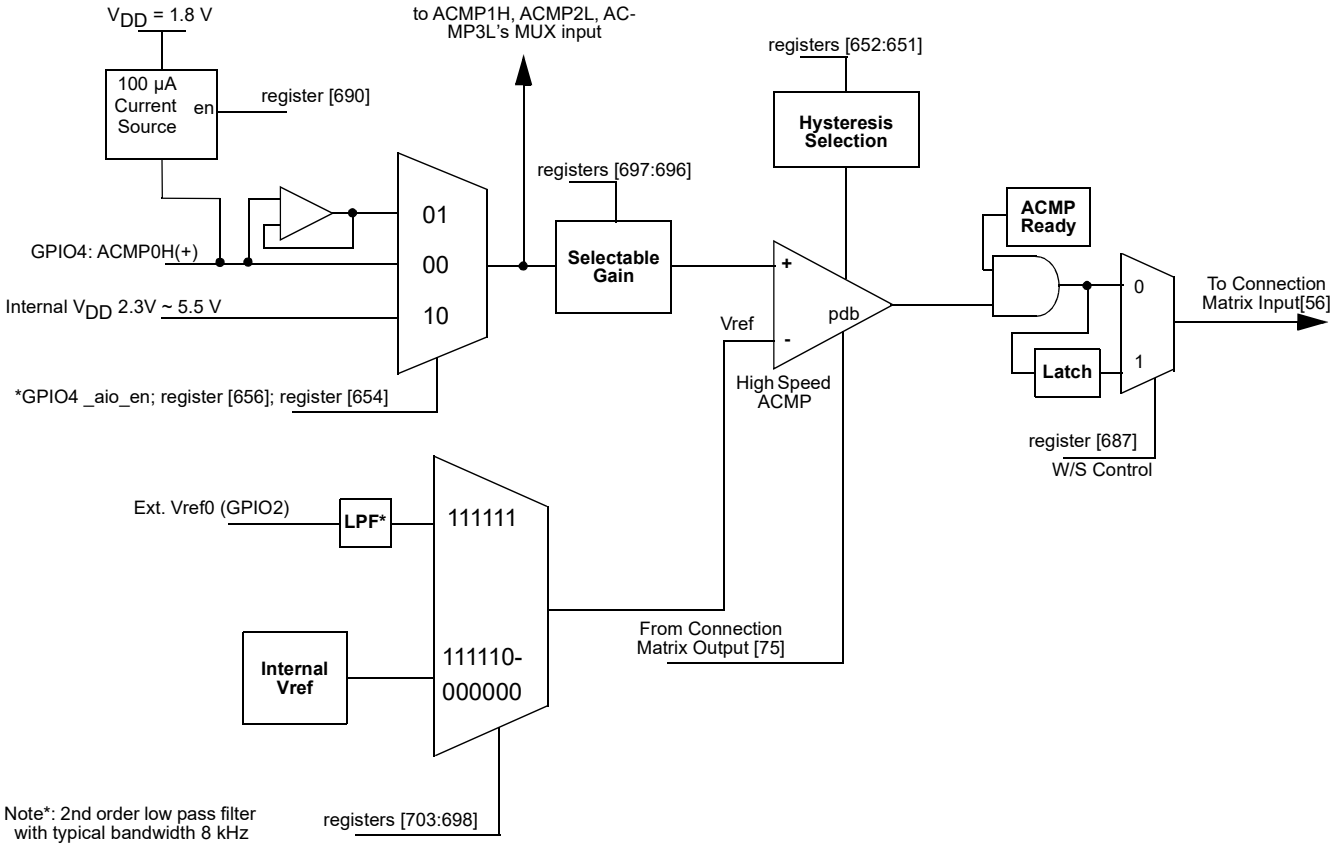



**Figure 58: ACMP0H Block Diagram**

### 9.2 ACMP1H BLOCK DIAGRAM

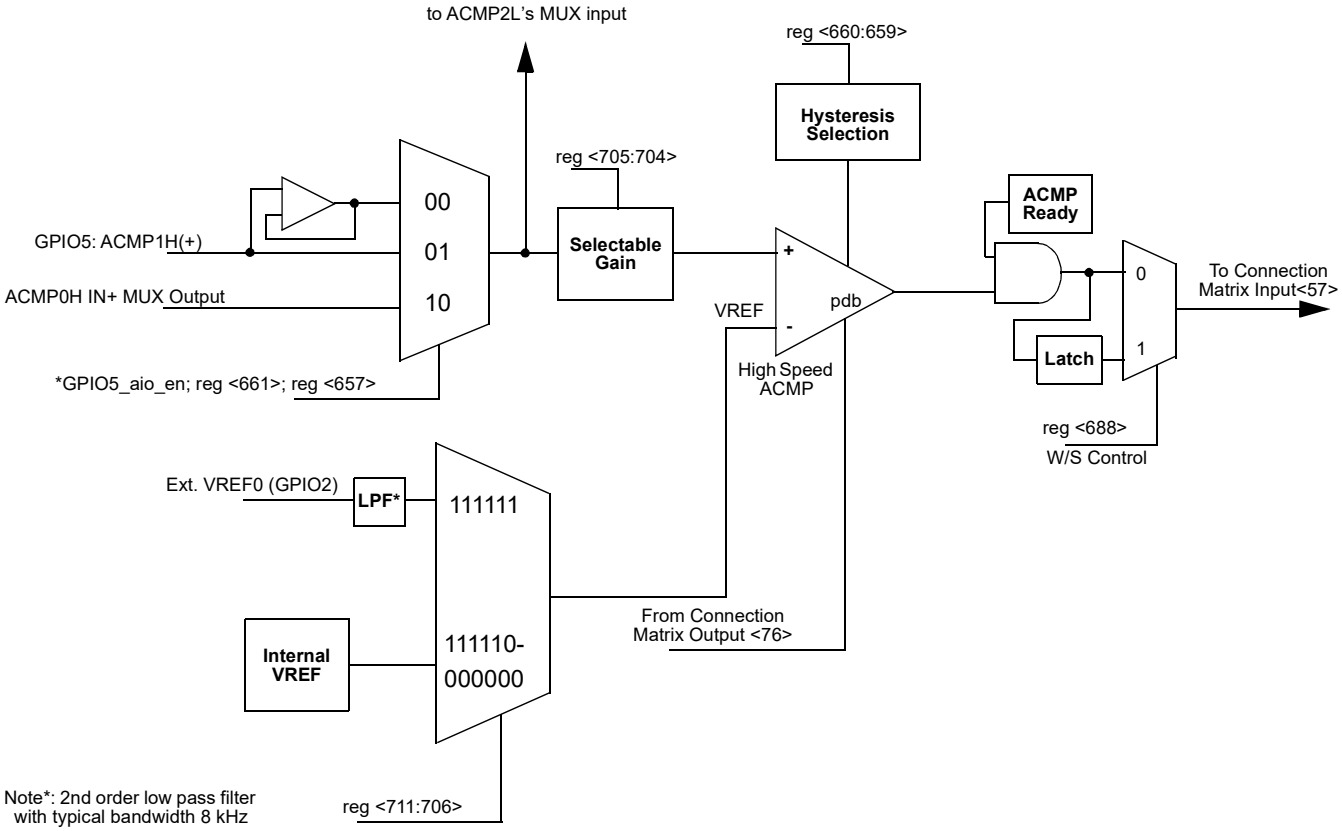



**Figure 59: ACMP1H Block Diagram**

### 9.3 ACMP2L BLOCK DIAGRAM

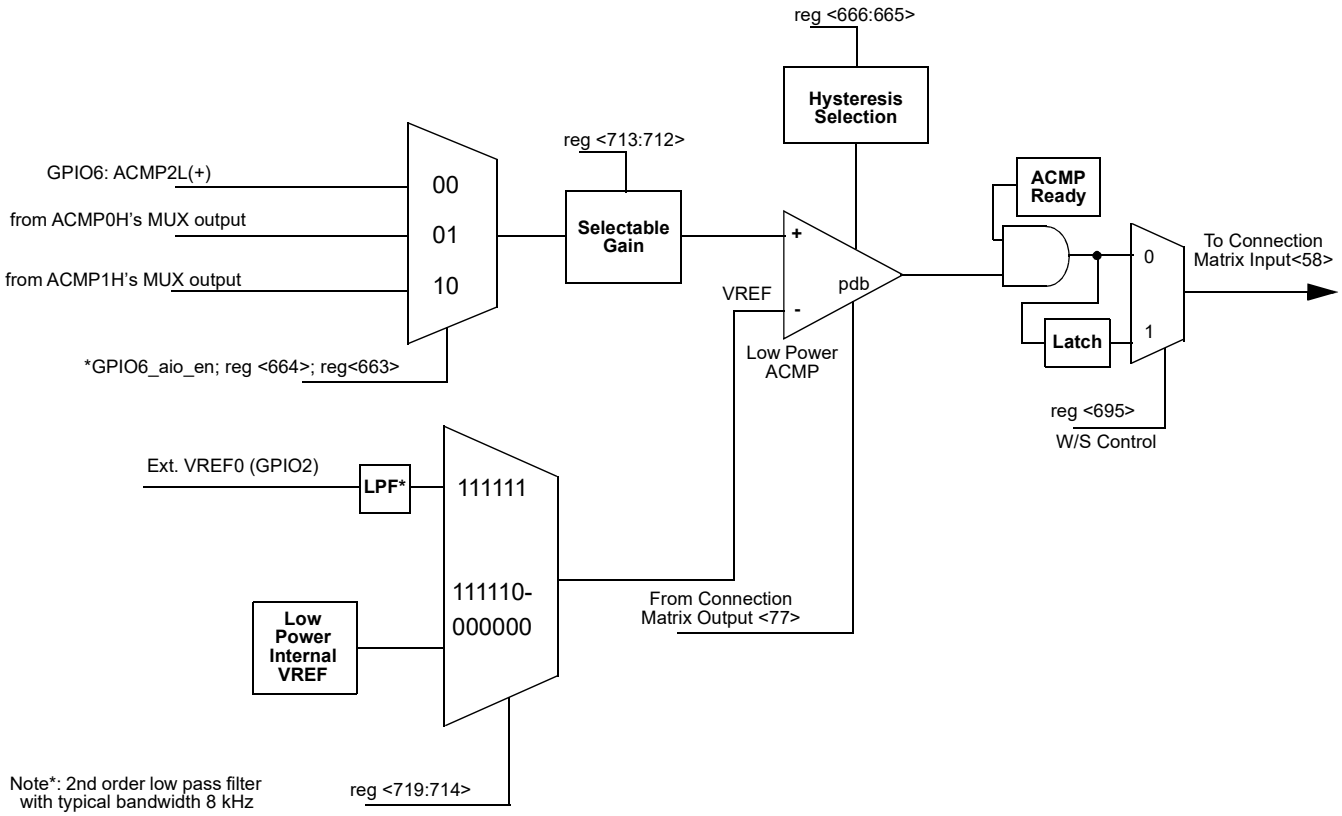



**Figure 60: ACMP2L Block Diagram**

### 9.4 ACMP3L BLOCK DIAGRAM

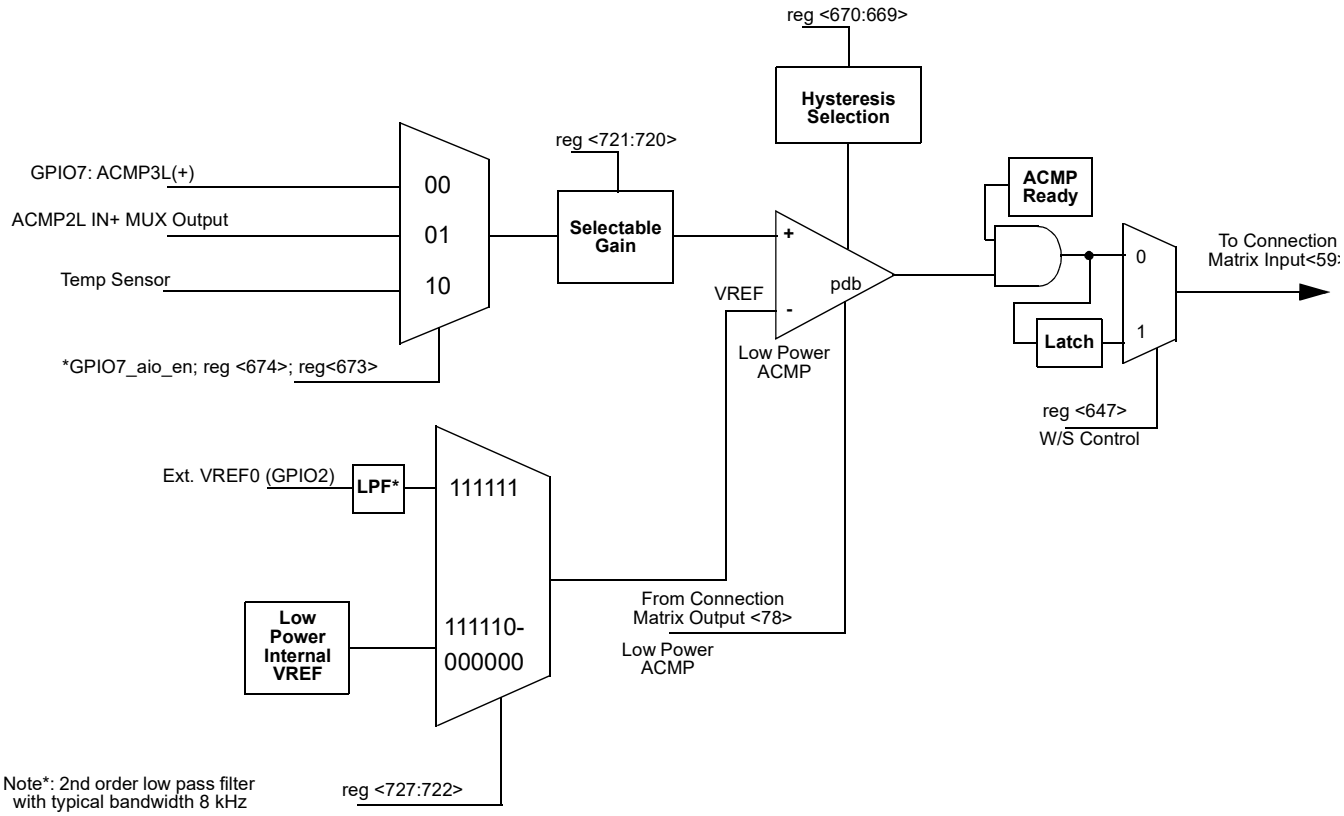



**Figure 61: ACMP3L Block Diagram**

# 10 Programmable Delay/Edge Detector

The SLG46867 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See Figure 62 for further information.

**Note:** The input signal must be longer than the delay, otherwise it will be filtered out.

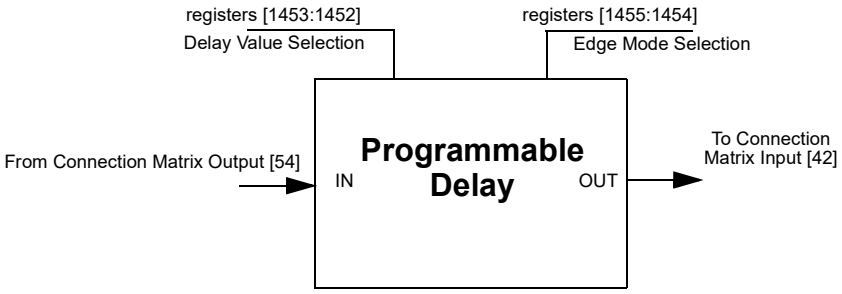



**Figure 62: Programmable Delay**

## 10.1 PROGRAMMABLE DELAY TIMING DIAGRAM - EDGE DETECTOR OUTPUT

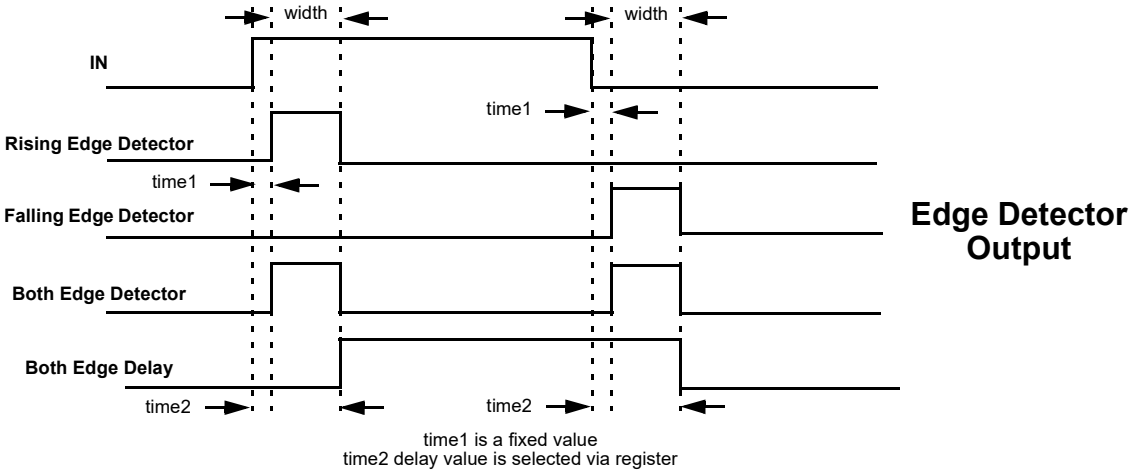



**Figure 63: Edge Detector Output**

Please refer to Table 9.

## 11 Additional Logic Function. Deglitch Filter

The SLG46867 has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection Matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

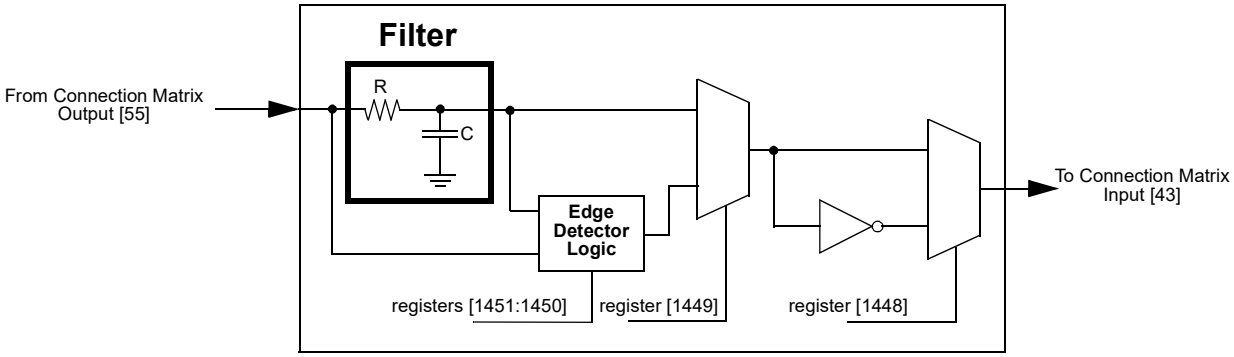



**Figure 64: Deglitch Filter/Edge Detector**

# 12 Voltage Reference (Vref)

## 12.1 VOLTAGE REFERENCE OVERVIEW

The SLG46867 has a Voltage Reference macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on GPIO8 and GPIO9. See Table 51 for the available selections for each analog comparator.

Also see Figure 65, which shows the reference output structure.

## 12.2 VREF SELECTION TABLE

**Table 51: Vref Selection Table**

| SEL[5:0] | Vref | SEL[5:0] | Vref |
|---|---|---|---|
| 0 | 0.032 | 32 | 1.056 |
| 1 | 0.064 | 33 | 1.088 |
| 2 | 0.096 | 34 | 1.12 |
| 3 | 0.128 | 35 | 1.152 |
| 4 | 0.16 | 36 | 1.184 |
| 5 | 0.192 | 37 | 1.216 |
| 6 | 0.224 | 38 | 1.248 |
| 7 | 0.256 | 39 | 1.28 |
| 8 | 0.288 | 40 | 1.312 |
| 9 | 0.32 | 41 | 1.344 |
| 10 | 0.352 | 42 | 1.376 |
| 11 | 0.384 | 43 | 1.408 |
| 12 | 0.416 | 44 | 1.44 |
| 13 | 0.448 | 45 | 1.472 |
| 14 | 0.48 | 46 | 1.504 |
| 15 | 0.512 | 47 | 1.536 |
| 16 | 0.544 | 48 | 1.568 |
| 17 | 0.576 | 49 | 1.6 |
| 18 | 0.608 | 50 | 1.632 |
| 19 | 0.64 | 51 | 1.664 |
| 20 | 0.672 | 52 | 1.696 |
| 21 | 0.704 | 53 | 1.728 |
| 22 | 0.736 | 54 | 1.76 |
| 23 | 0.768 | 55 | 1.792 |
| 24 | 0.8 | 56 | 1.824 |
| 25 | 0.832 | 57 | 1.856 |
| 26 | 0.864 | 58 | 1.888 |
| 27 | 0.896 | 59 | 1.92 |
| 28 | 0.928 | 60 | 1.952 |
| 29 | 0.96 | 61 | 1.984 |
| 30 | 0.992 | 62 | 2.016 |
| 31 | 1.024 | 63 | External |

### 12.3 VREF BLOCK DIAGRAM

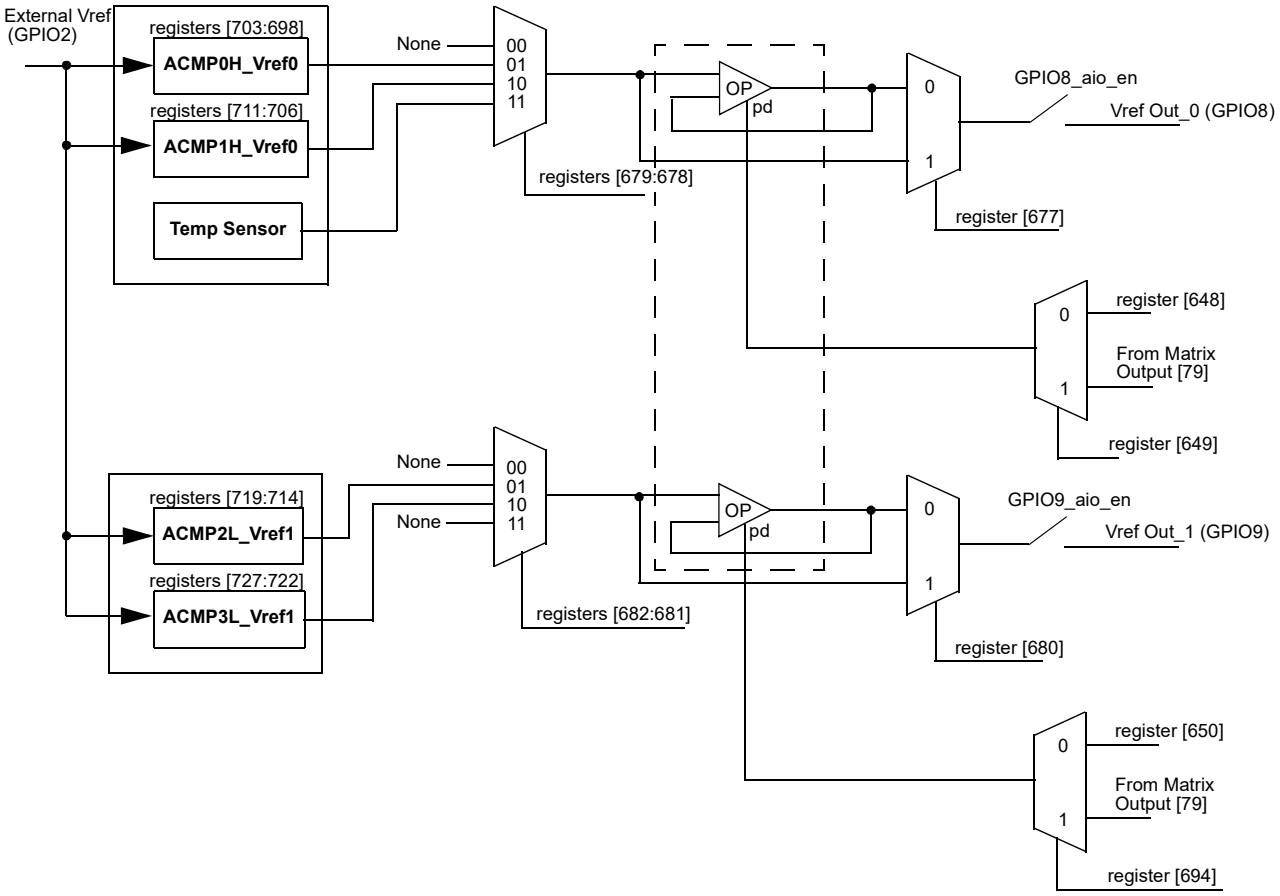



**Figure 65: Voltage Reference Block Diagram**

### 12.4 VREF LOAD REGULATION

**Note 1** It is not recommended to use Vref connected to external pin without buffer.

**Note 2** Vref buffer performance is not guaranteed at $V_{DD}$ < 2.7 V.

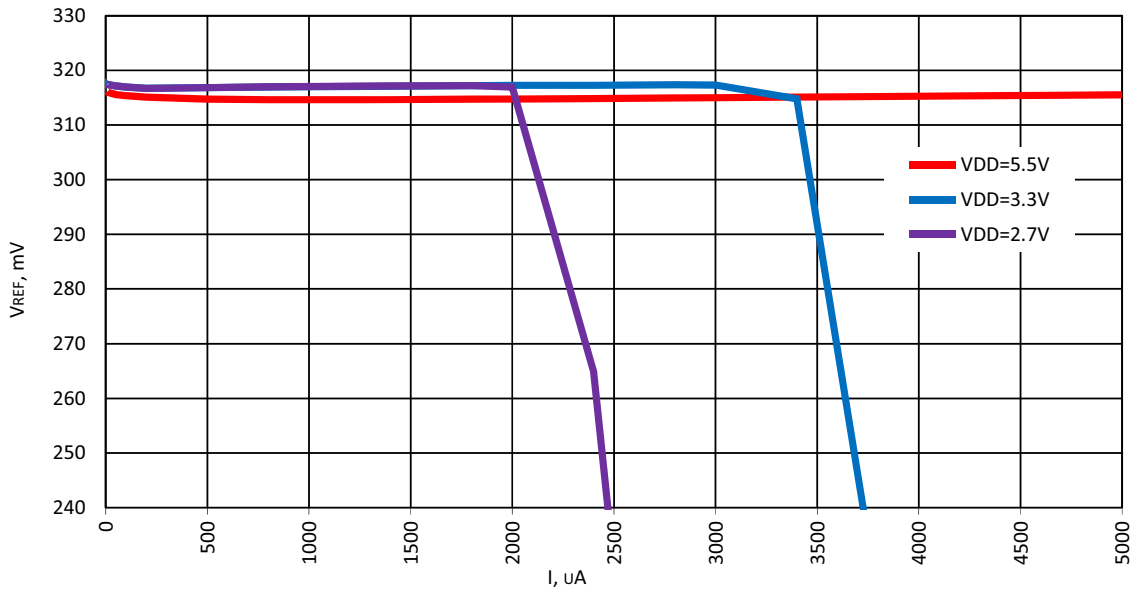



**Figure 66: Typical Load Regulation, Vref = 320 mV, T = -40 °C to +85 °C, Buffer - Enable**

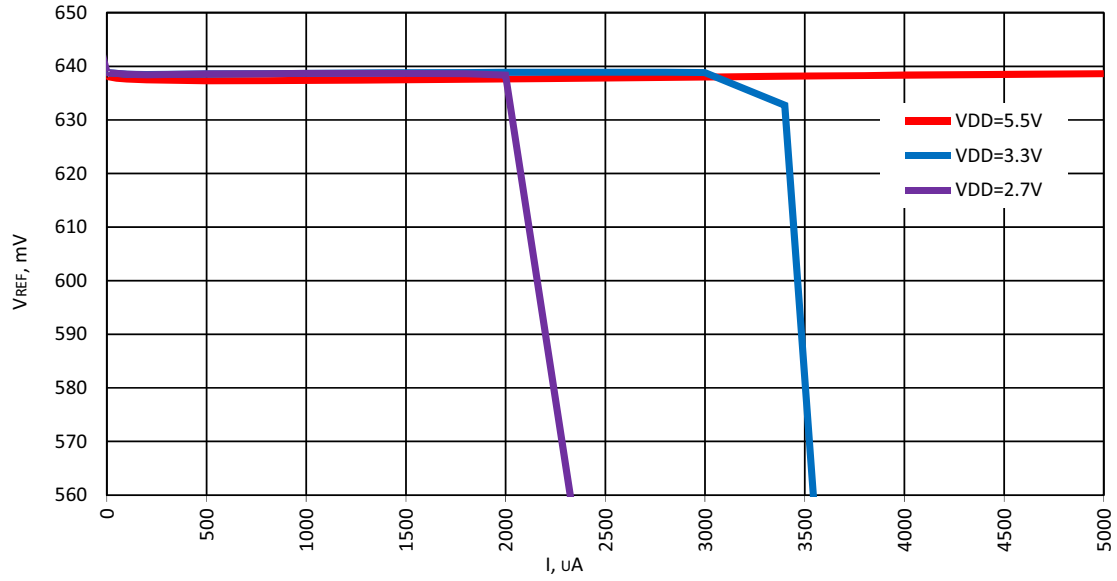



**Figure 67: Typical Load Regulation, Vref = 640 mV, T = -40 °C to +85 °C, Buffer - Enable**

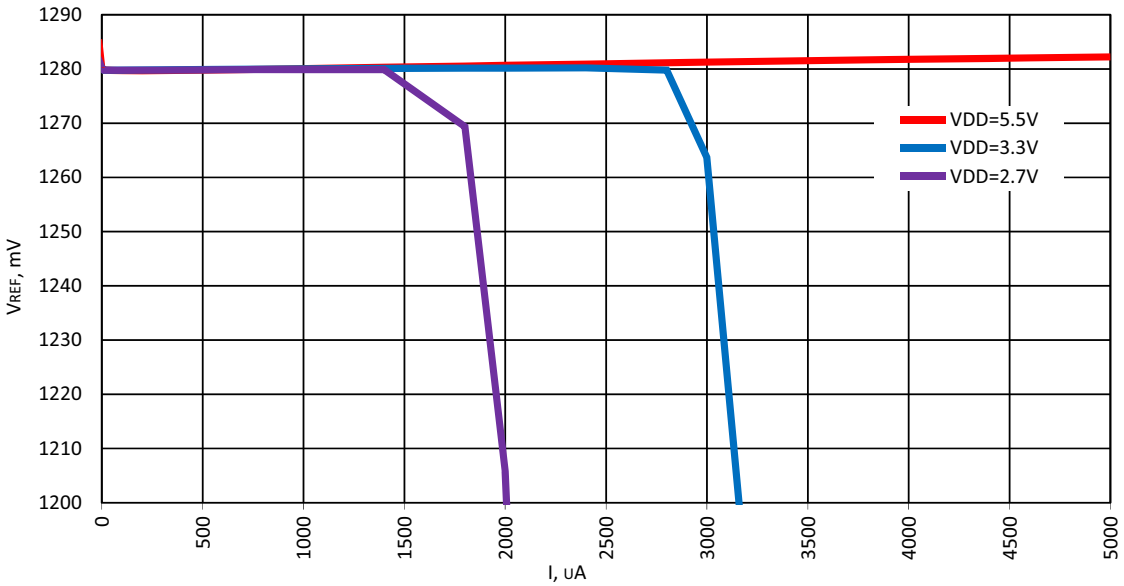



**Figure 68: Typical Load Regulation, Vref = 1280 mV, T = -40 °C to +85 °C, Buffer - Enable**

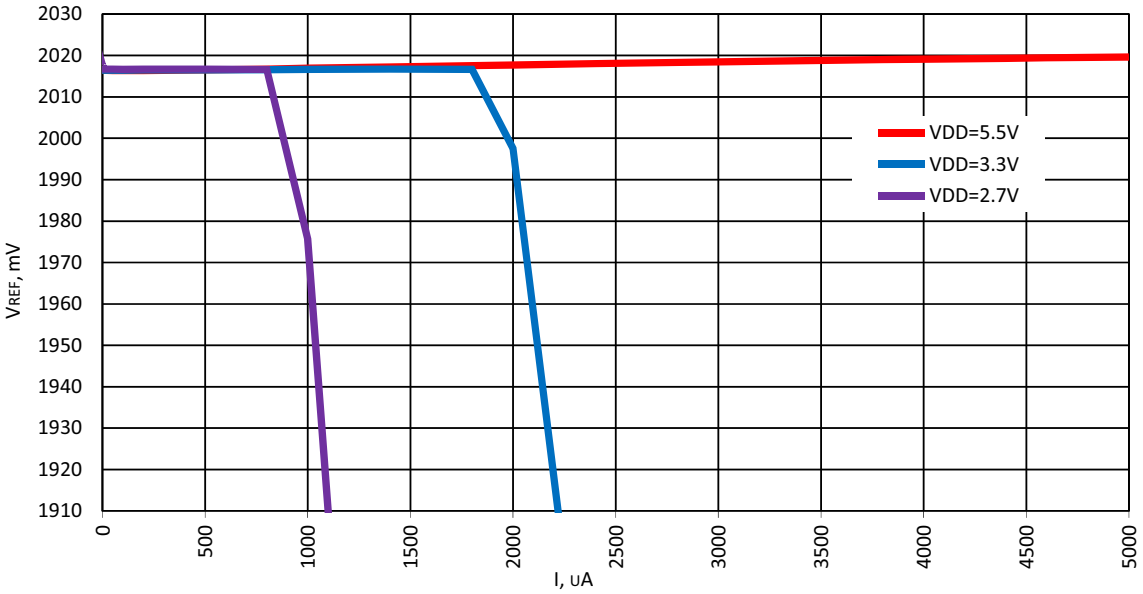



**Figure 69: Typical Load Regulation, Vref = 2016 mV, T = -40 °C to +85 °C, Buffer - Enable**

# 13 Clocking

## 13.1 OSC GENERAL DESCRIPTION

The SLG46867 has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [53], [54] and [55]. Please see Figure 73, for more details on the SLG46867 clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [749]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power Down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power Down/Force On (Connection Matrix Output [80], [81], [82]) signal has the highest priority. The OSC operates according to the following table:

**Table 52: Oscillator Operation Mode Configuration Settings**

| POR | External Clock Selection | Signal From Connection Matrix | Register: Power Down or Force On by Matrix Input | Register: Auto Power-On or Force On | OSC Enable Signal from CNT/DLY Macrocells | OSC Operation Mode |
|---|---|---|---|---|---|---|
| 0 | X | X | X | X | X | OFF |
| 1 | 1 | X | X | X | X | Internal OSC is OFF, logic is ON |
| 1 | 0 | 1 | 0 | X | X | OFF |
| 1 | 0 | 1 | 1 | X | X | ON |
| 1 | 0 | 0 | X | 1 | X | ON |
| 1 | 0 | 0 | X | 0 | CNT/DLY requires OSC | ON |
| 1 | 0 | 0 | X | 0 | CNT/DLY does not require OSC | OFF |

**Note 1** The OSC will run only when any macrocell that uses OSC is powered on.

### 13.2 OSCILLATOR0 (2.048 KHZ)

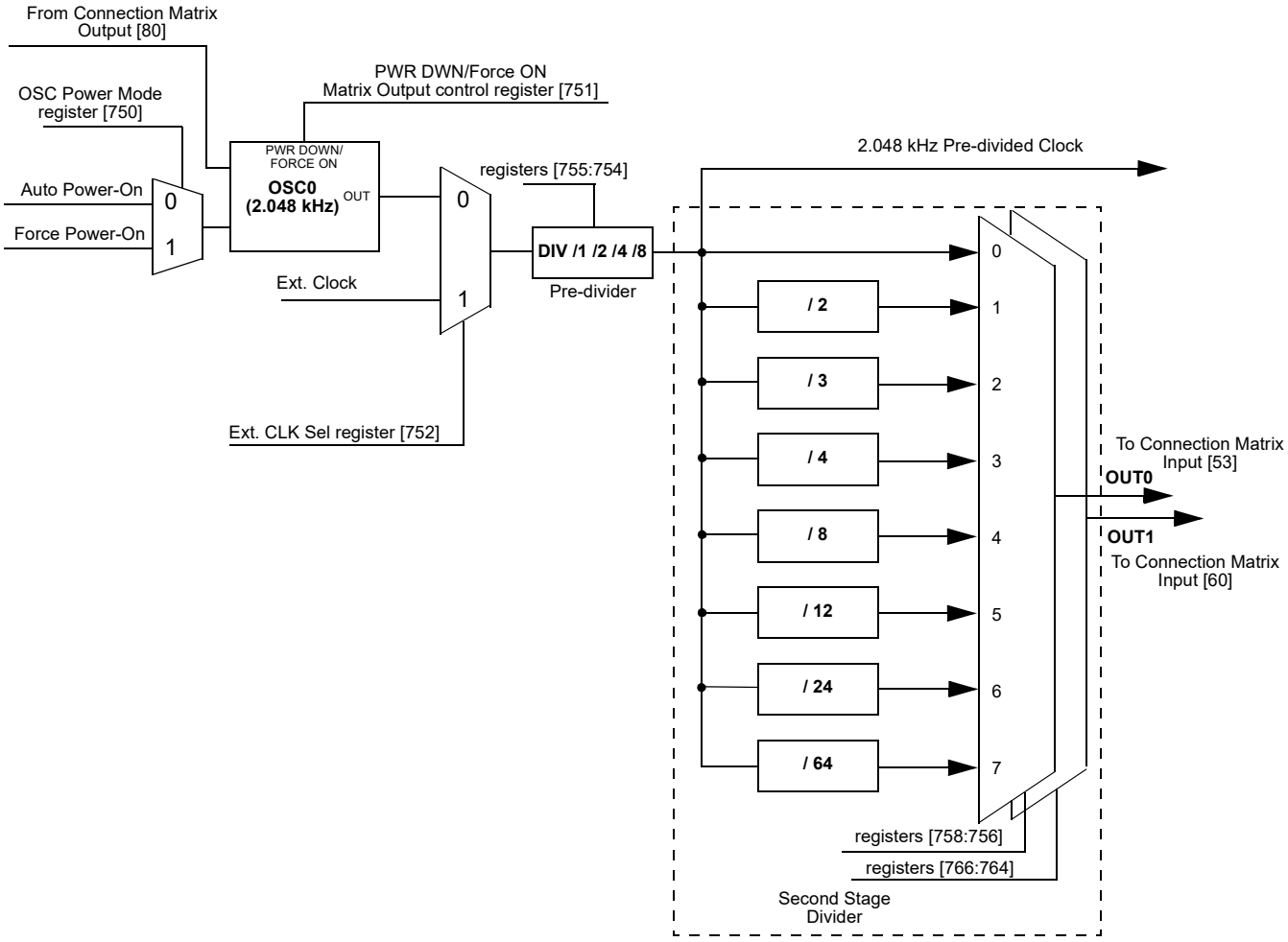



**Figure 70: Oscillator0 Block Diagram**

### 13.3 OSCILLATOR1 (2.048 MHZ)

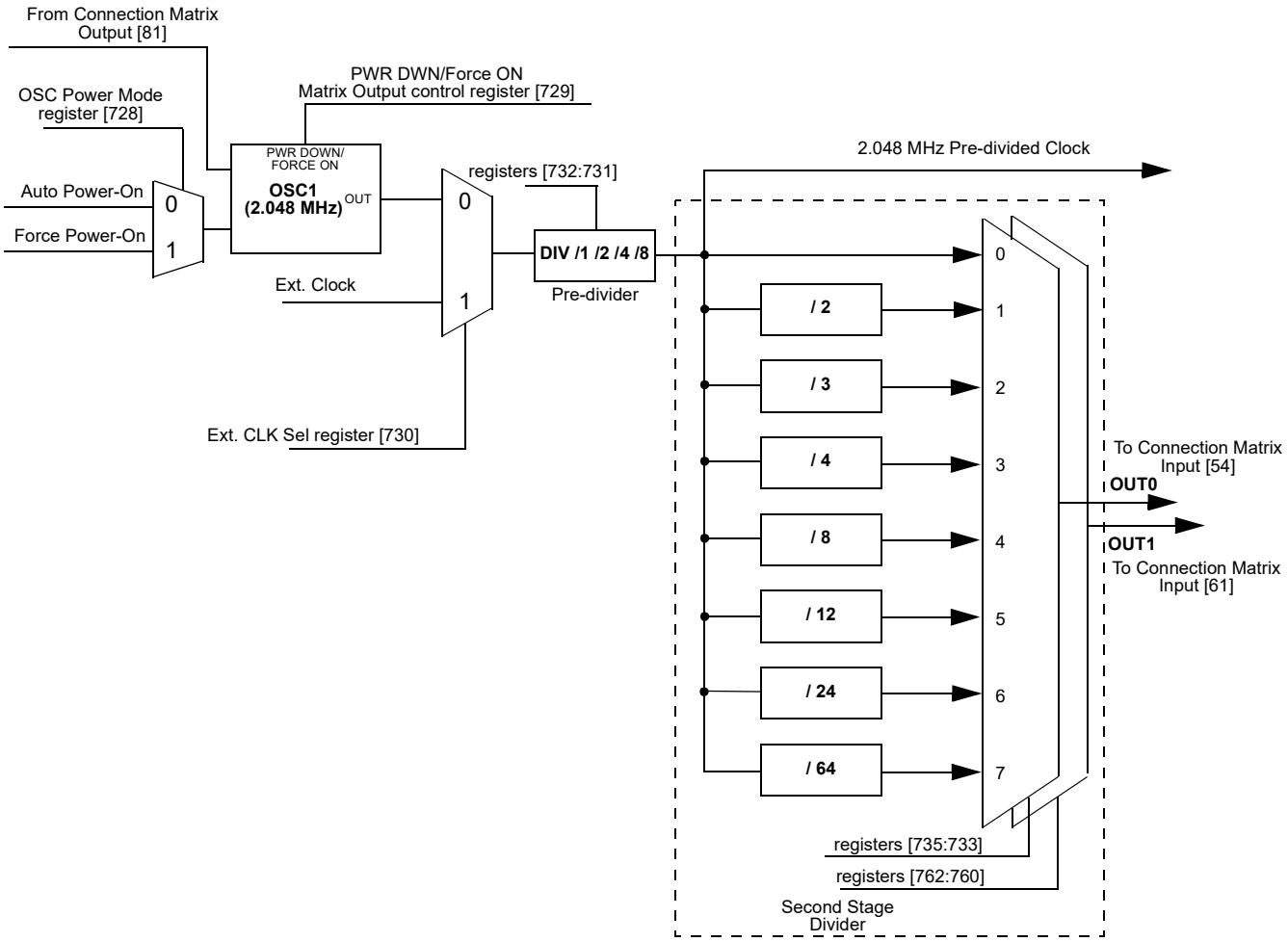



**Figure 71: Oscillator1 Block Diagram**

### 13.4 OSCILLATOR2 (25 MHZ)

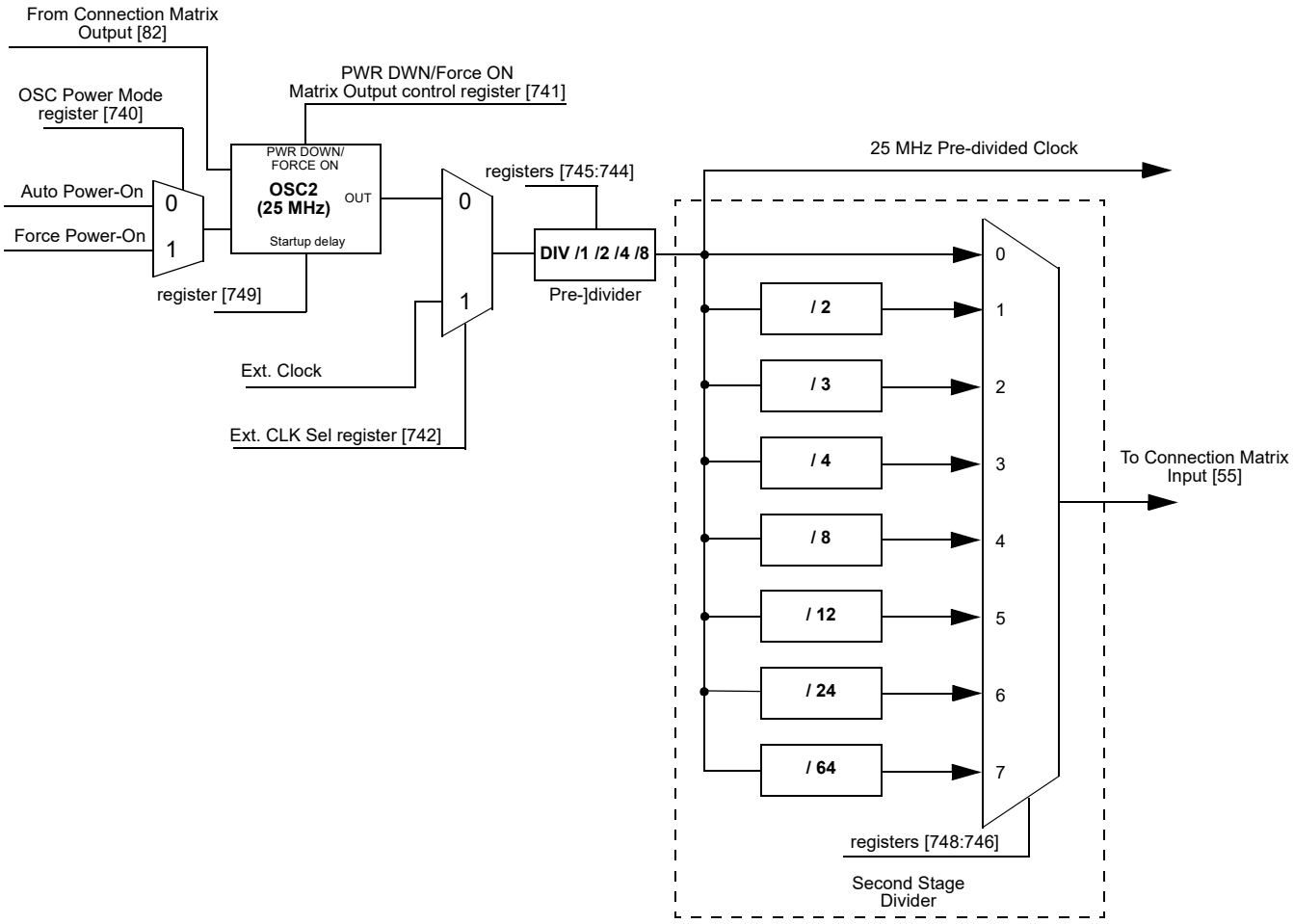



**Figure 72: Oscillator2 Block Diagram**

### 13.5 CNT/DLY CLOCK SCHEME

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

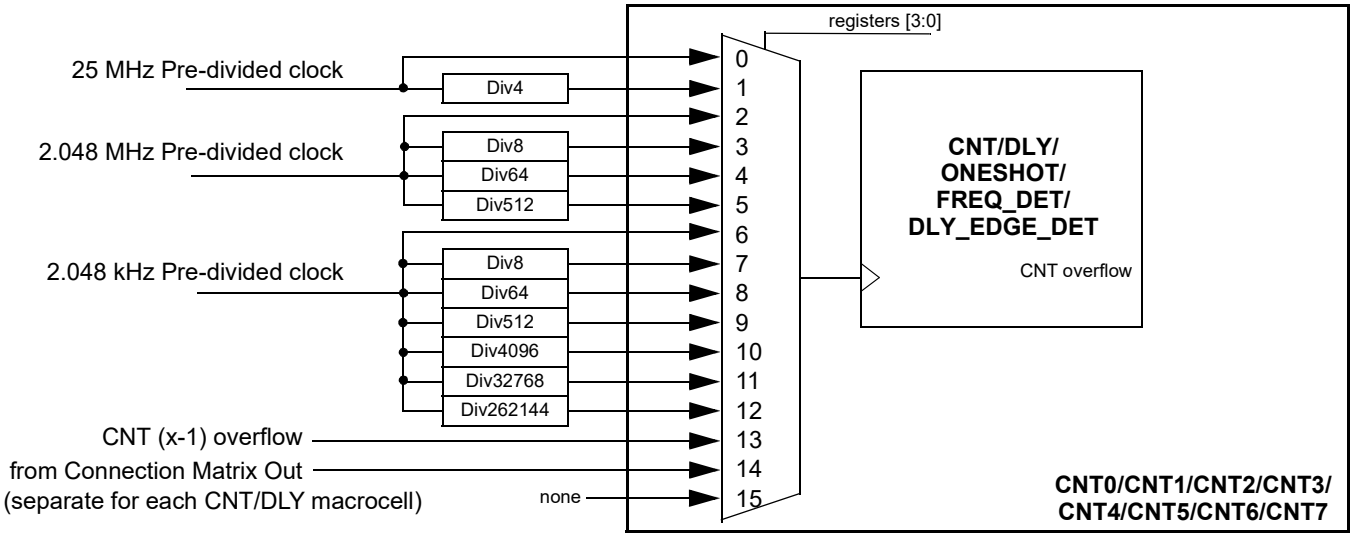



**Figure 73: Clock Scheme**

## 13.6 EXTERNAL CLOCKING

The SLG46867 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

### 13.6.1 GPI0 Source for Oscillator0 (2.048 kHz)

When register [752] is set to 1, an external clocking signal on GPI0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 70. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

### 13.6.2 GPIO2 Source for Oscillator1 (2.048 MHz)

When register [730] is set to 1, an external clocking signal on GPIO2 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 71. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

### 13.6.3 GPIO8 Source for Oscillator 2 (25 MHz)

When register [742] is set to 1, an external clocking signal on GPIO8 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 72. The external frequency range is 0 MHz to 20 MHz at $V_{DD}$ = 2.3 V, 30 MHz at $V_{DD}$ = 3.3 V, 50 MHz at $V_{DD}$ = 5.0 V.

### 13.7 OSCILLATORS POWER-ON DELAY

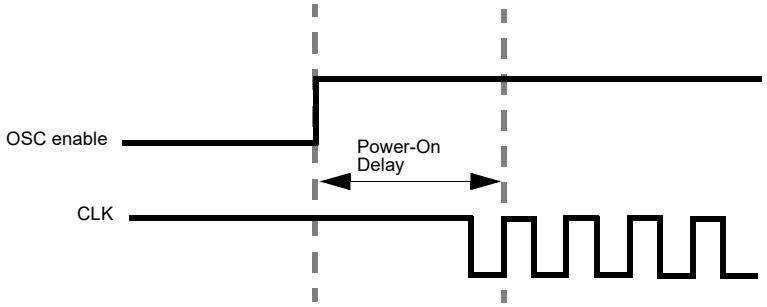



**Figure 74: Oscillator Startup Diagram**

**Note 1** OSC power mode: “Auto Power-On”.

**Note 2** “OSC enable” signal appears when any macrocell that uses OSC is powered on.

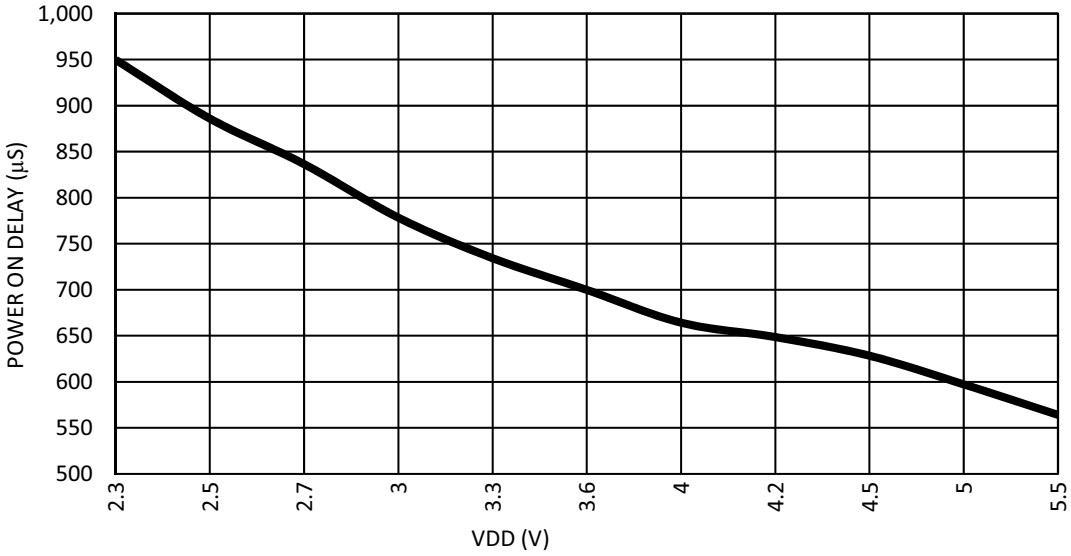



**Figure 75: RC Oscillator Maximum Power-On Delay vs. $V_{DD}$ at Room Temperature, OSC0 = 2.048 kHz**

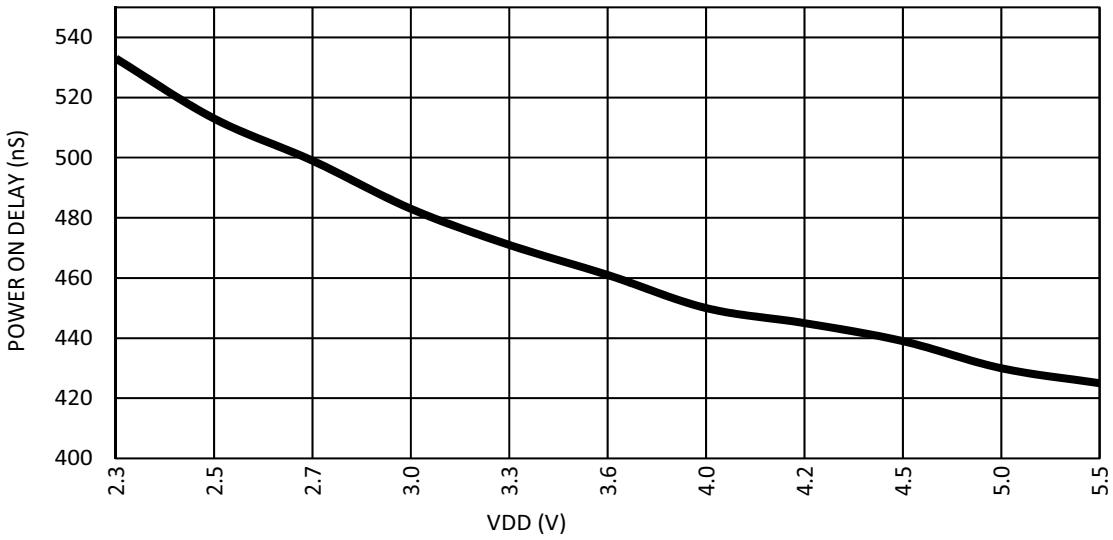



**Figure 76: RC Oscillator Maximum Power-On Delay vs. $V_{DD}$ at Room Temperature, OSC1 = 2.048 MHz**

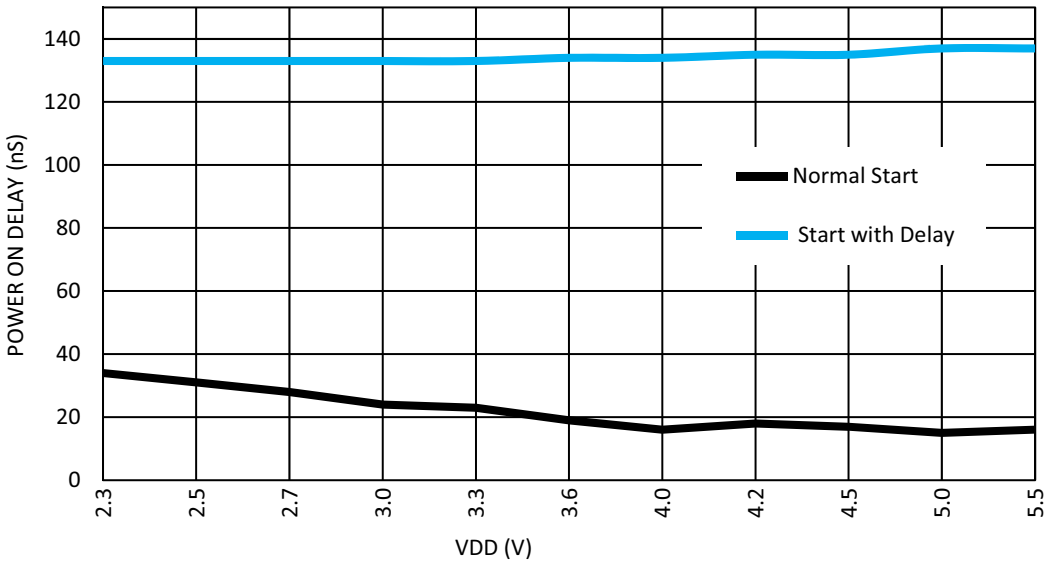



**Figure 77: RC Oscillator Maximum Power-On Delay vs. $V_{DD}$ at Room Temperature, OSC2 = 25 MHz**

### 13.8 OSCILLATORS ACCURACY

**Note:** OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

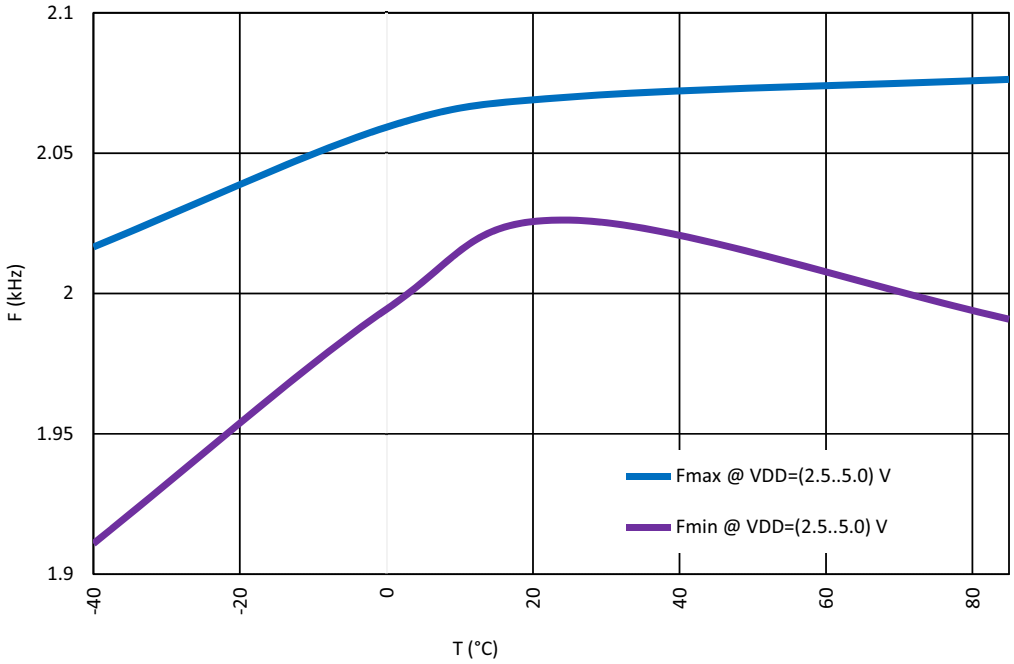



**Figure 78: RC Oscillator Frequency vs. Temperature, OSC0 = 2.048 kHz**

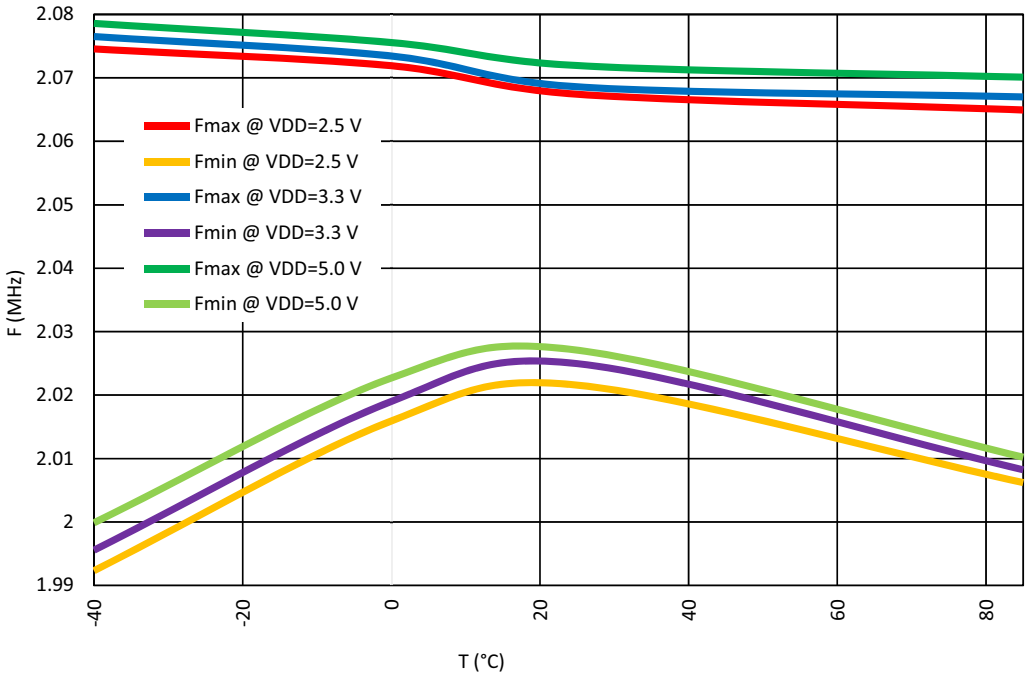



**Figure 79: RC Oscillator Frequency vs. Temperature, OSC1 = 2.048 MHz**

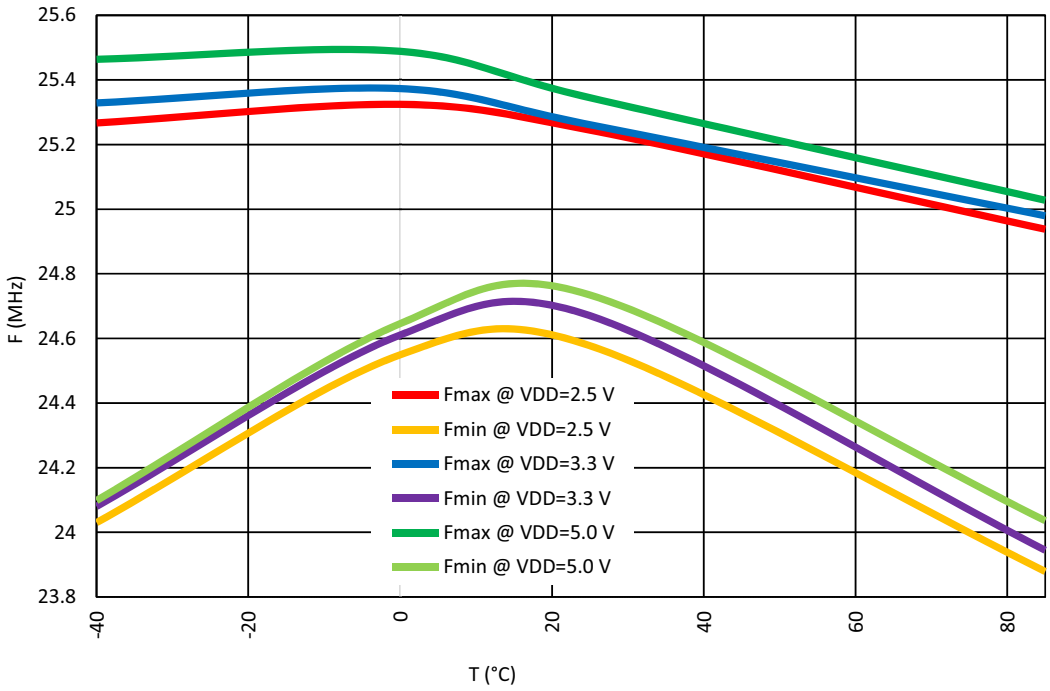



**Figure 80: RC Oscillator Frequency vs. Temperature, OSC2 = 25 MHz**

**Note:** For more information see Section 3.6.

# 14 Power-On Reset (POR)

The SLG46867 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the $V_{DD}$ power is first ramping to the device, and also while the $V_{DD}$ is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

## 14.1 GENERAL OPERATION

The SLG46867 is guaranteed to be powered down and non-operational when the $V_{DD}$ voltage (voltage on PIN1) is less than Power-Off Threshold (see in Table 3.3), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher **(Note)** than the $V_{DD}$ voltage is applied to any other PIN. For example, if $V_{DD}$ voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

**Note:** There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46867, the voltage applied on the $V_{DD}$ should be higher than the Power_ON threshold **(Note)**. The full operational $V_{DD}$ range for the SLG46867 is 2.3 V to 5.5 V. This means that the $V_{DD}$ voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the $V_{DD}$ voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46867 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

**Note:** The Power_ON threshold is defined in Table 3.3.

To power down the chip the $V_{DD}$ voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can't be bigger than the $V_{DD}$, this rule also applies to the case when the chip is powered on.

### 14.2 POR SEQUENCE

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 81.

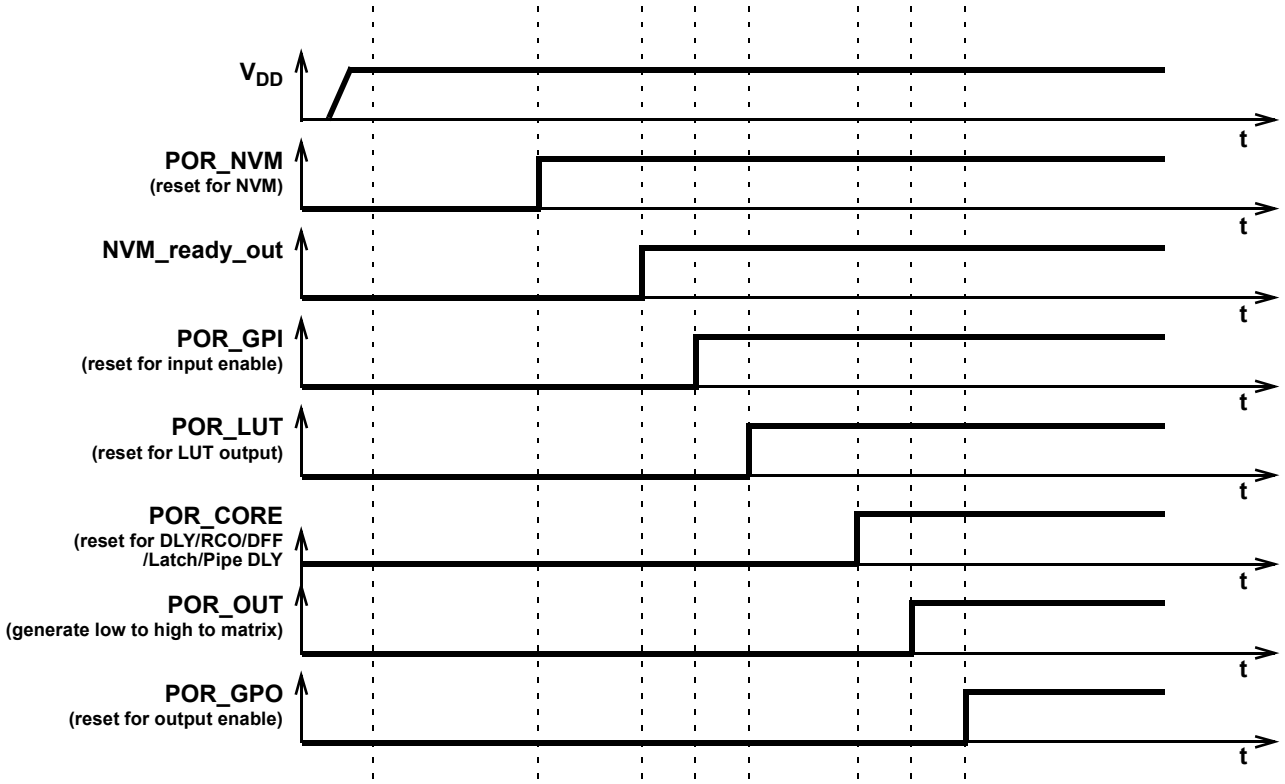



**Figure 81: POR Sequence**

As can be seen from Figure 81 after the $V_{DD}$ has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to a CMOS Latch that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, $V_{DD}$ value, temperature and even will vary from chip to chip (process influence).

### 14.3 MACROCELLS OUTPUT STATES DURING POR SEQUENCE

To have a full picture of SLG46867 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 82 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

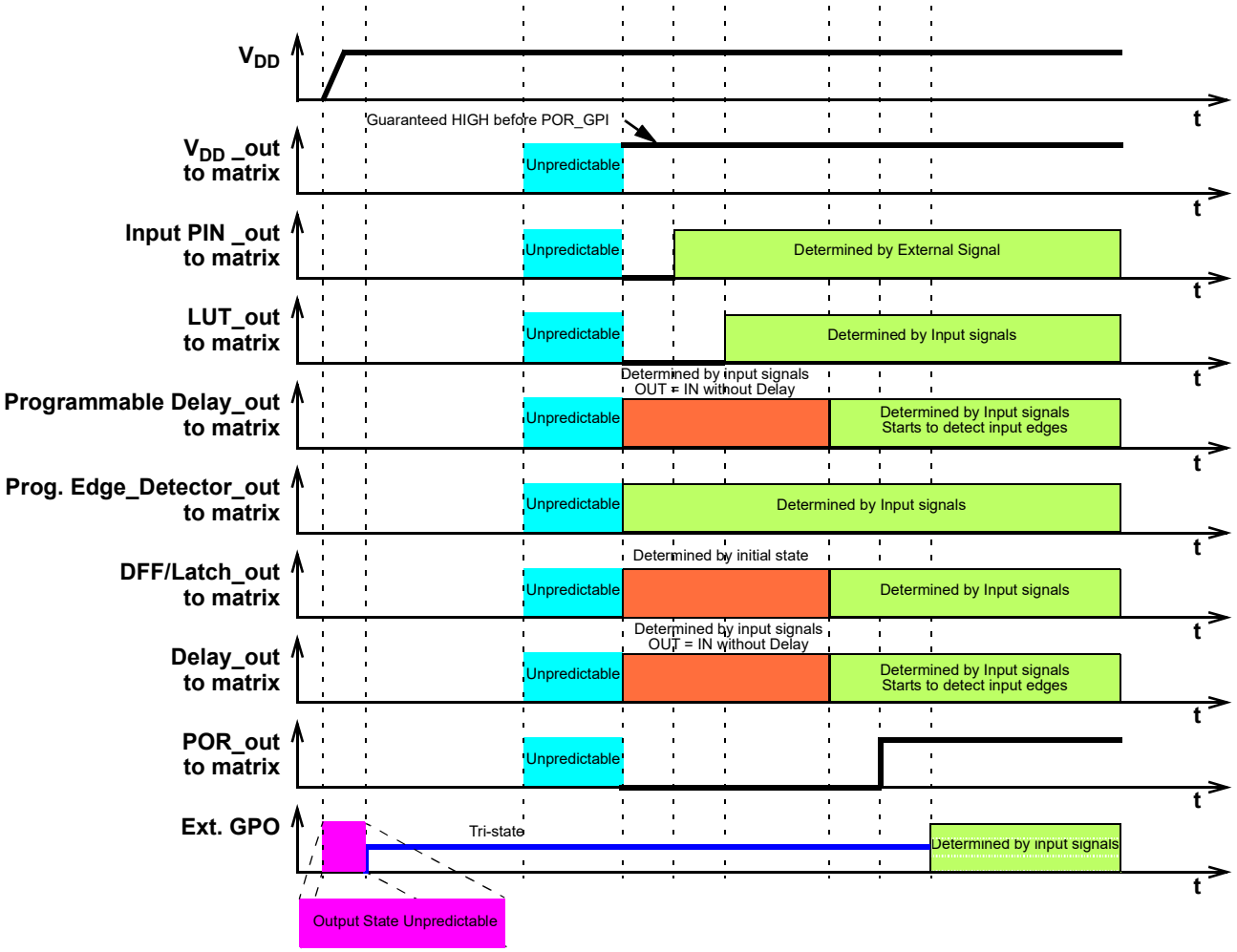



**Figure 82: Internal Macrocell States During POR Sequence**

### 14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.62 V to 1.98 V, macrocells in SLG46867 are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, pull up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

**Note:** The maximum voltage applied to any pin should not be higher than the $V_{DD}$ level. There are ESD Diodes between pin → $V_{DD}$ and pin → GND on each pin. So if the input signal applied to pin is higher than $V_{DD}$, then current will sink through the diode to $V_{DD}$. Exceeding $V_{DD}$ results in leakage current on the input pin, and $V_{DD}$ will be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as $V_{DD}$.

### 14.3.2 Power Down

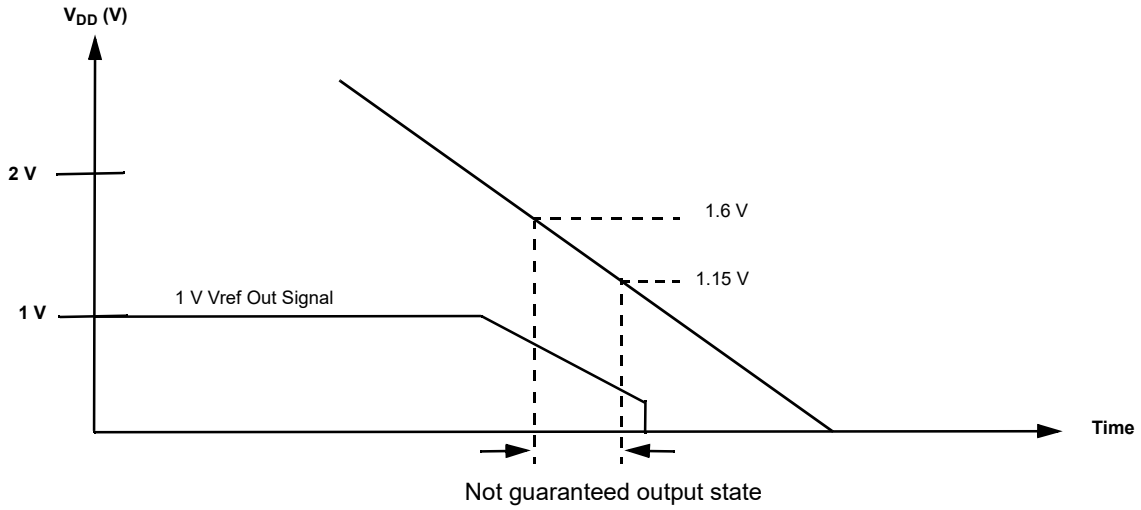



**Figure 83: Power Down**

During powerdown, macrocells in SLG46867 are powered off after $V_{DD}$ falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

# 15 I²C Serial Communications Macrocell

## 15.1 I²C SERIAL COMMUNICATIONS MACROCELL OVERVIEW

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1967:1965]. See Section 15.5.1 for more details on I²C read/write memory protection.

## 15.2 I²C SERIAL COMMUNICATIONS DEVICE ADDRESSING

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 84. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by GPI0, GPIO2, GPIO4 and GPIO5. The LSB of the control code is defined by the value of GPI0, while the MSB is defined by the value of GPIO5. The address source (either register bit or PIN) for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46867 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9 and A8) will be "0" for all commands to the SLG46867.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 84 shows this basic command structure.

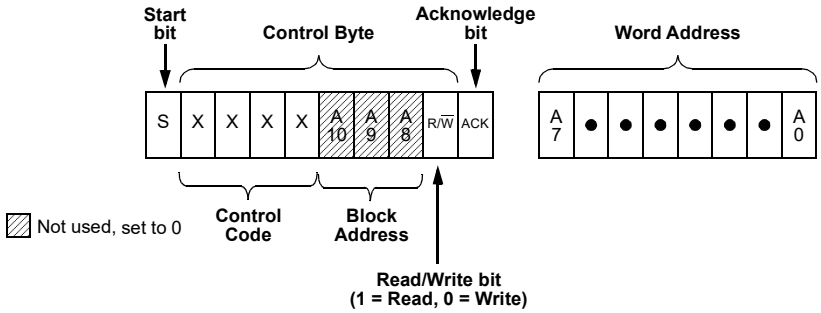



**Figure 84: Basic Command Structure**

## 15.3 I²C SERIAL GENERAL TIMING

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 85. Timing specifications can be found in the AC Characteristics section.

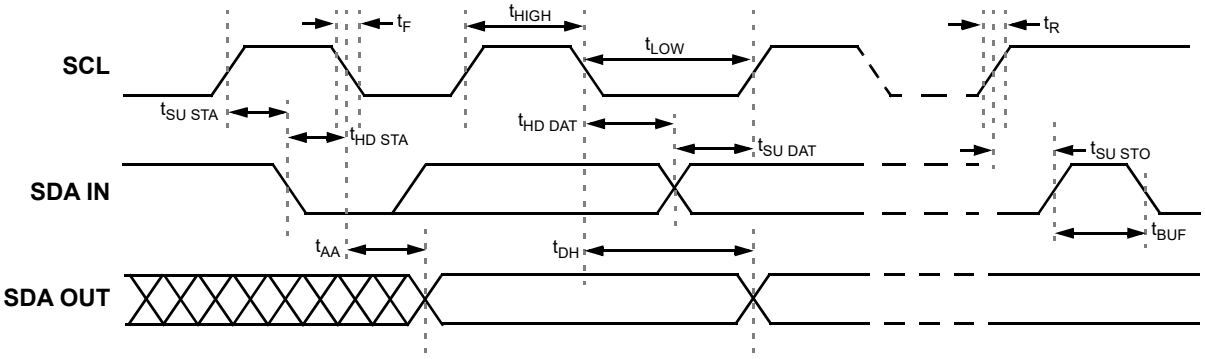



**Figure 85: I²C General Timing Characteristics**

## 15.4 I²C SERIAL COMMUNICATIONS COMMANDS

### 15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits] and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46867 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46867 where the data byte is to be written. After the SLG46867 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46867 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46867 generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1961]=1 - Enable. It means that IOs will remain their state until the write command is done.

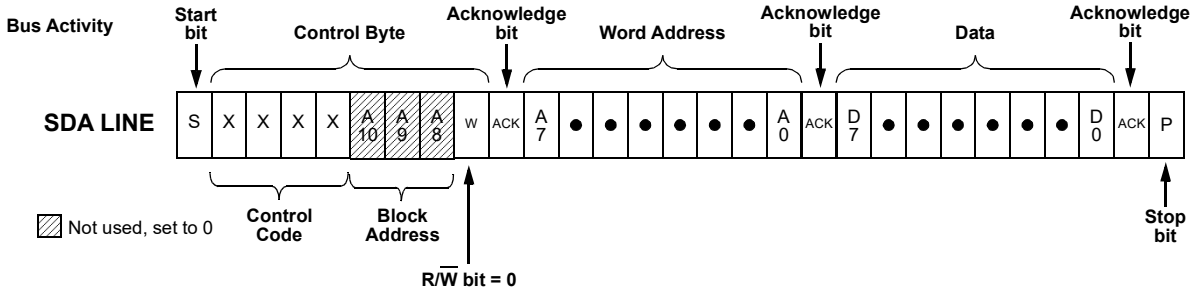



**Figure 86: Byte Write Command, R/$\overline{W}$ = 0**

### 15.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46867 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46867. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46867 generates the Acknowledge bit.

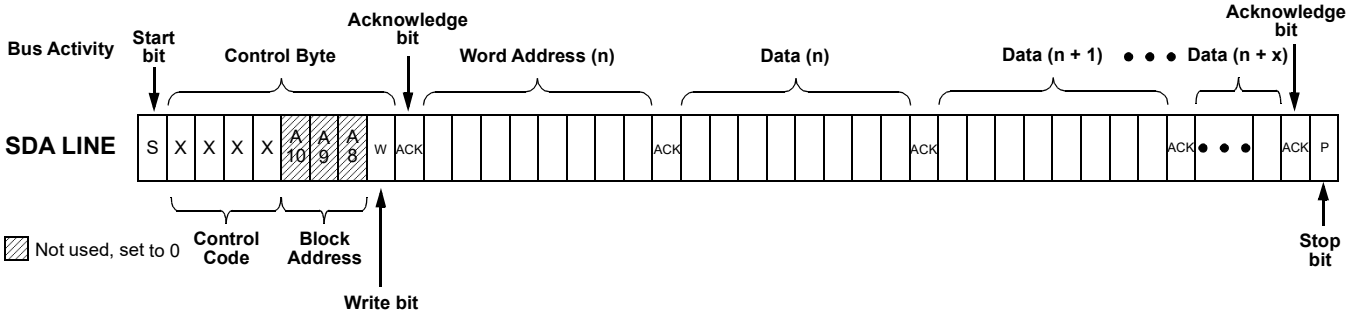



**Figure 87: Sequential Write Command**

### 15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46867 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

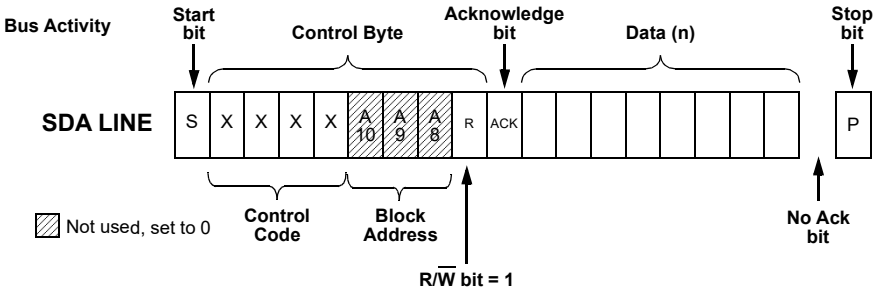



**Figure 88: Current Address Read Command, R/$\overline{W}$ = 1**

### 15.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46867 issues an Acknowledge bit, followed by the requested eight data bits.

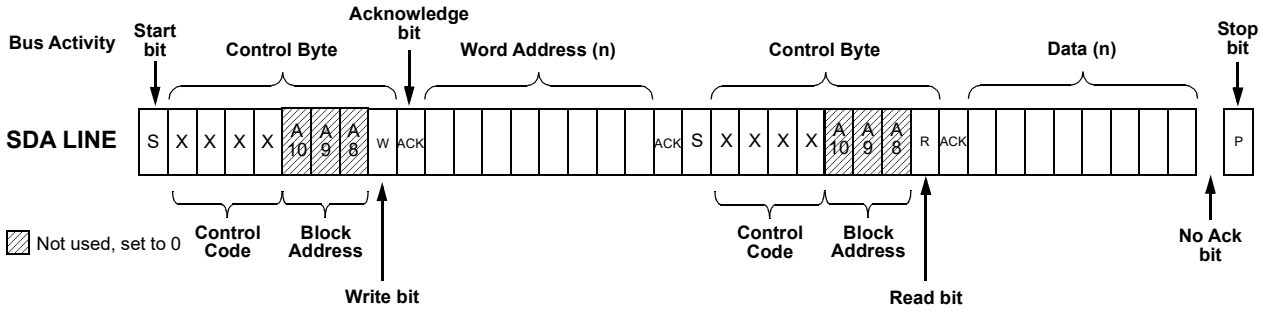



**Figure 89: Random Read Command**

### 15.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG46867 transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

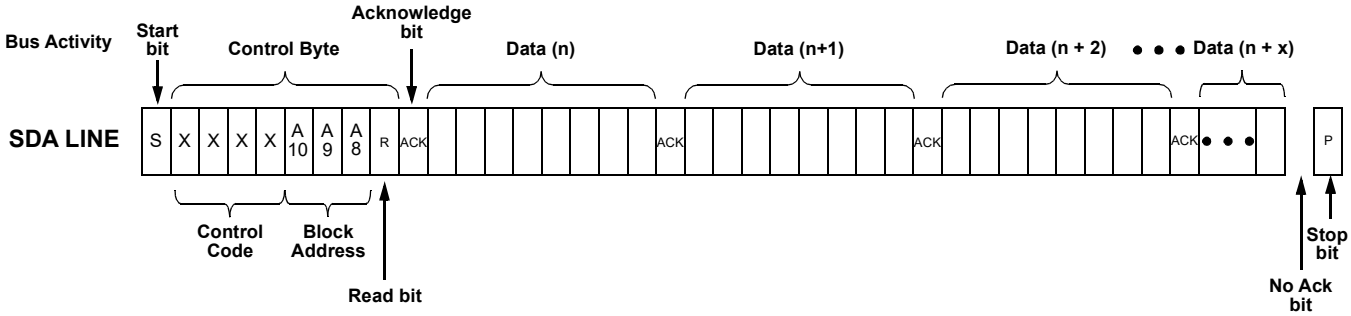



**Figure 90: Sequential Read Command**

## 15.5 I²C SERIAL COMMAND REGISTER MAP

### 15.5.1 Register Read/Write Protection

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 53 for details.

**Table 53: Read/Write Protection Options**

| Configurations | Protection Modes Configuration | | | | | | | Data Output From | Register Address |
|---|---|---|---|---|---|---|---|---|---|
| | Unlocked | Partly Lock Read1 | Partly Lock Read2 | Partly Lock Read2/ Write | Lock Read | Lock Write | Lock Read/ Write | | |
| | (Mode 0) | (Mode 1) | (Mode 2) | (Mode 3) | (Mode 4) | (Mode 5) | (Mode 6) | | |
| I²C Byte Write Bit Masking (section 15.5.6) | R/W | R/W | R/W | R/W | W | R | - | Memory | F6 |
| I²C Serial Reset Command (section 15.5.2) | R/W | R/W | R/W | R/W | W | R | - | Memory | F5,b'0 |
| Outputs Latching During I²C Write | R/W | R/W | R/W | R/W | W | R | - | Memory | F5,b'1 |
| Connection Matrix Virtual Inputs (section 6.3) | R/W | R/W | R/W | R/W | W | R | - | Macrocell | 4C |
| Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, etc.) | R/W | R/W | W | - | W | R | - | Memory | |
| Macrocells Inputs Configuration (Connection Matrix Outputs, section 6.2) | R/W | W | W | - | W | R | - | Memory | 0~47 |
| Protection Mode Enable | R | R | R | R | R | R | R | Memory | F5,b'3 |
| Protection Mode Selection | R/W | R | R | R | R | R | R | Memory | F5,b'7~5 |
| Macrocells Output Values (Connection Matrix Inputs, section 6.1) | R | R | R | R | - | R | - | Macrocell | 48~4B; 4D~4F |
| Counter Current Value (for 16-bit CNT) | R | R | R | R | - | R | - | Macrocell | A5,A6 |
| Counter Current Value (for 8-bit CNT) | R | R | R | R | - | R | - | Macrocell | A7,A8 |
| I²C Control Code (section 15.2) | R | R | R | R | R | R | R | Memory | FD,b'3~0 |
| Pin Slave Address Select | R | R | R | R | R | R | R | Memory | FD,b'7~4 |
| I²C Disable/Enable | R | R | R | R | R | R | R | Memory | FE,b'0 |

**Table 53: Read/Write Protection Options** (continued)

| Configurations | Protection Modes Configuration | | | | | | | Data Output From | Register Address |
|---|---|---|---|---|---|---|---|---|---|
| | Unlocked | Partly Lock Read1 | Partly Lock Read2 | Partly Lock Read2/ Write | Lock Read | Lock Write | Lock Read/ Write | | |
| | (Mode 0) | (Mode 1) | (Mode 2) | (Mode 3) | (Mode 4) | (Mode 5) | (Mode 6) | | |
| Programming disable | R | R | R | R | R | R | R | Memory | FE,b'1 |
| Code Compare Enable | R | R | R | R | R | R | R | Memory | FE,b'2 |

| | |
|---|---|
| R/W | Allow Read and Write Data |
| W | Allow Write Data Only |
| R | Allow Read Data Only |
| - | The Data is protected for Read and Write |

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I2C write will do not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, etc.

See Section 18 for detailed information on all registers.

### 15.5.2 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1960] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1960] will be set to “0” automatically. The Figure 91 illustrates the sequence of events for this reset function.

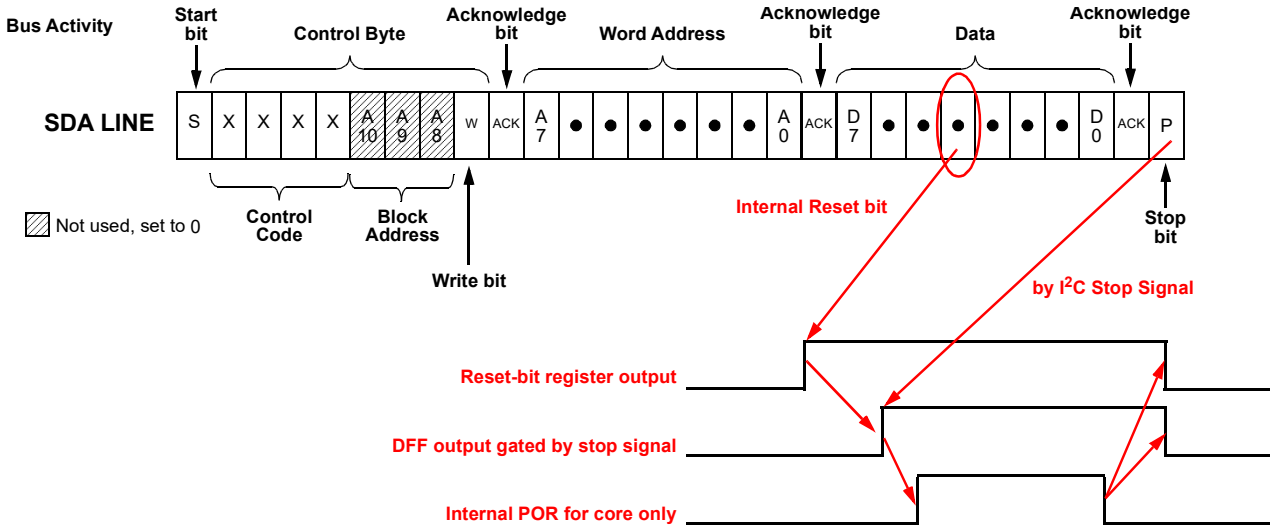



**Figure 91: Reset Command Timing**

### 15.5.3 I²C Additional Options

When Output latching during I²C write, register [1961] = 1 allows all PINs output value to be latched until I²C write is done. It will protect the output change due to configuration process during I²C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I²C write.

If the user sets GPIO0 and GPIO1 function to a selection other than SDA and SCL, all access via I²C will be disabled.

**Note:** Any write commands that come to the device via I²C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section 18 for detailed information on all registers.

### 15.5.4 Reading Counter Data via I²C

The current count value in three counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

### 15.5.5 I²C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46867 chip has four pins which can be used as an I²C Expander. These four pins are GPO0, GPIO6, GPIO7, and GPIO8.

Each of these pins can be used as an I²C Expander output or used as a normal pin. Also each of these four expander outputs have initial state settings which are specified in registers [1959:1952].

### 15.5.6 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46867 supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 for details) on the I²C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I²C Byte Write Mask Register will mask the effect of changing that

particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 92 shows an example of this function.


**Figure 92: Example of I²C Byte Write Bit Masking**

## 16 Analog Temperature Sensor

The SLG46867 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref0, so it is impossible to use both cells simultaneously, its output can be connected directly to the GPIO8 or to the ACPM3_L positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40°C to 85°C temperature range. The error in the whole temperature range does not exceed ±1.5 %. TS output voltage variation over $V_{DD}$ at constant temperature is less than ±1.5 %. For more detail refer to section 3.8.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2°C.

$$V_{TS1} = -2.3 \times T + 905.2$$

$$V_{TS2} = -2.8 \times T + 1077.2$$

where:

$V_{TS1}$ (mV) - TS Output Voltage, range 1

$V_{TS2}$ (mV) - TS Output Voltage, range 2

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

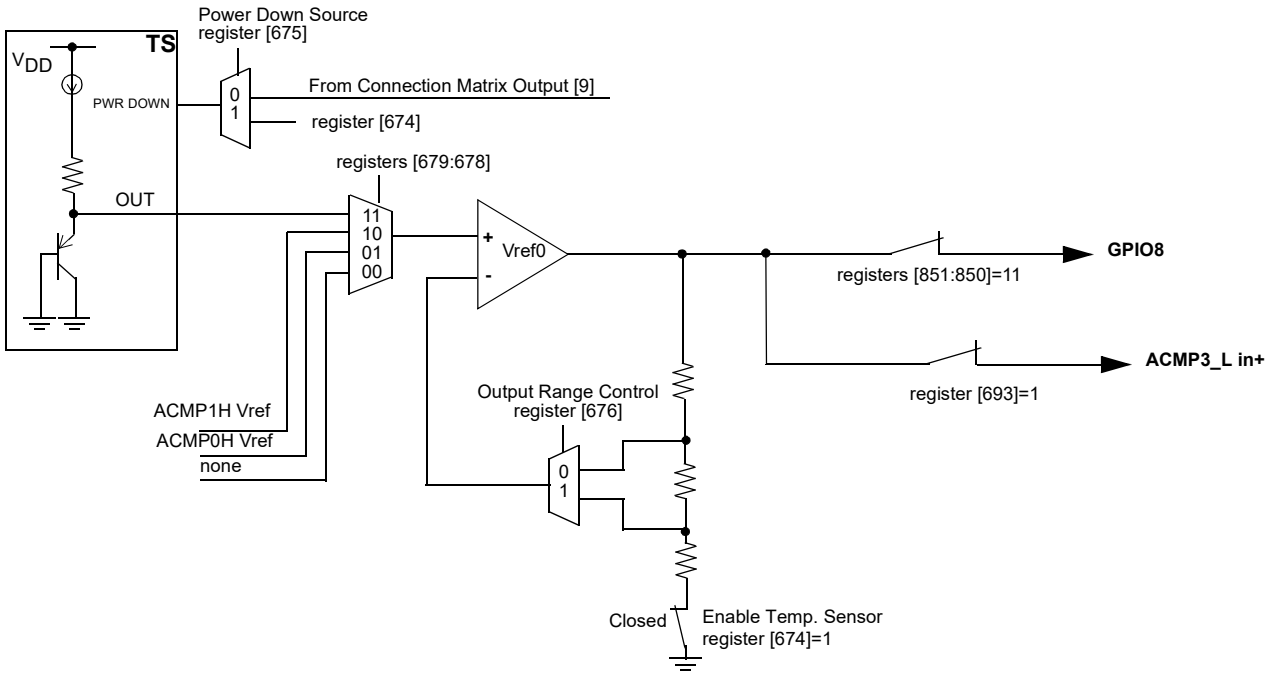



**Figure 93: Analog Temperature Sensor Structure Diagram**

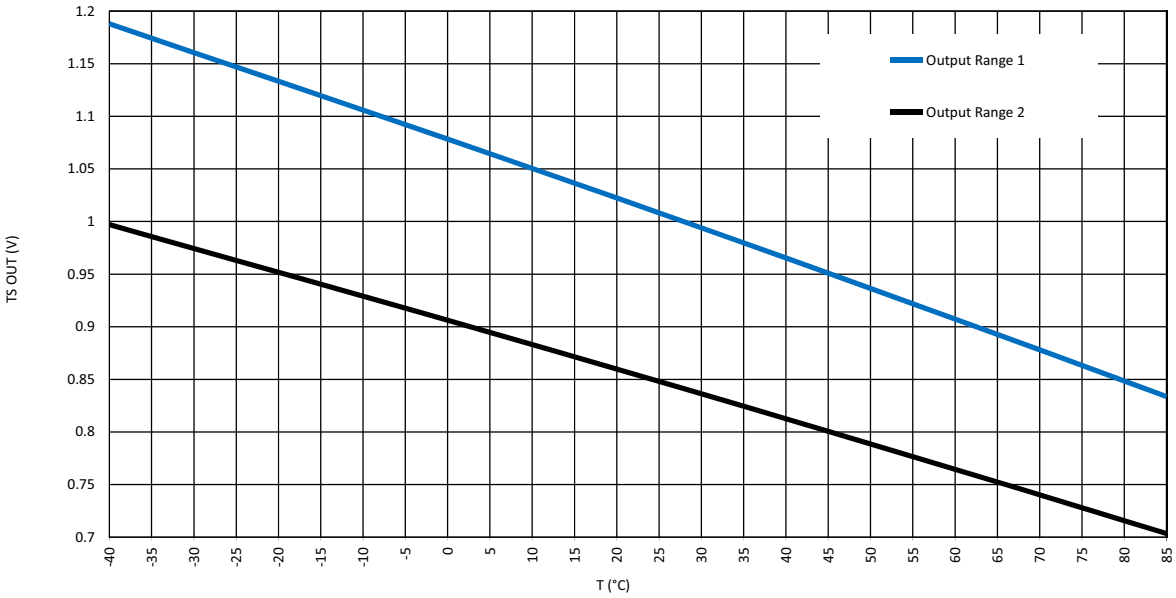



**Figure 94: TS Output vs. Temperature, $V_{DD}$ = 2.3 V to 5.5 V**

# 17 Dual, 2A P-FET Power Switches

## 17.1 POWER SWITCHES OVERVIEW

The SLG46867 has a dual-channel, 44 mΩ PMOS power switch designed to switch 1.71 V to 5.5 V power rails up to 2 A per channel.

Each P-FET Power Switch can be controlled internally via the ONx digital input of the P-FET Power Switch component in GreenPAK Designer, allowing the user to generate integrated mixed-signal control circuits, or externally via PWR_SW_ONx.

Whether controlled externally or internally, a low signal on either ONx or PWR_SW_ONx will close the P-FET Power Switch.

Each P-FET Power Switch need not be used in the same voltage domain as $V_{DD}$. However, when VIN is not tied to $V_{DD}$, using a large pull-up resistor on PWR_SW_ON0 and PWR_SW_ON1 is recommended to prevent current from flowing through the P-FET Power Switch while the device is not powered.

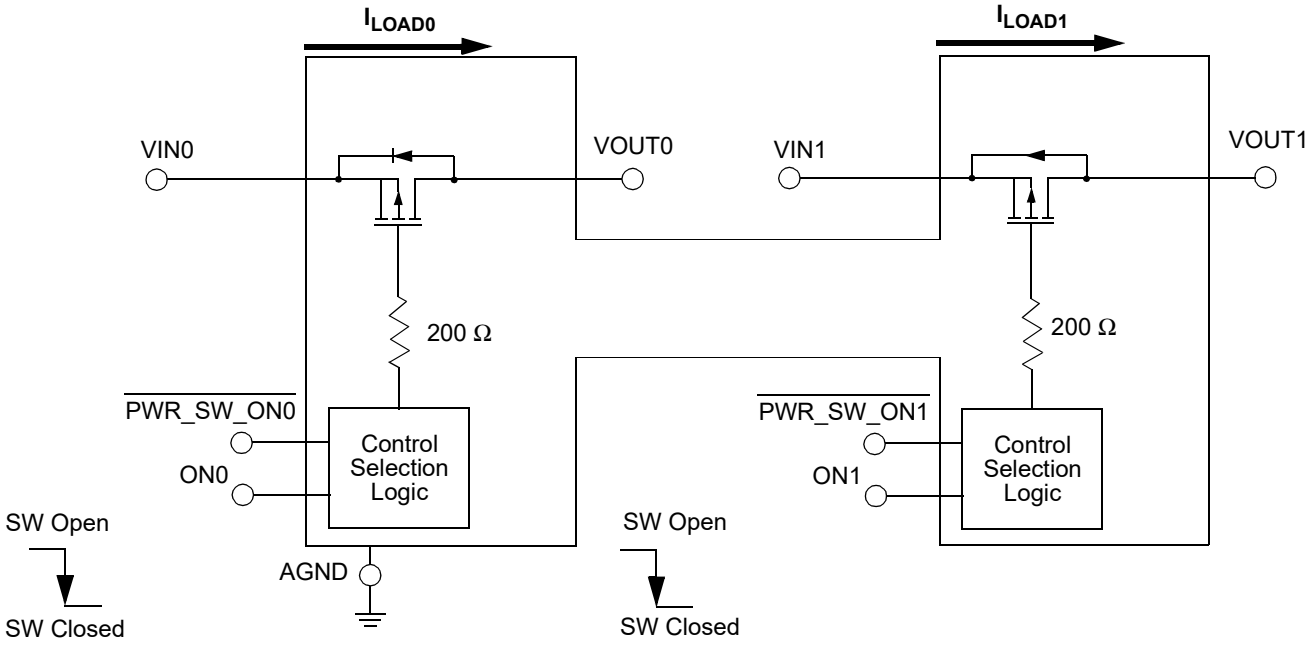



**Figure 95: Dual P-FET Power Switch**

### 17.2 DRIVING THE P-FET SWITCH

Gate of P-FET power switch can be driven by either internally generated signal or directly by external source connected to corresponding PWR_SW_ONx pin. Simplified circuit topologies are illustrated on Figure 96.

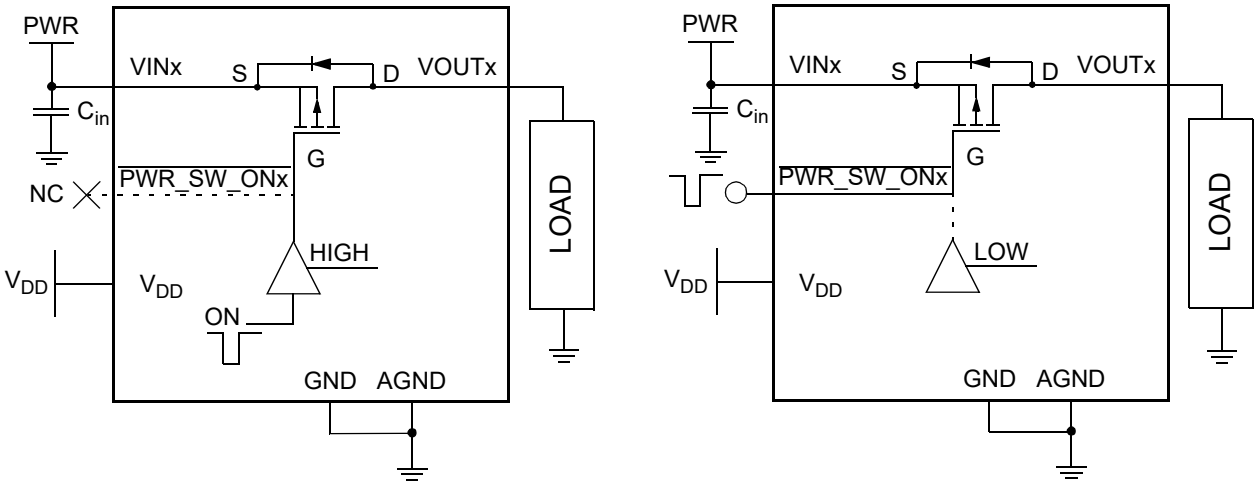



**Figure 96: Typical Circuit Topology for Internal (left) and External (right) drive modes**

Datasheet values for switching times are given for driving the resistive loads. The definitions of rise ($t_r$), fall ($t_f$) and delay times ($t_{d(on)}$ and $t_{d(off)}$) are given on Figure 97. To achieve highest switching performance circuit should be laid off using high speed PCB layout techniques.

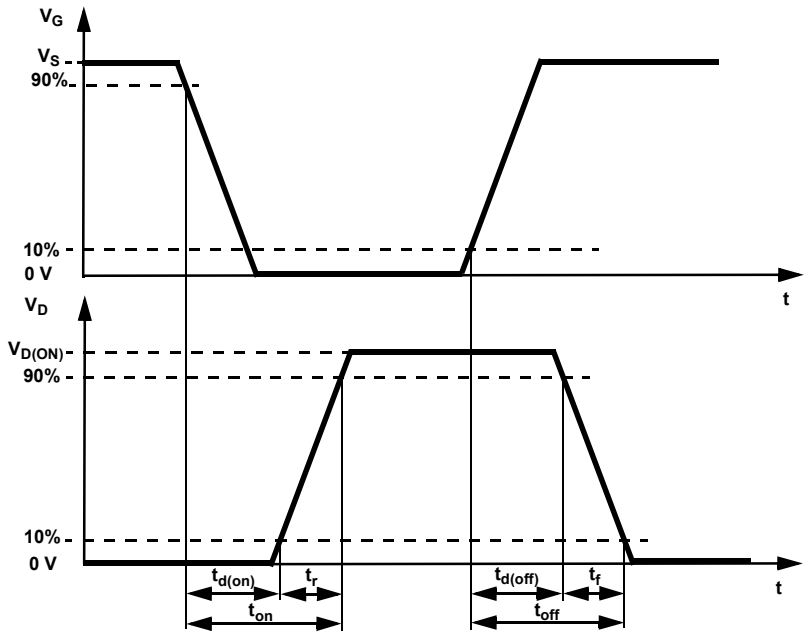



**Figure 97: Definitions for Rise, Fall and Switching Delay Times**

Typical resistive switching waveforms are given on Figure 99 and Figure 100. Note that fall time is dependent on load current (see section 17.4). At low loads turn off process can be delayed, therefore discharge circuit should be provided to reduce load turn off time in that case.

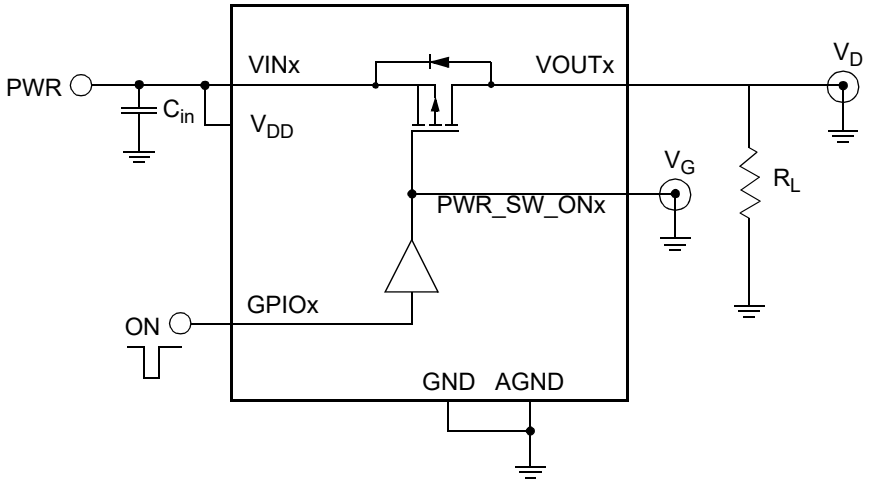



**Figure 98: Test Circuit for Typical Switching Waveforms**

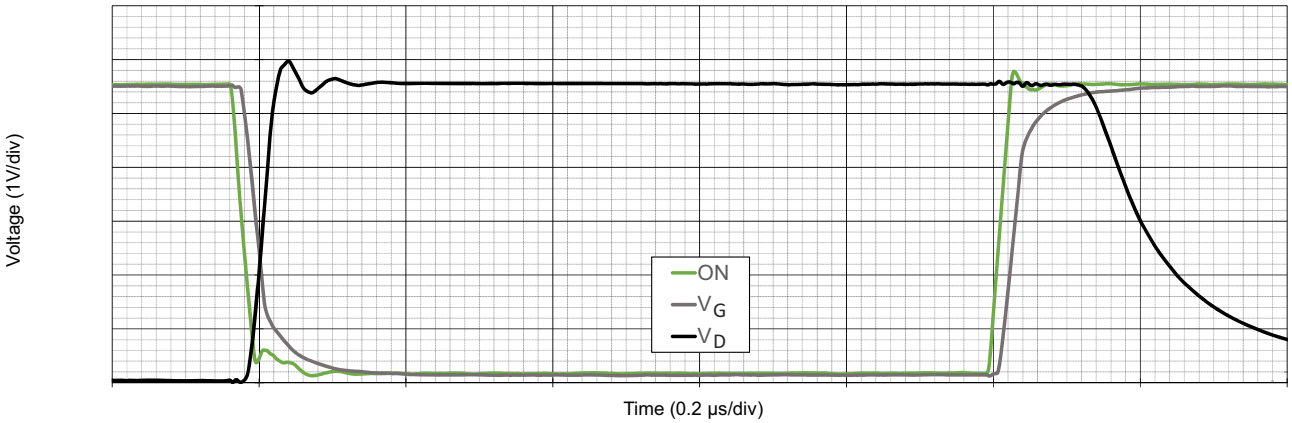



**Figure 99: Test Circuit for Typical Switching Waveforms (Internal Drive, Resistive Load, $R_L$ = 100 Ω, $V_{DD}$ = VIN = 5.5 V)**

**Figure 100: Test Circuit for Typical Switching Waveforms (Resistive Load, $R_L$ = 100 Ω, $V_{DD}$ = VIN = 1.71 V)**

## 17.3 POWER DISSIPATION

The junction temperature of the Power Switch depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the $RDS_{ON}$-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the Power Switch is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON0} \times I_{OUT0}^2) + (RDS_{ON1} \times I_{OUT1}^2)$$

where:

$PD_{TOTAL}$ = Total package power dissipation, in Watts (W)

$RDS_{ON}$ = Channel 0 and Channel 1 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{OUT}$ = Channel 0 and Channel 1 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \Theta_{JA} + T_A$$

where:

$T_J$ = Die junction temperature, in Celsius degrees (°C)

$\Theta_{JA}$ = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on PCB layout

$T_A$ = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the Power Switch power dissipation can also be calculated by taking into account the voltage drop across each switch ($V_{INx}$-$V_{OUTx}$) and the magnitude of that channel's output current ($I_{OUTx}$):

$$PD_{TOTAL} = [(V_{IN0}-V_{OUT0}) \times I_{OUT0}] + [(V_{IN1}-V_{OUT1}) \times I_{OUT1}] \text{ or}$$

$$PD_{TOTAL} = [(V_{IN0} - (R_{LOAD0} \times I_{OUT0})) \times I_{OUT0}] + [(V_{IN1} - (R_{LOAD1} \times I_{OU1})) \times I_{OUT1}]$$

where:

$PD_{TOTAL}$ = Total package power dissipation, in Watts (W)

$V_{IN}$ = Channel 0 and Channel 1 Input Voltage, in Volts (V), respectively

$R_{LOAD}$ = Channel 0 and Channel 1 Output Load Resistance, in Ohms (Ω), respectively

$I_{OUT}$ = Channel 0 and Channel 1 output current, in Amps (A), respectively

$V_{OUT}$ = Channel 0 and Channel 1 output voltage, or $R_{LOAD} \times I_{OUT}$, respectively

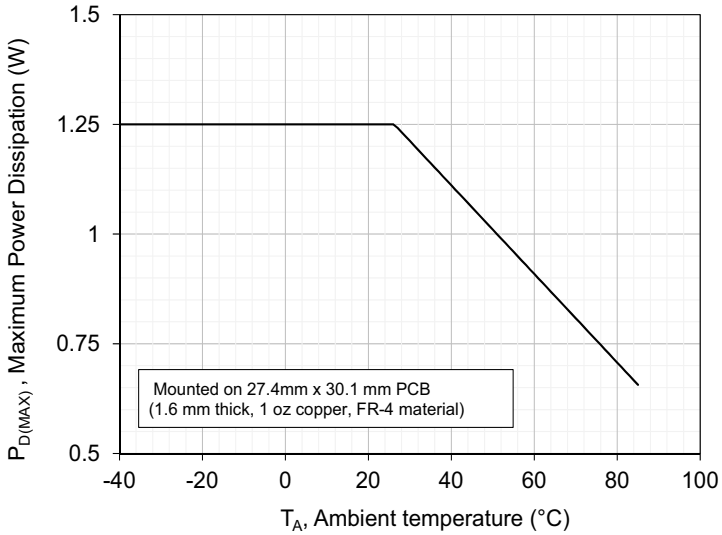



**Figure 101: Power Dissipation Derating Curve**

## 17.4 POWER SWITCH TYPICAL PERFORMANCE

$T_A$ = 25 °C, $V_{DD}$ = 5.5 V, unless otherwise noted.

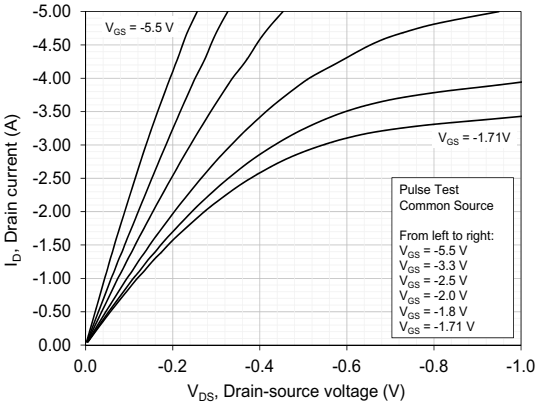



**Figure 102: Typical Output Characteristics**

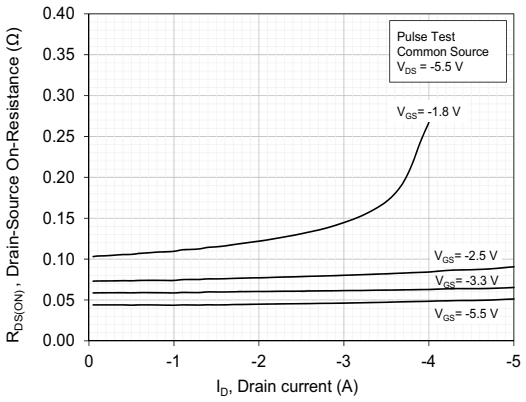



**Figure 103: Drain-Source On-Resistance vs. Drain Current**

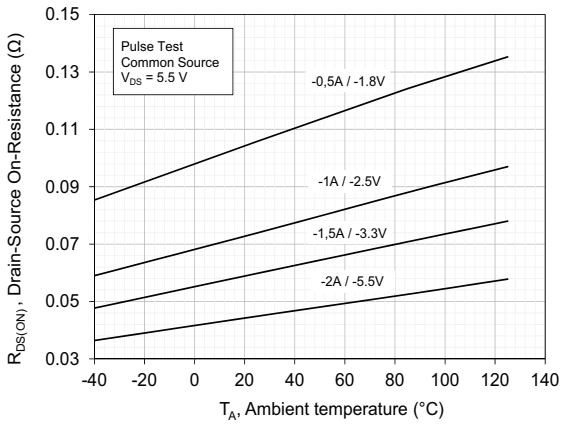



**Figure 104: Typical Drain-Source On-Resistance vs. Ambient Temperature**

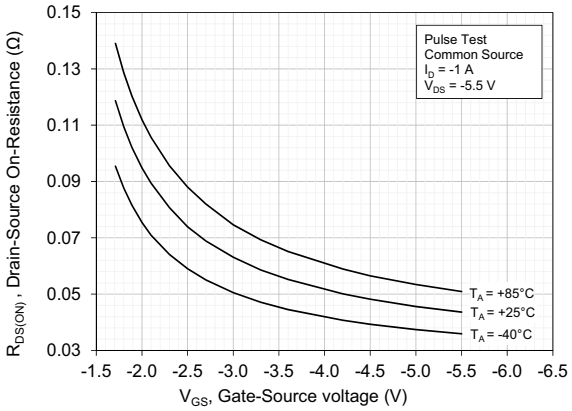



**Figure 105: Gate-Source On-Resistance Gate-Source Voltage**

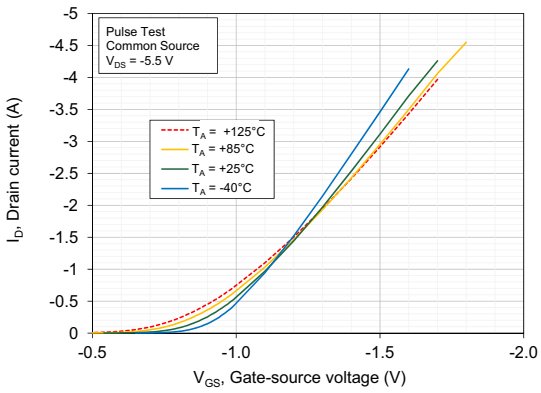



**Figure 106: Drain Current vs. Gate-Source Voltage**

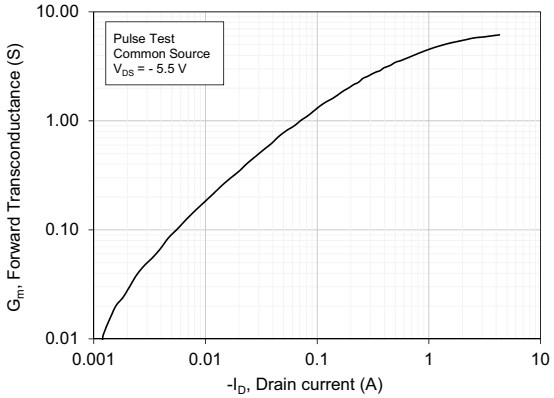



**Figure 107: Typical Forward Transconductance**

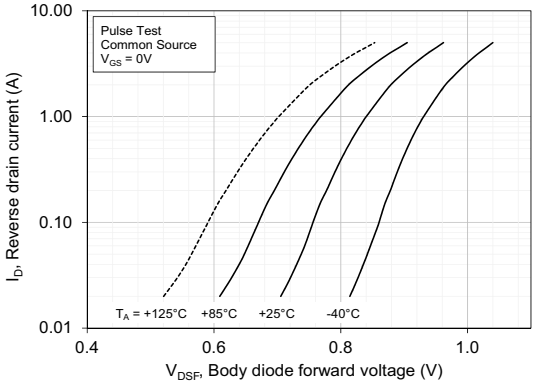



**Figure 108: Typical Drain-Source Diode Forward Voltage**

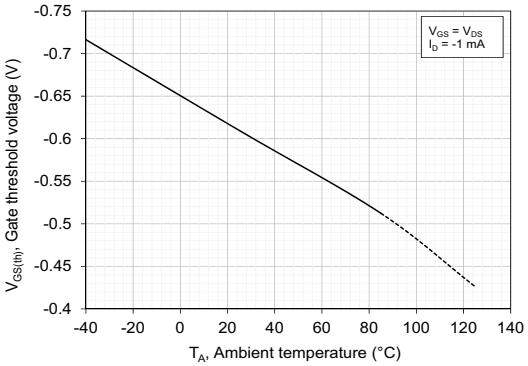



**Figure 109: Gate Threshold Voltage vs Ambient Temperature**

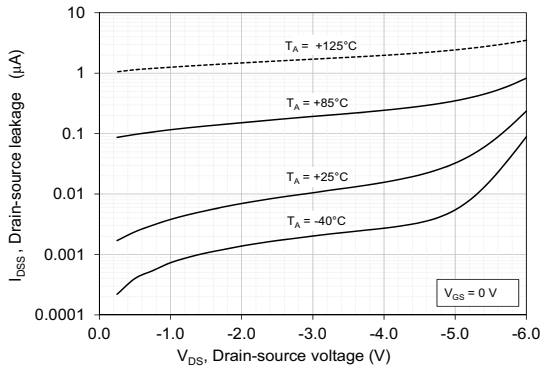



**Figure 110: Zero Gate Voltage Drain Current**

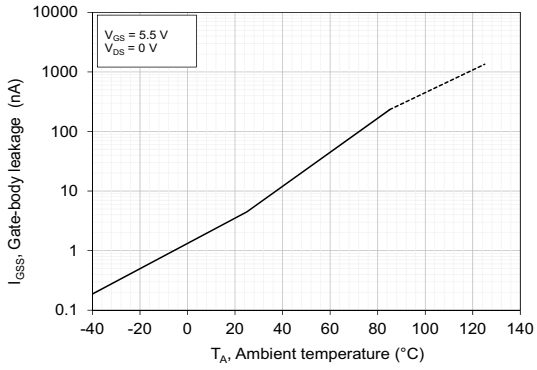



**Figure 111: Gate-Body Leakage vs. Ambient Temperature**

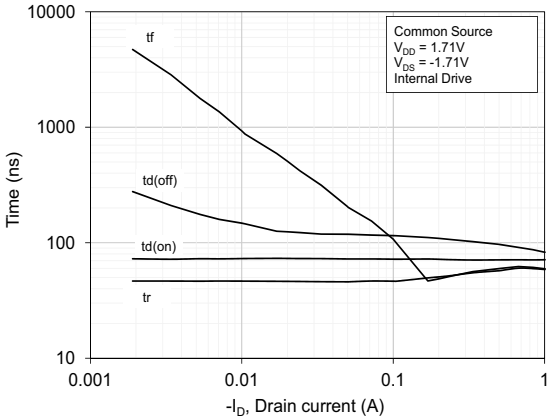



**Figure 112: Typical Switching Time (Internal Gate Drive) at $V_{DS}$ = 1.71 V**

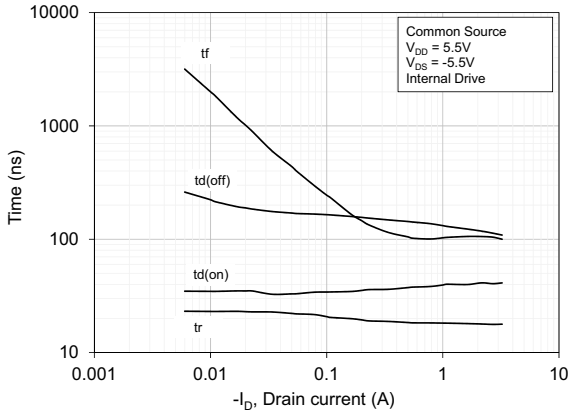



**Figure 113: Typical Switching Time (Internal Gate Drive) at $V_{DS}$ = 5.5 V**

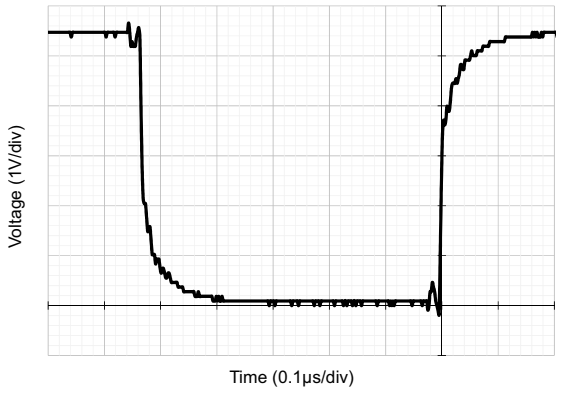



**Figure 114: Typical Gate Input Waveform, Internal Gate Drive Source (Switching Time Test)**

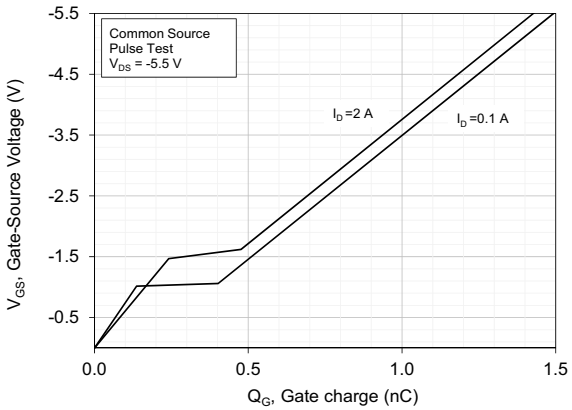



**Figure 115: Typical Gate Charge vs. Gate-Source Voltage**

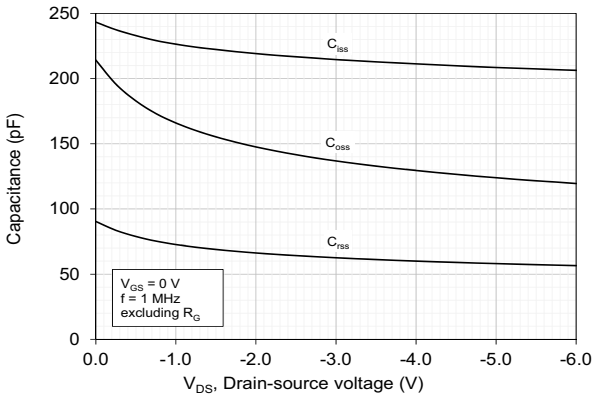



**Figure 116: Typical Capacitance vs. Drain-Source Voltage**

## 18 Register Definitions

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| **Matrix Output** | | | | | |
| 0 | 0 | LUT2_0 & DFF0 | OUT0:<br>IN0 of LUT2_0 or Clock Input of DFF0 | | |
| | 1 | | | | |
| | 2 | | | | |
| | 3 | | | | |
| | 4 | | | | |
| | 5 | | | | |
| | 6 | | OUT1<br>IN1 of LUT2_0 or Data Input of DFF0 | | |
| | 7 | | | | |
| 1 | 8 | | | | |
| | 9 | | | | |
| | 10 | | | | |
| | 11 | | | | |
| | 12 | LUT2_1 & DFF1 | OUT2:<br>IN0 of LUT2_1 or Clock Input of DFF1 | | |
| | 13 | | | | |
| | 14 | | | | |
| | 15 | | | | |
| 2 | 16 | | | | |
| | 17 | | | | |
| | 18 | | OUT3:<br>IN1 of LUT2_1 or Data Input of DFF1 | | |
| | 19 | | | | |
| | 20 | | | | |
| | 21 | | | | |
| | 22 | | | | |
| | 23 | | | | |
| 3 | 24 | LUT2_2 & DFF2 | OUT4:<br>IN0 of LUT2_2 or Clock Input of DFF2 | | |
| | 25 | | | | |
| | 26 | | | | |
| | 27 | | | | |
| | 28 | | | | |
| | 29 | | | | |
| | 30 | | OUT5:<br>IN1 of LUT2_2 or Data Input of DFF2 | | |
| | 31 | | | | |
| 4 | 32 | | | | |
| | 33 | | | | |
| | 34 | | | | |
| | 35 | | | | |
| | 36 | LUT2_3 & PGEN | OUT6:<br>IN0 of LUT2_3 or Clock Input of PGEN | | |
| | 37 | | | | |
| | 38 | | | | |
| | 39 | | | | |
| 5 | 40 | | | | |
| | 41 | | | | |
| | 42 | | OUT7:<br>IN1 of LUT2_3 or nRST of PGEN | | |
| | 43 | | | | |
| | 44 | | | | |
| | 45 | | | | |
| | 46 | | | | |
| | 47 | | | | |

| Address | | Signal Function | Register Bit Definition | $I^2C$ Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 6 | 48 | LUT3_0 & DFF3 | OUT8:<br>IN0 of LUT3_0 or CLK Input of DFF3 | | |
| | 49 | | | | |
| | 50 | | | | |
| | 51 | | | | |
| | 52 | | | | |
| | 53 | | | | |
| | 54 | | OUT9:<br>IN1 of LUT3_0 or Data of DFF3 | | |
| | 55 | | | | |
| 7 | 56 | | | | |
| | 57 | | | | |
| | 58 | | | | |
| | 59 | | | | |
| | 60 | | OUT10:<br>IN2 of LUT3_0 or nRST (nSET) of DFF3 | | |
| | 61 | | | | |
| | 62 | | | | |
| | 63 | | | | |
| 8 | 64 | | | | |
| | 65 | | | | |
| | 66 | LUT3_1 & DFF4 | OUT11:<br>IN0 of LUT3_1 or CLK Input of DFF4 | | |
| | 67 | | | | |
| | 68 | | | | |
| | 69 | | | | |
| | 70 | | | | |
| | 71 | | | | |
| 9 | 72 | LUT3_1 & DFF4 | OUT12:<br>IN1 of LUT3_1 or Data of DFF4 | | |
| | 73 | | | | |
| | 74 | | | | |
| | 75 | | | | |
| | 76 | | | | |
| | 77 | | | | |
| | 78 | | OUT13:<br>IN2 of LUT3_1 or nRST (nSET) of DFF4 | | |
| | 79 | | | | |
| A | 80 | | | | |
| | 81 | | | | |
| | 82 | | | | |
| | 83 | | | | |
| | 84 | LUT3_2 & DFF5 | OUT14:<br>IN0 of LUT3_2 or CLK Input of DFF5 | | |
| | 85 | | | | |
| | 86 | | | | |
| | 87 | | | | |
| B | 88 | | | | |
| | 89 | | | | |
| | 90 | | OUT15:<br>IN1 of LUT3_2 or Data of DFF5 | | |
| | 91 | | | | |
| | 92 | | | | |
| | 93 | | | | |
| | 94 | | | | |
| | 95 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| C | 96 | | OUT16:<br>IN2 of LUT3_2 or nRST (nSET) of DFF5 | | |
| | 97 | | | | |
| | 98 | | | | |
| | 99 | | | | |
| | 100 | | | | |
| | 101 | | | | |
| | 102 | LUT3_3 & DFF6 | OUT17:<br>IN0 of LUT3_3 or CLK Input of DFF6 | | |
| | 103 | | | | |
| D | 104 | | | | |
| | 105 | | | | |
| | 106 | | | | |
| | 107 | | | | |
| | 108 | | OUT18:<br>IN1 of LUT3_3 or Data of DFF6 | | |
| | 109 | | | | |
| | 110 | | | | |
| | 111 | | | | |
| E | 112 | | | | |
| | 113 | | | | |
| | 114 | | OUT19:<br>IN2 of LUT3_3 or nRST (nSET) of DFF6 | | |
| | 115 | | | | |
| | 116 | | | | |
| | 117 | | | | |
| | 118 | | | | |
| | 119 | | | | |
| F | 120 | LUT3_4 & DFF7 | OUT20:<br>IN0 of LUT3_4 or CLK Input of DFF7 | | |
| | 121 | | | | |
| | 122 | | | | |
| | 123 | | | | |
| | 124 | | | | |
| | 125 | | | | |
| | 126 | | OUT21:<br>IN1 of LUT3_4 or Data of DFF7 | | |
| | 127 | | | | |
| 10 | 128 | | | | |
| | 129 | | | | |
| | 130 | | | | |
| | 131 | | | | |
| | 132 | | OUT22:<br>IN2 of LUT3_4 or nRST (nSET) of DFF7 | | |
| | 133 | | | | |
| | 134 | | | | |
| | 135 | | | | |
| 11 | 136 | | | | |
| | 137 | | | | |
| | 138 | LUT3_5 & DFF8 | OUT23:<br>IN0 of LUT3_5 or CLK Input of DFF8 | | |
| | 139 | | | | |
| | 140 | | | | |
| | 141 | | | | |
| | 142 | | | | |
| | 143 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 12 | 144 | | OUT24:<br>IN1 of LUT3_5 or Data of DFF8 | | |
| | 145 | | | | |
| | 146 | | | | |
| | 147 | | | | |
| | 148 | | | | |
| | 149 | | | | |
| | 150 | | OUT25:<br>IN2 of LUT3_5 or nRST (nSET) of DFF8 | | |
| | 151 | | | | |
| 13 | 152 | | | | |
| | 153 | | | | |
| | 154 | | | | |
| | 155 | | | | |
| | 156 | LUT3_6 & DFF9 | OUT26:<br>IN0 of LUT3_6 or CLK Input of DFF9 | | |
| | 157 | | | | |
| | 158 | | | | |
| | 159 | | | | |
| 14 | 160 | | | | |
| | 161 | | | | |
| | 162 | | OUT27:<br>IN1 of LUT3_6 or Data of DFF9 | | |
| | 163 | | | | |
| | 164 | | | | |
| | 165 | | | | |
| | 166 | | | | |
| | 167 | | | | |
| 15 | 168 | LUT3_6 & DFF9 | OUT28:<br>IN2 of LUT3_6 or nRST (nSET) of DFF9 | | |
| | 169 | | | | |
| | 170 | | | | |
| | 171 | | | | |
| | 172 | | | | |
| | 173 | | | | |
| | 174 | LUT3_7 & DFF10 | OUT29:<br>IN0 of LUT3_7 or CLK Input of DFF10 | | |
| | 175 | | | | |
| 16 | 176 | | | | |
| | 177 | | | | |
| | 178 | | | | |
| | 179 | | | | |
| | 180 | | OUT30:<br>IN1 of LUT3_7 or Data of DFF10 | | |
| | 181 | | | | |
| | 182 | | | | |
| | 183 | | | | |
| 17 | 184 | | | | |
| | 185 | | | | |
| | 186 | | OUT31:<br>IN2 of LUT3_7 or nRST (nSET) of DFF10 | | |
| | 187 | | | | |
| | 188 | | | | |
| | 189 | | | | |
| | 190 | | | | |
| | 191 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 18 | 192 | LUT3_8 & DFF11 | OUT32:<br>IN0 of LUT3_8 or CLK Input of DFF11 | | |
| | 193 | | | | |
| | 194 | | | | |
| | 195 | | | | |
| | 196 | | | | |
| | 197 | | | | |
| | 198 | | OUT33:<br>IN1 of LUT3_8 or Data of DFF11 | | |
| | 199 | | | | |
| 19 | 200 | | | | |
| | 201 | | | | |
| | 202 | | | | |
| | 203 | | | | |
| | 204 | | OUT34:<br>IN2 of LUT3_8 or nRST (nSET) of DFF11 | | |
| | 205 | | | | |
| | 206 | | | | |
| | 207 | | | | |
| 1A | 208 | | | | |
| | 209 | | | | |
| | 210 | Multi_function4 | OUT35:<br>IN0 of LUT3_12 or CLK Input of DFF16<br>Delay4 Input (or Counter4 nRST Input) | | |
| | 211 | | | | |
| | 212 | | | | |
| | 213 | | | | |
| | 214 | | | | |
| | 215 | | | | |
| 1B | 216 | Multi_function4 | OUT36:<br>IN1 of LUT3_12 or nRST (nSET) of DFF16<br>Delay4 Input (or Counter4 nRST Input) | | |
| | 217 | | | | |
| | 218 | | | | |
| | 219 | | | | |
| | 220 | | | | |
| | 221 | | | | |
| | 222 | | OUT37:<br>IN2 of LUT3_12 or Data of DFF16<br>Delay4 Input (or Counter4 nRST Input) | | |
| | 223 | | | | |
| 1C | 224 | | | | |
| | 225 | | | | |
| | 226 | | | | |
| | 227 | | | | |
| | 228 | Multi_function5 | OUT38:<br>IN0 of LUT3_13 or CLK Input of DFF17<br>Delay5 Input (or Counter5 nRST Input) | | |
| | 229 | | | | |
| | 230 | | | | |
| | 231 | | | | |
| 1D | 232 | | | | |
| | 233 | | | | |
| | 234 | | OUT39:<br>IN1 of LUT3_13 or nRST (nSET) of DFF17<br>Delay5 Input (or Counter5 nRST Input) | | |
| | 235 | | | | |
| | 236 | | | | |
| | 237 | | | | |
| | 238 | | | | |
| | 239 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 1E | 240 | | OUT40:<br>IN2 of LUT3_13 or Data of DFF17<br>Delay5 Input (or Counter5 nRST Input) | | |
| | 241 | | | | |
| | 242 | | | | |
| | 243 | | | | |
| | 244 | | | | |
| | 245 | | | | |
| | 246 | Multi_function6 | OUT41:<br>IN0 of LUT3_14 or CLK Input of DFF18<br>Delay6 Input (or Counter6 nRST Input) | | |
| | 247 | | | | |
| 1F | 248 | | | | |
| | 249 | | | | |
| | 250 | | | | |
| | 251 | | | | |
| | 252 | | OUT42:<br>IN1 of LUT3_14 or nRST (nSET) of DFF18<br>Delay6 Input (or Counter6 nRST Input) | | |
| | 253 | | | | |
| | 254 | | | | |
| | 255 | | | | |
| 20 | 256 | | | | |
| | 257 | | | | |
| | 258 | | OUT43:<br>IN2 of LUT3_14 or Data of DFF18<br>Delay6 Input (or Counter6 nRST Input) | | |
| | 259 | | | | |
| | 260 | | | | |
| | 261 | | | | |
| | 262 | | | | |
| | 263 | | | | |
| 21 | 264 | Multi_function7 | OUT44:<br>IN0 of LUT3_15 or CLK Input of DFF19<br>Delay7 Input (or Counter7 nRST Input) | | |
| | 265 | | | | |
| | 266 | | | | |
| | 267 | | | | |
| | 268 | | | | |
| | 269 | | | | |
| | 270 | | OUT45:<br>IN1 of LUT3_15 or nRST (nSET) of DFF19<br>Delay7 Input (or Counter7 nRST Input) | | |
| | 271 | | | | |
| 22 | 272 | | | | |
| | 273 | | | | |
| | 274 | | | | |
| | 275 | | | | |
| | 276 | | OUT46:<br>IN2 of LUT3_15 or Data of DFF19<br>Delay7 Input (or Counter7 nRST Input) | | |
| | 277 | | | | |
| | 278 | | | | |
| | 279 | | | | |
| 23 | 280 | | | | |
| | 281 | | | | |
| | 282 | LUT3_16 & Pipe Delay (RIPP CNT) | OUT47:<br>IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT | | |
| | 283 | | | | |
| | 284 | | | | |
| | 285 | | | | |
| | 286 | | | | |
| | 287 | | | | |

| Address | | Signal Function | Register Bit Definition | $I^2C$ Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 24 | 288 | | OUT48:<br>IN1 of LUT3_16 or nRST of Pipe Delay or STB of RIPP CNT | | |
| | 289 | | | | |
| | 290 | | | | |
| | 291 | | | | |
| | 292 | | | | |
| | 293 | | | | |
| | 294 | | OUT49:<br>IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT | | |
| | 295 | | | | |
| 25 | 296 | | | | |
| | 297 | | | | |
| | 298 | | | | |
| | 299 | | | | |
| | 300 | LUT4_DFF12 | OUT50:<br>IN0 of LUT4_0 or CLK Input of DFF12 | | |
| | 301 | | | | |
| | 302 | | | | |
| | 303 | | | | |
| 26 | 304 | | | | |
| | 305 | | OUT51:<br>IN1 of LUT4_0 or Data of DFF12 | | |
| | 306 | | | | |
| | 307 | | | | |
| | 308 | | | | |
| | 309 | | | | |
| | 310 | | | | |
| | 311 | | | | |
| 27 | 312 | | OUT52:<br>IN2 of LUT4_0 or nRST (nSET) of DFF12 | | |
| | 313 | | | | |
| | 314 | | | | |
| | 315 | | | | |
| | 316 | | | | |
| | 317 | | | | |
| | 318 | | OUT53:<br>IN3 of LUT4_0 | | |
| | 319 | | | | |
| 28 | 320 | | | | |
| | 321 | | | | |
| | 322 | | | | |
| | 323 | | | | |
| | 324 | Programmable delay | OUT54: Programmable delay/edge detect input | | |
| | 325 | | | | |
| | 326 | | | | |
| | 327 | | | | |
| 29 | 328 | | | | |
| | 329 | | | | |
| | 330 | Filter/Edge Detect | OUT55: Filter/Edge detect input | | |
| | 331 | | | | |
| | 332 | | | | |
| | 333 | | | | |
| | 334 | | | | |
| | 335 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 2A | 336 | GPIO0 | OUT56: GPIO0 DOUT | | |
| | 337 | | | | |
| | 338 | | | | |
| | 339 | | | | |
| | 340 | | | | |
| | 341 | | | | |
| | 342 | GPIO1 | OUT57: GPIO1 DOUT | | |
| | 343 | | | | |
| 2B | 344 | | | | |
| | 345 | | | | |
| | 346 | | | | |
| | 347 | | | | |
| | 348 | GPIO2 | OUT58: GPIO2 DOUT | | |
| | 349 | | | | |
| | 350 | | | | |
| | 351 | | | | |
| 2C | 352 | | | | |
| | 353 | | | | |
| | 354 | | OUT59: GPIO2 DOUT OE | | |
| | 355 | | | | |
| | 356 | | | | |
| | 357 | | | | |
| | 358 | | | | |
| | 359 | | | | |
| 2D | 360 | Power Switch ON0, Digital Output | OUT60: Power Switch ON0, Digital Output | | |
| | 361 | | | | |
| | 362 | | | | |
| | 363 | | | | |
| | 364 | | | | |
| | 365 | | | | |
| | 366 | | OUT61: Reserved | | |
| | 367 | | | | |
| 2E | 368 | | | | |
| | 369 | | | | |
| | 370 | | | | |
| | 371 | | | | |
| | 372 | Power Switch ON1, Digital Output | OUT62: Power Switch ON1, Digital Output | | |
| | 373 | | | | |
| | 374 | | | | |
| | 375 | | | | |
| 2F | 376 | | | | |
| | 377 | | | | |
| | 378 | GPIO4 | OUT63: GPIO4 DOUT | | |
| | 379 | | | | |
| | 380 | | | | |
| | 381 | | | | |
| | 382 | | | | |
| | 383 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 30 | 384 | | OUT64: GPIO4 DOUT OE | | |
| | 385 | | | | |
| | 386 | | | | |
| | 387 | | | | |
| | 388 | | | | |
| | 389 | | | | |
| | 390 | GPIO5 | OUT65: GPIO5 DOUT | | |
| | 391 | | | | |
| 31 | 392 | | | | |
| | 393 | | | | |
| | 394 | | | | |
| | 395 | | | | |
| | 396 | | OUT66: GPIO5 DOUT OE | | |
| | 397 | | | | |
| | 398 | | | | |
| | 399 | | | | |
| 32 | 400 | | | | |
| | 401 | | | | |
| | 402 | GPIO6 | OUT67: GPIO6 DOUT | | |
| | 403 | | | | |
| | 404 | | | | |
| | 405 | | | | |
| | 406 | | | | |
| | 407 | | | | |
| 33 | 408 | GPIO6 | OUT68: GPIO6 DOUT OE | | |
| | 409 | | | | |
| | 410 | | | | |
| | 411 | | | | |
| | 412 | | | | |
| | 413 | | | | |
| | 414 | GPIO7 | OUT69: GPIO7 DOUT | | |
| | 415 | | | | |
| 34 | 416 | | | | |
| | 417 | | | | |
| | 418 | | | | |
| | 419 | | | | |
| | 420 | | OUT70: GPIO7 DOUT OE | | |
| | 421 | | | | |
| | 422 | | | | |
| | 423 | | | | |
| 35 | 424 | | | | |
| | 425 | | | | |
| | 426 | GPIO8 | OUT71: GPIO8 DOUT | | |
| | 427 | | | | |
| | 428 | | | | |
| | 429 | | | | |
| | 430 | | | | |
| | 431 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 36 | 432 | | OUT72: GPIO8 DOUT OE | | |
| | 433 | | | | |
| | 434 | | | | |
| | 435 | | | | |
| | 436 | | | | |
| | 437 | | | | |
| | 438 | GPIO9 | OUT73: GPIO9 DOUT | | |
| | 439 | | | | |
| 37 | 440 | | | | |
| | 441 | | | | |
| | 442 | | | | |
| | 443 | | | | |
| | 444 | | OUT74: GPIO9 DOUT OE | | |
| | 445 | | | | |
| | 446 | | | | |
| | 447 | | | | |
| 38 | 448 | | | | |
| | 449 | | | | |
| | 450 | ACMP0H | OUT75: pdb of ACMP0H | | |
| | 451 | | | | |
| | 452 | | | | |
| | 453 | | | | |
| | 454 | | | | |
| | 455 | | | | |
| 39 | 456 | ACMP1H | OUT76: pdb of ACMP1H | | |
| | 457 | | | | |
| | 458 | | | | |
| | 459 | | | | |
| | 460 | | | | |
| | 461 | | | | |
| | 462 | ACMP2L | OUT77: pdb of ACMP2L | | |
| | 463 | | | | |
| 3A | 464 | | | | |
| | 465 | | | | |
| | 466 | | | | |
| | 467 | | | | |
| | 468 | ACMP3L | OUT78: pdb of ACMP3L | | |
| | 469 | | | | |
| | 470 | | | | |
| | 471 | | | | |
| 3B | 472 | | | | |
| | 473 | | | | |
| | 474 | Temp Sensor | OUT79: pdb of Temp sensor | | |
| | 475 | | | | |
| | 476 | | | | |
| | 477 | | | | |
| | 478 | | | | |
| | 479 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 3C | 480 | LFOSC | OUT80: LFOSC ENABLE | | |
| | 481 | | | | |
| | 482 | | | | |
| | 483 | | | | |
| | 484 | | | | |
| | 485 | | | | |
| | 486 | RCOSC | OUT81: RCOSC ENABLE | | |
| | 487 | | | | |
| 3D | 488 | | | | |
| | 489 | | | | |
| | 490 | | | | |
| | 491 | | | | |
| | 492 | RINGOSC | OUT82: RINGOSC ENABLE | | |
| | 493 | | | | |
| | 494 | | | | |
| | 495 | | | | |
| 3E | 496 | Multi_function0 | OUT83:<br>IN0 of LUT4_1 or CLK Input of DFF20<br>Delay0 Input (or Counter0 nRST Input) | | |
| | 497 | | | | |
| | 498 | | | | |
| | 499 | | | | |
| | 500 | | | | |
| | 501 | | | | |
| | 502 | | | | |
| | 503 | | | | |
| 3F | 504 | Multi_function0 | OUT84:<br>IN1 of LUT4_1 or nRST of DFF20<br>Delay0 Input (or Counter0 nRST Input)<br>Delay/Counter0 External CLK source | | |
| | 505 | | | | |
| | 506 | | | | |
| | 507 | | | | |
| | 508 | | | | |
| | 509 | | | | |
| | 510 | | OUT85:<br>IN2 of LUT4_1 or nSET of DFF20<br>Delay0 Input (or Counter0 nRST Input)<br>Delay/Counter0 External CLK source<br>KEEP Input of FSM0 | | |
| | 511 | | | | |
| 40 | 512 | | | | |
| | 513 | | | | |
| | 514 | | | | |
| | 515 | | | | |
| | 516 | | OUT86:<br>IN3 of LUT4_1 or Data of DFF20<br>Delay0 Input (or Counter0 nRST Input)<br>UP Input of FSM0 | | |
| | 517 | | | | |
| | 518 | | | | |
| | 519 | | | | |
| 41 | 520 | | | | |
| | 521 | | | | |
| | 522 | Multi_function1 | OUT87:<br>IN0 of LUT3_9 or CLK Input of DFF13<br>Delay1 Input (or Counter1 nRST Input) | | |
| | 523 | | | | |
| | 524 | | | | |
| | 525 | | | | |
| | 526 | | | | |
| | 527 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 42 | 528 | | OUT88:<br>IN1 of LUT3_9 or nRST (nSET) of DFF13<br>Delay1 Input (or Counter1 nRST Input) | | |
| | 529 | | | | |
| | 530 | | | | |
| | 531 | | | | |
| | 532 | | | | |
| | 533 | | | | |
| | 534 | | OUT89:<br>IN2 of LUT3_9 or Data of DFF13<br>Delay1 Input (or Counter1 nRST Input) | | |
| | 535 | | | | |
| 43 | 536 | | | | |
| | 537 | | | | |
| | 538 | | | | |
| | 539 | | | | |
| | 540 | Multi_function2 | OUT90:<br>IN0 of LUT3_10 or CLK Input of DFF14<br>Delay2 Input (or Counter2 nRST Input) | | |
| | 541 | | | | |
| | 542 | | | | |
| | 543 | | | | |
| 44 | 544 | | | | |
| | 545 | | | | |
| | 546 | | OUT91:<br>IN1 of LUT3_10 or nRST (nSET) of DFF14<br>Delay2 Input (or Counter2 nRST Input) | | |
| | 547 | | | | |
| | 548 | | | | |
| | 549 | | | | |
| | 550 | | | | |
| | 551 | | | | |
| 45 | 552 | Multi_function2 | OUT92:<br>IN2 of LUT3_10 or Data of DFF14<br>Delay2 Input (or Counter2 nRST Input) | | |
| | 553 | | | | |
| | 554 | | | | |
| | 555 | | | | |
| | 556 | | | | |
| | 557 | | | | |
| | 558 | Multi_function3 | OUT93:<br>IN0 of LUT3_11 or CLK Input of DFF15<br>Delay3 Input (or Counter3 nRST Input) | | |
| | 559 | | | | |
| 46 | 560 | | | | |
| | 561 | | | | |
| | 562 | | | | |
| | 563 | | | | |
| | 564 | | OUT94:<br>IN1 of LUT3_11 or nRST (nSET) of DFF15<br>Delay3 Input (or Counter3 nRST Input) | | |
| | 565 | | | | |
| | 566 | | | | |
| | 567 | | | | |
| 47 | 568 | | | | |
| | 569 | | | | |
| | 570 | | OUT95:<br>IN2 of LUT3_11 or Data of DFF15<br>Delay3 Input (or Counter3 nRST Input) | | |
| | 571 | | | | |
| | 572 | | | | |
| | 573 | | | | |
| | 574 | | | | |
| | 575 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 48 | 576 | Matrix Input 0 | GND | | |
| | 577 | Matrix Input 1 | LUT2_0/DFF0 output | | |
| | 578 | Matrix Input 2 | LUT2_1/DFF1 output | | |
| | 579 | Matrix Input 3 | LUT2_2/DFF2 output | | |
| | 580 | Matrix Input 4 | LUT2_3/PGEN output | | |
| | 581 | Matrix Input 5 | LUT3_0/DFF3 output | | |
| | 582 | Matrix Input 6 | LUT3_1/DFF4 output | | |
| | 583 | Matrix Input 7 | LUT3_2/DFF5 output | | |
| 49 | 584 | Matrix Input 8 | LUT3_3/DFF6 output | | |
| | 585 | Matrix Input 9 | LUT3_4/DFF7 output | | |
| | 586 | Matrix Input 10 | LUT3_5/DFF8 output | | |
| | 587 | Matrix Input 11 | LUT3_6/DFF9 output | | |
| | 588 | Matrix Input 12 | LUT3_7/DFF10 output | | |
| | 589 | Matrix Input 13 | LUT3_8/DFF11 output | | |
| | 590 | Matrix Input 14 | CNT0 output | | |
| | 591 | Matrix Input 15 | MLT0_LUT4/DFF_OUT | | |
| 4A | 592 | Matrix Input 16 | CNT1 output | | |
| | 593 | Matrix Input 17 | MLT1_LUT3/DFF_OUT | | |
| | 594 | Matrix Input 18 | CNT2 output | | |
| | 595 | Matrix Input 19 | MLT2_LUT3/DFF_OUT | | |
| | 596 | Matrix Input 20 | CNT3 output | | |
| | 597 | Matrix Input 21 | MLT3_LUT3/DFF_OUT | | |
| | 598 | Matrix Input 22 | CNT4 output | | |
| | 599 | Matrix Input 23 | MLT4_LUT3/DFF_OUT | | |
| 4B | 600 | Matrix Input 24 | CNT5 output | | |
| | 601 | Matrix Input 25 | MLT5_LUT3/DFF_OUT | | |
| | 602 | Matrix Input 26 | CNT6 output | | |
| | 603 | Matrix Input 27 | MLT6_LUT3/DFF_OUT | | |
| | 604 | Matrix Input 28 | CNT7 output | | |
| | 605 | Matrix Input 29 | MLT7_LUT3/DFF_OUT | | |
| | 606 | Matrix Input 30 | LUT3_16/Ripple CNT/Pipe Delay_out0 | | |
| | 607 | Matrix Input 31 | Ripple CNT/Pipe Delay_out1 | | |
| 4C | 608 | Matrix Input 32 | GPIO0 digital input or I2C_virtual_0 Input | | |
| | 609 | Matrix Input 33 | GPIO1 digital input or I2C_virtual_1 Input | | |
| | 610 | Matrix Input 34 | I2C_virtual_2 Input | | |
| | 611 | Matrix Input 35 | I2C_virtual_3 Input | | |
| | 612 | Matrix Input 36 | I2C_virtual_4 Input | | |
| | 613 | Matrix Input 37 | I2C_virtual_5 Input | | |
| | 614 | Matrix Input 38 | I2C_virtual_6 Input | | |
| | 615 | Matrix Input 39 | I2C_virtual_7 Input | | |
| 4D | 616 | Matrix Input 40 | Ripple CNT_out2 | | |
| | 617 | Matrix Input 41 | LUT4_0/DFF12 output | | |
| | 618 | Matrix Input 42 | Programmable Delay Edge Detect Output | | |
| | 619 | Matrix Input 43 | Edge Detect Filter Output | | |
| | 620 | Matrix Input 44 | GPI0 Digital Input | | |
| | 621 | Matrix Input 45 | GPIO2 Digital Input | | |
| | 622 | Matrix Input 46 | Power Switch ON0, Digital Input | | |
| | 623 | Matrix Input 47 | GPIO4 Digital Input | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 4E | 624 | Matrix Input 48 | GPIO5 Digital Input | | |
| | 625 | Matrix Input 49 | GPIO6 Digital Input | | |
| | 626 | Matrix Input 50 | GPIO7 Digital Input | | |
| | 627 | Matrix Input 51 | GPIO8 Digital Input | | |
| | 628 | Matrix Input 52 | GPIO9 Digital Input | | |
| | 629 | Matrix Input 53 | LFOSC output 0 | | |
| | 630 | Matrix Input 54 | RCOSC output 0 | | |
| | 631 | Matrix Input 55 | RINGOSC output | | |
| 4F | 632 | Matrix Input 56 | ACMP0H Output (normal speed) | | |
| | 633 | Matrix Input 57 | ACMP1H Output (normal speed) | | |
| | 634 | Matrix Input 58 | ACMP2L Output (low speed) | | |
| | 635 | Matrix Input 59 | ACMP3L output (low speed) | | |
| | 636 | Matrix Input 60 | LFOSC output 1 | | |
| | 637 | Matrix Input 61 | RCOSC output 1 | | |
| | 638 | Matrix Input 62 | Matrix nRST | | |
| | 639 | Matrix Input 63 | VDD | | |
| 50 | 640 | BG CHOP OFF | 0: CHOP enable<br>1: chopper off | | |
| | 641 | BG Chopper clock test enable | 1: enable | | |
| | 642 | Bandgap internal voltage output to IO enable | 1: enable | | |
| | 643 | Bandgap power down control | 0: always on<br>1: power down if no function enable it (ACMP, Vref, TS) | | |
| | 644 | Reserved | | | |
| | 645 | Reserved | | | |
| | 646 | Reserved | | | |
| | 647 | ACMP3L wake sleep enable | 1: enable<br>0: disable | | |
| 51 | 648 | VrefO0 register power on/off | 1: on<br>0: off | | |
| | 649 | VrefO0 power down selection | 0: come from register [648]<br>1: come from matrix out92 | | |
| | 650 | VrefO1 register power on/off | 1: on<br>0: off | | |
| | 651 | ACMP0H hysteresis | 00: 0 mV<br>01: 32 mV<br>10: 64 mV<br>11: 192 mV | | |
| | 652 | | | | |
| | 653 | Reserved | | | |
| | 654 | ACMP0_H input buffer enable | 1: enable | | |
| | 655 | Reserved | | | |
| 52 | 656 | ACMP0H input tie to VDD enable | 1: enable | | |
| | 657 | ACMP1_H positive input come from ACMP0_H's input mux output enable; 1:enable | | | |
| | 658 | Reserved | | | |
| | 659 | ACMP1H hysteresis | 00: 0 mV<br>01: 32 mV<br>10: 64 mV<br>11: 196 mV | | |
| | 660 | | | | |
| | 661 | ACMP1H input buffer enable | 1: enable | | |
| | 662 | Reserved | | | |
| | 663 | ACMP2L positive input come from ACMP0H's input mux output enable | 1:enable | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 53 | 664 | ACMP2L positive input come from ACMP1H's input mux output enable | 1: enable | | |
| | 665 | ACMP2L hysteresis | 00: 0 mV<br>01: 32 mV<br>10: 64 mV<br>11: 196 mV | | |
| | 666 | | | | |
| | 667 | Reserved | | | |
| | 668 | Reserved | | | |
| | 669 | ACMP3_L hysteresis | 00: 0 mV<br>01: 32 mV<br>10: 64 mV<br>11: 196 mV | | |
| | 670 | | | | |
| | 671 | Reserved | | | |
| 54 | 672 | Reserved | | | |
| | 673 | ACMP3_L positive input come from ACMP2L's input mux output enable | 1: enable | | |
| | 674 | Temp sensor register pdb control | 0: power down<br>1: power on | | |
| | 675 | Temp sensor register pdb select | 0: come from register<br>1: come from Matrix | | |
| | 676 | Temp sensor range select | 0: 0.62V ~ 0.99V (TYP)<br>1: 0.75V ~ 1.2V (TYP) | | |
| | 677 | Vref0 output OP | 0: disable<br>1: enable | | |
| | 678 | Vref0 input selection | 00: None<br>01: ACMP0H Vref<br>10: ACMP1H Vref<br>11: temp sensor | | |
| | 679 | | | | |
| 55 | 680 | Vref1 output OP | 0: disable<br>1: enable | | |
| | 681 | Vref1 input selection | 00: None<br>01: ACMP2L Vref<br>10: ACMP3L Vref | | |
| | 682 | | | | |
| | 683 | VBG fine tune selection | 0000: 1.194, 0001:1.195, 0011:1.196,<br>0100:1.197, 0101:1.198, 0110:1.199<br>0111:1.2, 1000:1.201, 1001:1.202,<br>1010:1.203, 1011:1.204, 1100:1.205,<br>1101:1.206, 1110:1.207, 1111:1.208 | | |
| | 684 | | | | |
| | 685 | | | | |
| | 686 | | | | |
| | 687 | ACMP0H Wake/sleep enable | | | |
| 56 | 688 | ACMP1H Wake/sleep enable | | | |
| | 689 | ACMP wake/sleep time selection | 0: short time<br>1: normal w/s | | |
| | 690 | ACMP0H 100 uA current source enable | | | |
| | 691 | Reserve for ACMP | | | |
| | 692 | BG Trimming source select | 0: VBG<br>1: Vref normal 2.048 output | | |
| | 693 | ACMP3L input come from Temp sensor output enable | | | |
| | 694 | VrefO1 power down selection | 0: come from register [650]<br>1: come from matrix OUT92 | | |
| | 695 | ACMP2L wake sleep enable | 0: disable<br>1: enable | | |
| 57 | 696 | ACMP0H Gain divider | ACMP gain divider select:<br>00: 1X<br>01:0.5X<br>10:0.33X<br>11:0.25X | | |
| | 697 | | | | |
| | 698 | ACMP0H Vref0 | ACMP Vref select:<br>000000: 32mV ~<br>111110: 2.016V/ step=32mV<br>111111: External Vref | | |
| | 699 | | | | |
| | 700 | | | | |
| | 701 | | | | |
| | 702 | | | | |
| | 703 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 58 | 704 | ACMP1L Gain divider | ACMP gain divider select:<br>00: 1X<br>01:0.5X<br>10:0.33X<br>11:0.25X | | |
| | 705 | | | | |
| | 706 | ACMP1L Vref0 | ACMP Vref select:<br>000000: 32mV ~ 1<br>11110: 2.016V/ step=32mV<br>111111: External Vref | | |
| | 707 | | | | |
| | 708 | | | | |
| | 709 | | | | |
| | 710 | | | | |
| | 711 | | | | |
| 59 | 712 | ACMP2L Gain divider | ACMP gain divider select:<br>00: 1X<br>01:0.5X<br>10:0.33X<br>11:0.25X | | |
| | 713 | | | | |
| | 714 | ACMP2L Vref1 | ACMP Vref select:<br>000000: 32mV ~<br>111110: 2.016V/ step=32mV<br>111111: External Vref | | |
| | 715 | | | | |
| | 716 | | | | |
| | 717 | | | | |
| | 718 | | | | |
| | 719 | | | | |
| 5A | 720 | ACMP3L Gain divider | ACMP gain divider select:<br>00: 1X<br>01:0.5X<br>10:0.33X<br>11:0.25X | | |
| | 721 | | | | |
| | 722 | ACMP3L Vref1 | ACMP Vref select:<br>000000: 32mV ~<br>111110: 2.016V/ step=32mV<br>111112: External Vref | | |
| | 723 | | | | |
| | 724 | | | | |
| | 725 | | | | |
| | 726 | | | | |
| | 727 | | | | |
| **RCOSC** | | | | | |
| 5B | 728 | RCOSC turn on by register | when matrix output enable/pd control signal=0:<br>0: auto on by delay cells<br>1: always on | | |
| | 729 | matrix power down or on select | 0: matrix down<br>1: matrix on | | |
| | 730 | external clock source enable | 0: internal RCOSC<br>1: external clock from GPIO2 | | |
| | 731 | post divider ratio control | 00: div 1<br>01: div 2<br>10: div 4<br>11: div 8 | | |
| | 732 | | | | |
| | 733 | matrix divider ratio control | 000: /1, 001:/2, 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64 | | |
| | 734 | | | | |
| | 735 | | | | |
| 5C | 736 | matrix out enable | 0: disable<br>1: enable | | |
| | 737 | Reserved | | | |
| | 738 | Reserved | | | |
| | 739 | Reserved | | | |
| **RingOSC** | | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 5C | 740 | RingOSC turn on by register | when matrix output enable/pd control signal=0:<br>0: auto on by delay cells<br>1: always on | | |
| | 741 | matrix power down or on select | 0: matrix down<br>1: matrix on | | |
| | 742 | external clock source enable | 0: internal RingOSC<br>1: external clock from GPIO8 | | |
| | 743 | matrix out enable | 0: disable<br>1: enable | | |
| 5D | 744 | post divider ratio control | 00: div 1<br>01: div 2<br>10: div 4<br>11: div 8 | | |
| | 745 | | | | |
| 5D | 746 | matrix divider ratio control | 000: /1, 001:/2, 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64 | | |
| | 747 | | | | |
| | 748 | | | | |
| | 749 | startup delay with 100 ns | 0: enable<br>1: disable | | |
| **LFOSC** | | | | | |
| 5D | 750 | LFOSC turn on by register | when matrix output enable/pd control signal=0:<br>0: auto on by delay cells<br>1: always on | | |
| | 751 | matrix power down or on select | 0: matrix down<br>1: matrix on | | |
| 5E | 752 | external clock source enable | 0: internal LFOSC<br>1: external clock from GPIO | | |
| | 753 | matrix out enable | 0: disable<br>1: enable | | |
| | 754 | post divider ratio control | 00: div 1<br>01: div 2<br>10: div 4<br>11: div 8 | | |
| | 755 | | | | |
| | 756 | matrix divider ratio control | 000: /1, 001:/2, 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64 | | |
| | 757 | | | | |
| | 758 | | | | |
| | 759 | enable LFOSC output gating by wake_sleep signal (note: the wake_sleep clock is separated path, so it is not gated) | 0: no gating<br>1: enable | | |
| 5F | 760 | matrix divider ratio control | 000: /1, 001:/2, 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64 | | |
| | 761 | | | | |
| | 762 | | | | |
| | 763 | 2nd output to matrix enable | 0: disable<br>1: enable | | |
| | 764 | matrix divider ratio control | 000: /1, 001:/2, 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64 | | |
| | 765 | | | | |
| | 766 | | | | |
| | 767 | 2nd output to matrix enable | 0: disable<br>1: enable | | |
| 60 | 768 | Reserved | | | |
| | 769 | | | | |
| | 770 | Reserved | | | |
| | 771 | Reserved | | | |
| | 772 | Reserved | | | |
| | 773 | Reserved | | | |
| | 774 | Reserved | | | |
| | 775 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 61 | 776 | Reserved | | | |
| | 777 | Reserved | | | |
| | 778 | IO fast pull up/down enable | 0: disable<br>1: enable | | |
| **GPI0** | | | | | |
| 61 | 779 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 780 | | | | |
| | 781 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 782 | | | | |
| | 783 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **GPIO0** | | | | | |
| 62 | 784 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 785 | | | | |
| | 786 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 787 | | | | |
| | 788 | pull up/down selection | 0: pull down<br>1: pull up | | |
| | 789 | I2C mode selection | 0: I2C fast mode +<br>1: I2C standard/fast mode | | |
| | 790 | open-drain output enable (3.2X drivability) | 0: disable<br>1: enable (3.2X) | | |
| **GPIO1** | | | | | |
| 62 | 791 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| 63 | 792 | | | | |
| | 793 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 794 | | | | |
| | 795 | pull up/down selection | 0: pull down<br>1: pull up | | |
| | 796 | open-drain output enable (3.2X drivability) | 0: disable<br>1: enable (3.2X) | | |
| | 797 | Reserved | | | |
| **GPIO2** | | | | | |
| 63 | 798 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 799 | | | | |
| 64 | 800 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| | 801 | | | | |
| | 802 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 803 | | | | |
| | 804 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **PWR_SW_ON0** | | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 64 | 805 | input mode configuration | 00: digital without schmitt trigger<br>01: Reserved<br>10: Reserved<br>11: Reserved | | |
| | 806 | | | | |
| | 807 | output mode configuration | 00: Reserved<br>01: 2x push-pull<br>10: Reserved<br>11: Reserved | | |
| 65 | 808 | | | | |
| 65 | 809 | pull up/down resistance selection | 00: Reserved<br>01: Reserved<br>10: Reserved<br>11: Reserved | | |
| | 810 | | | | |
| | 811 | pull up/down selection | 0: Reserved<br>1: Reserved | | |
| **PWR_SW_ON1** | | | | | |
| 65 | 812 | Reserved | | | |
| | 813 | | | | |
| | 814 | output mode configuration | 00: Reserved<br>01: 2x push-pull<br>10: Reserved<br>11: Reserved | | |
| | 815 | | | | |
| 66 | 816 | pull up/down resistance selection | 00: Reserved<br>01: Reserved<br>10: Reserved<br>11: Reserved | | |
| | 817 | | | | |
| | 818 | pull up/down selection | 0: Reserved<br>1: Reserved | | |
| | 819 | output enable | 0: Reserved<br>1: Reserved | | |
| | 820 | 4x drive | 0: Reserved<br>1: Reserved | | |
| **GPIO4** | | | | | |
| 66 | 821 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 822 | | | | |
| | 823 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| 67 | 824 | | | | |
| | 825 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 826 | | | | |
| | 827 | pull up/down selection | 0: pull down<br>1: pull up | | |
| | 828 | 4x drive | 0: disable<br>1: enable | | |
| **GPIO5** | | | | | |
| 67 | 829 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 830 | | | | |
| | 831 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| 68 | 832 | | | | |
| | 833 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 834 | | | | |
| | 835 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **GPIO6** | | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 68 | 836 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 837 | | | | |
| | 838 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| | 839 | | | | |
| 69 | 840 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 841 | | | | |
| | 842 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **GPIO7** | | | | | |
| 69 | 843 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 844 | | | | |
| | 845 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| | 846 | | | | |
| | 847 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| 6A | 848 | | | | |
| | 849 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **GPIO8** | | | | | |
| 6A | 850 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 851 | | | | |
| | 852 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| | 853 | | | | |
| | 854 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 855 | | | | |
| 6B | 856 | pull up/down selection | 0: pull down<br>1: pull up | | |
| **GPIO9** | | | | | |
| 6B | 857 | input mode configuration | 00: digital without schmitt trigger<br>01: digital with schmitt trigger<br>10: low voltage digital in<br>11: analog IO | | |
| | 858 | | | | |
| | 859 | output mode configuration | 00: 1x push-pull<br>01: 2x push-pull<br>10: 1x open-drain<br>11: 2x open-drain | | |
| | 860 | | | | |
| | 861 | pull up/down resistance selection | 00: floating<br>01: 10K<br>10: 100K<br>11: 1M | | |
| | 862 | | | | |
| | 863 | pull up/down selection | 0: pull down<br>1: pull up | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 6C | 864 | Reserved | | | |
| | 865 | Reserved | | | |
| | 866 | Reserved | | | |
| | 867 | Reserved | | | |
| | 868 | Reserved | | | |
| | 869 | Reserved | | | |
| | 870 | Reserved | | | |
| | 871 | Reserved | | | |
| 6D | 872 | Reserved | | | |
| | 873 | Reserved | | | |
| | 874 | Reserved | | | |
| | 875 | Reserved | | | |
| | 876 | Reserved | | | |
| | 877 | Reserved | | | |
| | 878 | Reserved | | | |
| | 879 | Reserved | | | |
| 6E | 880 | Reserved | | | |
| | 881 | Reserved | | | |
| | 882 | Reserved | | | |
| | 883 | Reserved | | | |
| | 884 | Reserved | | | |
| | 885 | Reserved | | | |
| | 886 | Reserved | | | |
| | 887 | Reserved | | | |
| 6F | 888 | Reserved | | | |
| | 889 | Reserved | | | |
| | 890 | Reserved | | | |
| | 891 | Reserved | | | |
| | 892 | Reserved | | | |
| | 893 | Reserved | | | |
| | 894 | Reserved | | | |
| | 895 | Reserved | | | |
| 70 | 896 | Reserved | | | |
| | 897 | Reserved | | | |
| | 898 | Reserved | | | |
| | 899 | Reserved | | | |
| | 900 | Reserved | | | |
| | 901 | Reserved | | | |
| | 902 | Reserved | | | |
| | 903 | Reserved | | | |
| 71 | 904 | Reserved | | | |
| | 905 | Reserved | | | |
| | 906 | Reserved | | | |
| | 907 | Reserved | | | |
| | 908 | Reserved | | | |
| | 909 | Reserved | | | |
| | 910 | Reserved | | | |
| | 911 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 72 | 912 | Reserved | | | |
| | 913 | Reserved | | | |
| | 914 | Reserved | | | |
| | 915 | Reserved | | | |
| | 916 | Reserved | | | |
| | 917 | Reserved | | | |
| | 918 | Reserved | | | |
| | 919 | Reserved | | | |
| 73 | 920 | Reserved | | | |
| | 921 | Reserved | | | |
| | 922 | Reserved | | | |
| | 923 | Reserved | | | |
| | 924 | Reserved | | | |
| | 925 | Reserved | | | |
| | 926 | Reserved | | | |
| | 927 | Reserved | | | |
| 74 | 928 | Reserved | | | |
| | 929 | Reserved | | | |
| | 930 | Reserved | | | |
| | 931 | Reserved | | | |
| | 932 | Reserved | | | |
| | 933 | Reserved | | | |
| | 934 | Reserved | | | |
| | 935 | Reserved | | | |
| 75 | 936 | Reserved | | | |
| | 937 | Reserved | | | |
| | 938 | Reserved | | | |
| | 939 | Reserved | | | |
| | 940 | Reserved | | | |
| | 941 | Reserved | | | |
| | 942 | Reserved | | | |
| | 943 | Reserved | | | |
| 76 | 944 | Reserved | | | |
| | 945 | Reserved | | | |
| | 946 | Reserved | | | |
| | 947 | Reserved | | | |
| | 948 | Reserved | | | |
| | 949 | Reserved | | | |
| | 950 | Reserved | | | |
| | 951 | Reserved | | | |
| 77 | 952 | Reserved | | | |
| | 953 | Reserved | | | |
| | 954 | Reserved | | | |
| | 955 | Reserved | | | |
| | 956 | Reserved | | | |
| | 957 | Reserved | | | |
| | 958 | Reserved | | | |
| | 959 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 78 | 960 | Reserved | | | |
| | 961 | Reserved | | | |
| | 962 | Reserved | | | |
| | 963 | Reserved | | | |
| | 964 | Reserved | | | |
| | 965 | Reserved | | | |
| | 966 | Reserved | | | |
| | 967 | Reserved | | | |
| 79 | 968 | Reserved | | | |
| | 969 | Reserved | | | |
| | 970 | Reserved | | | |
| | 971 | Reserved | | | |
| | 972 | Reserved | | | |
| | 973 | Reserved | | | |
| | 974 | Reserved | | | |
| | 975 | Reserved | | | |
| 7A | 976 | Reserved | | | |
| | 977 | Reserved | | | |
| | 978 | Reserved | | | |
| | 979 | Reserved | | | |
| | 980 | Reserved | | | |
| | 981 | Reserved | | | |
| | 982 | Reserved | | | |
| | 983 | Reserved | | | |
| 7B | 984 | Reserved | | | |
| | 985 | Reserved | | | |
| | 986 | Reserved | | | |
| | 987 | Reserved | | | |
| | 988 | Reserved | | | |
| | 989 | Reserved | | | |
| | 990 | Reserved | | | |
| | 991 | Reserved | | | |
| 7C | 992 | Reserved | | | |
| | 993 | Reserved | | | |
| | 994 | Reserved | | | |
| | 995 | Reserved | | | |
| | 996 | Reserved | | | |
| | 997 | Reserved | | | |
| | 998 | Reserved | | | |
| | 999 | Reserved | | | |
| 7D | 1000 | Reserved | | | |
| | 1001 | Reserved | | | |
| | 1002 | Reserved | | | |
| | 1003 | Reserved | | | |
| | 1004 | Reserved | | | |
| | 1005 | Reserved | | | |
| | 1006 | Reserved | | | |
| | 1007 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 7E | 1008 | Reserved | | | |
| | 1009 | Reserved | | | |
| | 1010 | Reserved | | | |
| | 1011 | Reserved | | | |
| | 1012 | Reserved | | | |
| | 1013 | Reserved | | | |
| | 1014 | Reserved | | | |
| | 1015 | Reserved | | | |
| 7F | 1016 | Reserved | | | |
| | 1017 | Reserved | | | |
| | 1018 | Reserved | | | |
| | 1019 | Reserved | | | |
| | 1020 | Reserved | | | |
| | 1021 | Reserved | | | |
| | 1022 | Reserved | | | |
| | 1023 | Reserved | | | |
| 80 | 1030:1024 | Single 4-bit LUT | 0000000: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 0010000: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 0000001: Matrix A - UP (CNT); Matrix B - KEEP (CNT); Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (CNT)<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 0000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - In1; Matrix D - In0<br>(DLY_OUT connected to In3) | | |
| | | CNT/DLY→ DFF | 0010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 0100010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0<br>(DLY_OUT connected to In3; In2 - LOW) | | |
| | | CNT/DLY→ DFF | 0110010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK<br>(DLY_OUT connected to D; nSET - HIGH) | | |
| | | CNT/DLY→ LUT | 1000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - EXT_CLK (CNT);<br>Matrix D - In0<br>(DLY_OUT connected to In3; In1 - LOW) | | |
| | | CNT/DLY→ DFF | 1010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - EXT_CLK (CNT);<br>Matrix D - CLK<br>(DLY_OUT connected to D; nRST - HIGH) | | |
| | | CNT/DLY→ LUT | 0000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - In1; Matrix D - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 0010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - nRST; Matrix D - CLK<br>(DLY_OUT connected to nSET) | | |
| | | CNT/DLY→ LUT | 1000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT);<br>Matrix D - In0<br>(DLY_OUT connected to In2; In1 - LOW) | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 80 | 1030:1024 | CNT/DLY→ DFF | 1010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT);<br>Matrix D - CLK<br>(DLY_OUT connected to nSET; nRST - HIGH) | | |
| | | CNT/DLY→ LUT | 0001010: Matrix A - In3; Matrix B - In2; Matrix C - DLY_IN; Matrix D - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 0011010: Matrix A - D; Matrix B - nSET; Matrix C - DLY_IN; Matrix D - CLK<br>(DLY_OUT connected to nRST) | | |
| | | CNT/DLY→ LUT | 0101010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN;<br>Matrix D - In0<br>(DLY_OUT connected to In1; In2 - LOW) | | |
| | | CNT/DLY→ DFF | 0111010: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - CLK<br>(DLY_OUT connected to nRST; nSET - HIGH) | | |
| | | CNT/DLY→ LUT | 0001110: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 0011110: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | CNT/DLY→ LUT | 0101110: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1;<br>Matrix D - DLY_IN<br>(DLY_OUT connected to In0; In2 - LOW) | | |
| | | CNT/DLY→ DFF | 0111110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - DLY_IN<br>(DLY_OUT connected to CLK; nSET - HIGH) | | |
| | | CNT/DLY→ LUT | 1001110: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT);<br>Matrix D - DLY_IN<br>(DLY_OUT connected to In0; In1 - LOW) | | |
| | | CNT/DLY→ DFF | 1011110: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN<br>(DLY_OUT connected to CLK; nRST - HIGH) | | |
| | | LUT→ CNT/DLY | 0000011: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 0010011: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| | | LUT→ CNT/DLY | 0100011: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0<br>(LUT_OUT connected to DLY_IN; In2 - LOW) | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 80 | 1030:1024 | DFF→ CNT/DLY | 0110011: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN; nSET - HIGH) | | |
| | | LUT→ CNT/DLY | 1000011: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (LUT_OUT connected to DLY_IN; In1 - LOW) | | |
| | | DFF→ CNT/DLY | 1010011: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DFF_OUT connected to DLY_IN; nRST - HIGH) | | |
| | 1031 | DLY/CNT0 Mode Selection | 00: DLY<br>01: one shot<br>10: frequency det<br>11: CNT register [1040]=0 | | |
| 81 | 1032 | | | | |
| | 1033 | DLY/CNT0 edge Mode Selection | 00: both edge<br>01: falling edge<br>10: rising edge<br>11: High Level Reset (only in CNT mode) | | |
| | 1034 | | | | |
| | 1035 | DLY/CNT0 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011: 2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110: 2K(LF OSC); 0111: 2K/8;<br>1000: 2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011: 2K/32768;<br>1100: 2 K/262144; 1101: CNT4_END;<br>1110: External; 1111: No-used | | |
| | 1036 | | | | |
| | 1037 | | | | |
| | 1038 | | | | |
| | 1039 | FSM0 SET/RST Selection | 0: Reset to 0<br>1: Set to data | | |
| 82 | 1040 | CNT0 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection (registers [1032:1031]=00) | | |
| | 1041 | UP signal sync selection | 0: bypass<br>1: after two DFF | | |
| | 1042 | Keep signal sync selection | 0: bypass<br>1: after two DFF | | |
| | 1043 | CNT0 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1044 | | | | |
| | 1045 | Wake sleep power down state selection | 0: low<br>1: high | | |
| | 1046 | wake sleep mode selection | 0: Default Mode<br>1: Wake Sleep Mode<br>(registers [1032:1031]=11) | | |
| | 1047 | CNT0 output pol selection | 0: Default Output<br>1: Inverted Output | | |
| 83 | 1048 | CNT0 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |
| | 1053:1049 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 83 | 1053:1049 | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| | 1054 | CNT1 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1055 | | | | |
| 84 | 1056 | | | | |
| | 1057 | | | | |
| | 1058 | CNT1 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1059 | | | | |
| | 1060 | DLY/CNT1 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1061 | | | | |
| | 1062 | | | | |
| | 1063 | | | | |
| 85 | 1064 | CNT1 output pol selection | 0: Default Output<br>1: Inverted Output | | |
| 85 | 1065 | CNT1 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |
| | 1066 | CNT1 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection<br>(registers [1057:1054]=0000/0001/0010) | | |
| | 1071:1067 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1;<br>Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 85 | 1071:1067 | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| 86 | 1072 | CNT2 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1073 | | | | |
| | 1074 | CNT2 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1075 | | | | |
| | 1076 | | | | |
| | 1077 | | | | |
| | 1078 | DLY/CNT2 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1079 | | | | |
| 87 | 1080 | | | | |
| | 1081 | | | | |
| | 1082 | CNT2 output pol selection | 0: Default Output, 1: Inverted Output | | |
| | 1083 | CNT2 CNT mode SYNC selection | 0: bypass; 1: after two DFF | | |
| | 1084 | CNT2 DLY EDET FUNCTION Selection | 0: normal; 1: DLY function edge detection (registers [1077:1074]=0000/0001/0010) | | |
| | 1085 | CNT3 initial value selection | 00:bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1 | | |
| | 1086 | | | | |
| | 1087 | Multi3 register configure | refer to byte 88 | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 88 | 1088 | CNT3 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1089 | | | | |
| | 1090 | | | | |
| | 1091 | | | | |
| 88 | 1087, 1093:1092, 1095:1094 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1;<br>Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| 89 | 1096 | DLY/CNT3 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1097 | | | | |
| | 1098 | | | | |
| | 1099 | | | | |
| | 1100 | CNT3 output pol selection | 0: Default Output<br>1: Inverted Output | | |
| | 1101 | CNT3 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |
| | 1102 | CNT3 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection<br>(registers [1091:1088]=0000/0001/0010) | | |
| | 1103 | CNT4 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 8A | 1104 | CNT4 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1105 | | | | |
| | 1106 | CNT4 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection<br>(registers [1119:1116]=0000/0001/0010) | | |
| | 1111:1107 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1;<br>Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DLY_IN - LOW) | | |
| 8A | 1107,<br>1111:1108 | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST;<br>Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| 8B | 1112 | DLY/CNT4 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1113 | | | | |
| | 1114 | | | | |
| | 1115 | | | | |
| | 1116 | CNT4 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1117 | | | | |
| | 1118 | | | | |
| | 1119 | | | | |
| 8C | 1120 | CNT4 output pol selection | 0: Default Output<br>1: Inverted Output | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 8C | 1121 | CNT5 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1122 | | | | |
| | 1123 | | | | |
| | 1124 | | | | |
| | 1125 | CNT5 output pol selection | 0: Default Output<br>1: Inverted Output | | |
| | 1134, 1127:1126, 1133:1132 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| 8D | 1128 | DLY/CNT5 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1129 | | | | |
| | 1130 | | | | |
| | 1131 | | | | |
| | 1135 | CNT5 DLY EDET FUNCTION Selection | 0: normal;<br>1: DLY function edge detection<br>(registers [1124:1121]=0000/0001/0010) | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 8E | 1136 | CNT5 CNT mode SYNC selection | 0: bypass;<br>1: after two DFF | | |
| | 1137 | CNT5 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1138 | | | | |
| | 1139 | CNT6 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1140 | | | | |
| | 1141 | | | | |
| | 1142 | | | | |
| | 1143 | CNT6 output pol selection | 0: Default Output<br>1: Inverted Output | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 8F | 1144 | DLY/CNT6 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1145 | | | | |
| | 1146 | | | | |
| | 1147 | | | | |
| | 1152, 1149:1148, 1151:1150. | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| 90 | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| | 1153 | CNT6 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection<br>(registers [1142:1139]=0000/0001/0010) | | |
| | 1154 | CNT6 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |
| | 1155 | CNT6 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1156 | | | | |
| | 1157 | CNT7 initial value selection | 00: bypass the initial<br>01: initial 0<br>10: initial 1<br>11: initial 1 | | |
| | 1158 | | | | |
| | 1159 | CNT7 CNT mode SYNC selection | 0: bypass<br>1: after two DFF | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 91 | 1160 | CNT7 DLY EDET FUNCTION Selection | 0: normal<br>1: DLY function edge detection<br>(registers [1174:1171]=0000/0001/0010) | | |
| | 1161, 1165:1162 | Single 3-bit LUT | 00000: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(DLY_IN - LOW) | | |
| | | Single DFF w RST and SET | 10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_IN - LOW) | | |
| | | Single CNT/DLY | 00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC<br>(DLY_OUT connected to LUT/DFF) | | |
| | | CNT/DLY→ LUT | 00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0<br>(DLY_OUT connected to In2) | | |
| | | CNT/DLY→ DFF | 10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK<br>(DLY_OUT connected to D) | | |
| | | CNT/DLY→ LUT | 00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0<br>(DLY_OUT connected to In1) | | |
| | | CNT/DLY→ DFF | 10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK<br>(DLY_OUT connected to nSET/nRST) | | |
| | | CNT/DLY→ LUT | 01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN<br>(DLY_OUT connected to In0) | | |
| | | CNT/DLY→ DFF | 11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN<br>(DLY_OUT connected to CLK) | | |
| | | LUT→ CNT/DLY | 00011: Matrix A - In2; Matrix B - In1; Matrix C - In0<br>(LUT_OUT connected to DLY_IN) | | |
| | | DFF→ CNT/DLY | 10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK<br>(DFF_OUT connected to DLY_IN) | | |
| 91 | 1166 | DLY/CNT7 Clock Source Select | Clock source sel[3:0]<br>0000: 25M(Ring OSC); 0001: 25M/4;<br>0010: 2M(RC OSC); 0011:2M/8;<br>0100: 2M/64; 0101: 2M/512;<br>0110:2K(LF OSC); 0111: 2K/8;<br>1000:2K/64; 1001: 2K/512;<br>1010: 2K/4096; 1011:2K/32768;<br>1100: 2K/262144; 1101: CNT0_END;<br>1110: External; 1111: No-used | | |
| | 1167 | | | | |
| 92 | 1168 | | | | |
| | 1169 | | | | |
| | 1170 | CNT7 output pol selection | 0: Default Output<br>1: Inverted Output | | |
| | 1171 | CNT7 function and edge mode selection | 0000: both edge Delay;<br>0001: falling edge delay;<br>0010: rising edge delay:<br>0011: both edge One Shot;<br>0100: falling edge One Shot;<br>0101: rising edge One Shot;<br>0110: both edge freq detect;<br>0111: falling edge freq detect;<br>1000: rising edge freq detect;<br>1001: both edge detect;<br>1010: falling edge detect;<br>1011: rising edge detect;<br>1100: both edge reset CNT;<br>1101: falling edge reset CNT;<br>1110: rising edge reset CNT;<br>1111: high level reset CNT | | |
| | 1172 | | | | |
| | 1173 | | | | |
| | 1174 | | | | |
| | 1175 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 93 | 1176 | Multi0_LUT4_DFF setting | [15]:LUT4_1 [15]/DFF20 or Latch Select<br>0: DFF function, 1: Latch function<br>[14]:LUT4_1 [14]/DFF20 Output Select<br>0: Q output, 1: QB output<br>[13]:LUT4_1 [13] /DFF20 Initial Polarity Select<br>0: Low, 1: High<br>[12:0]:LUT4_1 [12:0] | | |
| | 1177 | | | | |
| | 1178 | | | | |
| | 1179 | | | | |
| | 1180 | | | | |
| | 1181 | | | | |
| | 1182 | | | | |
| | 1183 | | | | |
| 94 | 1184 | | | | |
| | 1185 | | | | |
| | 1186 | | | | |
| | 1187 | | | | |
| | 1188 | | | | |
| | 1189 | | | | |
| | 1190 | | | | |
| | 1191 | | | | |
| 95 | 1192 | REG_CNT0_D[15:0] | Data[15:0] | | |
| | 1193 | | | | |
| | 1194 | | | | |
| | 1195 | | | | |
| | 1196 | | | | |
| | 1197 | | | | |
| | 1198 | | | | |
| | 1199 | | | | |
| 96 | 1200 | | | | |
| | 1201 | | | | |
| | 1202 | | | | |
| | 1203 | | | | |
| | 1204 | | | | |
| | 1205 | | | | |
| | 1206 | | | | |
| | 1207 | | | | |
| 97 | 1208 | Multi1_LUT3_DFF setting | [7]:LUT3_9 [7]/DFF13 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_9 [6]/DFF13 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_9 [5] /DFF13<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_9 [4]/DFF13 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_9 [3:0] | | |
| | 1209 | | | | |
| | 1210 | | | | |
| | 1211 | | | | |
| | 1212 | | | | |
| | 1213 | | | | |
| | 1214 | | | | |
| | 1215 | | | | |
| 98 | 1216 | REG_CNT1_D[7:0] | Data[7:0] | | |
| | 1217 | | | | |
| | 1218 | | | | |
| | 1219 | | | | |
| | 1220 | | | | |
| | 1221 | | | | |
| | 1222 | | | | |
| | 1223 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 99 | 1224 | Multi2_LUT3_DFF setting | [7]:LUT3_10 [7]/DFF14 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_10[6]/DFF14 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_10 [5] /DFF14<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_10 [4]/DFF14 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_10 [3:0] | | |
| | 1225 | | | | |
| | 1226 | | | | |
| | 1227 | | | | |
| | 1228 | | | | |
| | 1229 | | | | |
| | 1230 | | | | |
| | 1231 | | | | |
| 9A | 1232 | REG_CNT2_D[7:0] | Data[7:0] | | |
| | 1233 | | | | |
| | 1234 | | | | |
| | 1235 | | | | |
| | 1236 | | | | |
| | 1237 | | | | |
| | 1238 | | | | |
| | 1239 | | | | |
| 9B | 1240 | Multi3_LUT3_DFF setting | [7]:LUT3_11 [7]/DFF15 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_11[6]/DFF15 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_11 [5] /DFF15<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_11 [4]/DFF15 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_11 [3:0] | | |
| | 1241 | | | | |
| | 1242 | | | | |
| | 1243 | | | | |
| | 1244 | | | | |
| | 1245 | | | | |
| | 1246 | | | | |
| | 1247 | | | | |
| 9C | 1248 | REG_CNT3_D[7:0] | Data[7:0] | | |
| | 1249 | | | | |
| | 1250 | | | | |
| | 1251 | | | | |
| | 1252 | | | | |
| | 1253 | | | | |
| | 1254 | | | | |
| | 1255 | | | | |
| 9D | 1256 | Multi4_LUT3_DFF setting | [7]:LUT3_12 [7]/DFF16 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_12[6]/DFF16 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_12 [5] /DFF16<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_12 [4]/DFF16 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_12 [3:0] | | |
| | 1257 | | | | |
| | 1258 | | | | |
| | 1259 | | | | |
| | 1260 | | | | |
| | 1261 | | | | |
| | 1262 | | | | |
| | 1263 | | | | |
| 9E | 1264 | REG_CNT4_D[7:0] | Data[7:0] | | |
| | 1265 | | | | |
| | 1266 | | | | |
| | 1267 | | | | |
| | 1268 | | | | |
| | 1269 | | | | |
| | 1270 | | | | |
| | 1271 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| 9F | 1272 | Multi5_LUT3_DFF setting | [7]:LUT3_13 [7]/DFF17 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_13[6]/DFF17 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_13 [5] /DFF17<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_13 [4]/DFF17 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_13 [3:0] | | |
| | 1273 | | | | |
| | 1274 | | | | |
| | 1275 | | | | |
| | 1276 | | | | |
| | 1277 | | | | |
| | 1278 | | | | |
| | 1279 | | | | |
| A0 | 1280 | REG_CNT5_D[7:0] | Data[7:0] | | |
| | 1281 | | | | |
| | 1282 | | | | |
| | 1283 | | | | |
| | 1284 | | | | |
| | 1285 | | | | |
| | 1286 | | | | |
| | 1287 | | | | |
| A1 | 1288 | Multi6_LUT3_DFF setting | [7]:LUT3_14 [7]/DFF18 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_14[6]/DFF18 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_14 [5] /DFF18<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_14 [4]/DFF18 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_14 [3:0] | | |
| | 1289 | | | | |
| | 1290 | | | | |
| | 1291 | | | | |
| | 1292 | | | | |
| | 1293 | | | | |
| | 1294 | | | | |
| | 1295 | | | | |
| A2 | 1296 | REG_CNT6_D[7:0] | Data[7:0] | | |
| | 1297 | | | | |
| | 1298 | | | | |
| | 1299 | | | | |
| | 1300 | | | | |
| | 1301 | | | | |
| | 1302 | | | | |
| | 1303 | | | | |
| A3 | 1304 | Multi7_LUT3_DFF setting | [7]:LUT3_15 [7]/DFF19 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_15[6]/DFF19 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_15 [5] /DFF19<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[4]:LUT3_15 [4]/DFF19 Initial Polarity Select<br>0: Low, 1: High<br>[3:0]:LUT3_15 [3:0] | | |
| | 1305 | | | | |
| | 1306 | | | | |
| | 1307 | | | | |
| | 1308 | | | | |
| | 1309 | | | | |
| | 1310 | | | | |
| | 1311 | | | | |
| A4 | 1312 | REG_CNT7_D[7:0] | Data[7:0] | | |
| | 1313 | | | | |
| | 1314 | | | | |
| | 1315 | | | | |
| | 1316 | | | | |
| | 1317 | | | | |
| | 1318 | | | | |
| | 1319 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| A5 | 1320 | CNT0 (16bits) Counted Value | Virtual Input | | |
| | 1321 | | | | |
| | 1322 | | | | |
| | 1323 | | | | |
| | 1324 | | | | |
| | 1325 | | | | |
| | 1326 | | | | |
| | 1327 | | | | |
| A6 | 1328 | | | | |
| | 1329 | | | | |
| | 1330 | | | | |
| | 1331 | | | | |
| | 1332 | | | | |
| | 1333 | | | | |
| | 1334 | | | | |
| | 1335 | | | | |
| A7 | 1336 | CNT6 (8bits) Counted Value | Virtual Input | | |
| | 1337 | | | | |
| | 1338 | | | | |
| | 1339 | | | | |
| | 1340 | | | | |
| | 1341 | | | | |
| | 1342 | | | | |
| | 1343 | | | | |
| A8 | 1344 | CNT7 (8bits) Counted Value | Virtual Input | | |
| | 1345 | | | | |
| | 1346 | | | | |
| | 1347 | | | | |
| | 1348 | | | | |
| | 1349 | | | | |
| | 1350 | | | | |
| | 1351 | | | | |
| A9 | 1352 | LUT3_1_DFF4 setting | [7]:LUT3_1 [7]/DFF4 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_1 [6]/DFF4 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_1 [5] /DFF4 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_1 [4]/DFF4<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_1 [3]/DFF4 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_1 [2:0] | | |
| | 1353 | | | | |
| | 1354 | | | | |
| | 1355 | | | | |
| | 1356 | | | | |
| | 1357 | | | | |
| | 1358 | | | | |
| | 1359 | | | | |
| AA | 1360 | LUT3_2_DFF5 setting | [7]:LUT3_2 [7]/DFF5 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_2 [6]/DFF5 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_2 [5] /DFF5 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_2 [4]/DFF5<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_2 [3]/DFF5 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_2 [2:0] | | |
| | 1361 | | | | |
| | 1362 | | | | |
| | 1363 | | | | |
| | 1364 | | | | |
| | 1365 | | | | |
| | 1366 | | | | |
| | 1367 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| AB | 1368 | LUT3_3_DFF6 setting | [7]:LUT3_3 [7]/DFF6 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_3 [6]/DFF6 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_3 [5] /DFF6 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_3 [4]/DFF6<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_3 [3]/DFF6 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_3 [2:0] | | |
| | 1369 | | | | |
| | 1370 | | | | |
| | 1371 | | | | |
| | 1372 | | | | |
| | 1373 | | | | |
| | 1374 | | | | |
| | 1375 | | | | |
| AC | 1376 | LUT3_4_DFF7 setting | [7]:LUT3_4 [7]/DFF7 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_4 [6]/DFF7 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_4 [5] /DFF7 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_4 [4]/DFF7<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_4 [3]/DFF7 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_4 [2:0] | | |
| | 1377 | | | | |
| | 1378 | | | | |
| | 1379 | | | | |
| | 1380 | | | | |
| | 1381 | | | | |
| | 1382 | | | | |
| | 1383 | | | | |
| AD | 1384 | LUT2_3_VAL or PGEN_data | LUT2_3[3:0] or PGEN 4bit counter data[3:0] | | |
| | 1385 | | | | |
| | 1386 | | | | |
| | 1387 | | | | |
| | 1388 | LUT3_1 or DFF4 Select | 0: LUT3_1<br>1: DFF4 | | |
| | 1389 | LUT3_2 or DFF5 Select | 0: LUT3_2<br>1: DFF5 | | |
| | 1390 | LUT3_3 or DFF6 Select | 0: LUT3_3<br>1: DFF6 | | |
| | 1391 | LUT3_4 or DFF7 Select | 0: LUT3_4<br>1: DFF7 | | |
| AE | 1392 | PGEN data | PGEN Data[15:0] | | |
| | 1393 | | | | |
| | 1394 | | | | |
| | 1395 | | | | |
| | 1396 | | | | |
| | 1397 | | | | |
| | 1398 | | | | |
| | 1399 | | | | |
| AF | 1400 | | | | |
| | 1401 | | | | |
| | 1402 | | | | |
| | 1403 | | | | |
| | 1404 | | | | |
| | 1405 | | | | |
| | 1406 | | | | |
| | 1407 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| B0 | 1408 | LUT2_3 or PGEN Select | 0: LUT2_3<br>1: PGEN | | |
| | 1409 | Active level selection for RST/SET for LUT2_3 or PGEN | 0: Active low level reset/set<br>1: Active high level reset/set | | |
| | 1410 | Active level selection for RST/SET for LUT3_16 or Pipe Delay/RIPP CNT | 0: Active low level reset/set<br>1: Active high level reset/set | | |
| | 1411 | Out of LUT3_16 or Out0 of Pipe Delay/RIPP CNT Select | 0: LUT3_16<br>1: OUT0 of Pipe Delay or RIPP CNT | | |
| | 1412 | PIPE_RIPP_CNT_S | 0: Pipe delay mode selection<br>1: Ripple Counter mode selection | | |
| | 1413 | Pipe Delay OUT1 Polarity Select | 0: Non-inverted<br>1: Inverted | | |
| | 1414 | LUT4_0 or DFF12 Select | 0: LUT4_0<br>1: DFF12 | | |
| | 1415 | LUT3_0 or DFF3 Select | 0: LUT3_0<br>1: DFF3 | | |
| B1 | 1416 | LUT value or pipe delay out sel or nSET/END value | [7:4]: LUT3_8 [7:4]/REG_S1[3:0] pipe delay out1 sel<br>[3:0]: LUT3_8 [3:0]/REG_S0[3:0] pipe delay out0 sel<br>at RIPP CNT mode:<br>bit[1418:1416] is the nSET value<br>bit[1421:1419] is the END value<br>bit[1422] is the range control: 0 full cycle, 1 range cycle<br>bit[1423] Not used | | |
| | 1417 | | | | |
| | 1418 | | | | |
| | 1419 | | | | |
| | 1420 | | | | |
| | 1421 | | | | |
| | 1422 | | | | |
| | 1423 | | | | |
| B2 | 1424 | LUT4_0_DFF12 setting | [15]:LUT4_0 [15]/DFF12 or Latch Select<br>0: DFF function, 1: Latch function<br>[14]:LUT4_0 [14]/DFF12 Output Select<br>0: Q output, 1: QB output<br>[13]:LUT4_0 [13] /DFF12 Initial Polarity Select<br>0: Low, 1: High<br>[12]:LUT4_0 [12] /DFF12 stage selection<br>0: Q of first DFF; 1 Q of second DFF<br>[11]:LUT4_0 [11]/DFF12<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[10]:LUT4_0 [10]/DFF12 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[9:0]: LUT4_0 [9:0] | | |
| | 1425 | | | | |
| | 1426 | | | | |
| | 1427 | | | | |
| | 1428 | | | | |
| | 1429 | | | | |
| | 1430 | | | | |
| | 1431 | | | | |
| B3 | 1432 | | | | |
| | 1433 | | | | |
| | 1434 | | | | |
| | 1435 | | | | |
| | 1436 | | | | |
| | 1437 | | | | |
| | 1438 | | | | |
| | 1439 | | | | |
| B4 | 1440 | LUT3_0_DFF3 setting | [7]:LUT3_0 [7]/DFF3 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_0 [6]/DFF3 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_0 [5] /DFF3 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_0 [3]/DFF3stage selection<br>0: Q of first DFF; 1 Q of second DFF<br>[3]:LUT3_0 [4]/DFF3<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[2]:LUT3_0 [2]/DFF3 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[1:0]: LUT3_0 [1:0] | | |
| | 1441 | | | | |
| | 1442 | | | | |
| | 1443 | | | | |
| | 1444 | | | | |
| | 1445 | | | | |
| | 1446 | | | | |
| | 1447 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| B5 | 1448 | Filter or Edge Detector selection | 0, filter<br>1, edge det | | |
| | 1449 | Output Polarity Select | 0: output non-invert<br>1: output invert | | |
| | 1450 | Select the edge mode | 00: Rising Edge Det<br>01: Falling Edge Det<br>10: Both Edge Det<br>11: Both Edge DLY | | |
| | 1451 | | | | |
| | 1452 | Delay Value Select for Programmable Delay & Edge Detector | 00: 125 ns<br>01: 250 ns<br>10: 375 ns<br>11: 500 ns | | |
| | 1453 | | | | |
| | 1454 | Select the Edge Mode of Programmable Delay & Edge Detector | 00: Rising Edge Detector<br>01: Falling Edge Detector<br>10: Both Edge Detector<br>11: Both Edge Delay | | |
| | 1455 | | | | |
| B6 | 1456 | LUT3_5_DFF8 setting | [7]:LUT3_5 [7]/DFF8 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_5 [6]/DFF8 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_5 [5] /DFF8 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_5 [4]/DFF8<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_5 [3]/DFF8 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_5 [2:0] | | |
| | 1457 | | | | |
| | 1458 | | | | |
| | 1459 | | | | |
| | 1460 | | | | |
| | 1461 | | | | |
| | 1462 | | | | |
| | 1463 | | | | |
| B7 | 1464 | LUT3_6_DFF9 setting | [7]:LUT3_6 [7]/DFF9 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_6 [6]/DFF9 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_6 [5] /DFF9 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_6 [4]/DFF9<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_6 [3]/DFF9 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_6 [2:0] | | |
| | 1465 | | | | |
| | 1466 | | | | |
| | 1467 | | | | |
| | 1468 | | | | |
| | 1469 | | | | |
| | 1470 | | | | |
| | 1471 | | | | |
| B8 | 1472 | LUT3_7_DFF10 setting | [7]:LUT3_7 [7]/DFF10 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_7 [6]/DFF10 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_7 [5] /DFF10 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_7 [4]/DFF10<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_7 [3]/DFF10 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_7 [2:0] | | |
| | 1473 | | | | |
| | 1474 | | | | |
| | 1475 | | | | |
| | 1476 | | | | |
| | 1477 | | | | |
| | 1478 | | | | |
| | 1479 | | | | |
| B9 | 1480 | LUT3_8_DFF11 setting | [7]:LUT3_8 [7]/DFF11 or Latch Select<br>0: DFF function, 1: Latch function<br>[6]:LUT3_8 [6]/DFF11 Output Select<br>0: Q output, 1: QB output<br>[5]:LUT3_8 [5] /DFF11 Initial Polarity Select<br>0: Low, 1: High<br>[4]:LUT3_8 [4]/DFF11<br>0: nRST from Matrix Output, 1: nSET from Matrix Output<br>[3]:LUT3_8 [3]/DFF11 Active level selection for RST/SET<br>0: Active low level reset/set, 1: Active high level reset/set<br>[2:0]: LUT3_8 [2:0] | | |
| | 1481 | | | | |
| | 1482 | | | | |
| | 1483 | | | | |
| | 1484 | | | | |
| | 1485 | | | | |
| | 1486 | | | | |
| | 1487 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| BA | 1488 | LUT2_0 or DFF0 Select | 0: LUT2_0<br>1: DFF0 | | |
| | 1489 | LUT2_1 or DFF1 Select | 0: LUT2_1<br>1: DFF1 | | |
| | 1490 | LUT2_2 or DFF2 Select | 0: LUT2_2<br>1: DFF2 | | |
| | 1491 | Reserved | | | |
| | 1492 | LUT3_5 or DFF8 Select | 0: LUT3_5<br>1: DFF8 | | |
| | 1493 | LUT3_6 or DFF9 Select | 0: LUT3_6<br>1: DFF9 | | |
| | 1494 | LUT3_7 or DFF10 Select | 0: LUT3_7<br>1: DFF10 | | |
| | 1495 | LUT3_8 or DFF11 Select | 0: LUT3_8<br>1: DFF11 | | |
| BB | 1496 | LUT2_0/DFF0 setting | [3]:LUT2_0 [3]/DFF0 or Latch Select<br>0: DFF function, 1: Latch function<br>[2]:LUT2_0 [2]/DFF0 Output Select<br>0: Q output, 1: QB output<br>[1]:LUT2_0 [1]/DFF0 Initial Polarity Select<br>0: Low, 1: High<br>[0]:LUT2_0 [0] | | |
| | 1497 | | | | |
| | 1498 | | | | |
| | 1499 | | | | |
| | 1500 | LUT2_1/DFF1 setting | [3]:LUT2_1 [3]/DFF1 or Latch Select<br>0: DFF function, 1: Latch function<br>[2]:LUT2_1 [2]/DFF1 Output Select<br>0: Q output, 1: QB output<br>[1]:LUT2_1 [1]/DFF1 Initial Polarity Select<br>0: Low, 1: High<br>[0]:LUT2_1 [0] | | |
| | 1501 | | | | |
| | 1502 | | | | |
| | 1503 | | | | |
| BC | 1504 | LUT2_2/DFF2 setting | [3]:LUT2_2 [3]/DFF2 or Latch Select<br>0: DFF function, 1: Latch function<br>[2]:LUT2_2 [2]/DFF2 Output Select<br>0: Q output, 1: QB output<br>[1]:LUT2_2 [1]/DFF2 Initial Polarity Select<br>0: Low, 1: High<br>[0]:LUT2_2 [0] | | |
| | 1505 | | | | |
| | 1506 | | | | |
| | 1507 | | | | |
| | 1508 | Reserved | | | |
| | 1509 | | | | |
| | 1510 | | | | |
| | 1511 | | | | |
| BD | 1512 | | | | |
| | 1513 | | | | |
| | 1514 | | | | |
| | 1515 | | | | |
| | 1516 | | | | |
| | 1517 | | | | |
| | 1518 | | | | |
| | 1519 | | | | |
| BE | 1520 | DFT enable | 0: DFT disable<br>1: DFT enable | | |
| | 1521 | Signal of DFT selection (AOUT[48]) | Select DFT test matrix or test DFT itself function<br>0: bypass mode (normal DFT test);<br>1: tied high or low (test DFT itself function) | | |
| | 1522 | Signal of DFT tied low or high | Set input signal high or low to test DFT itself function<br>0: tied low<br>1: tied high | | |
| | 1523 | Reserved | | | |
| | 1524 | Reserved | | | |
| | 1525 | | | | |
| | 1526 | | | | |
| | 1527 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| BF | 1528 | Reserved | | | |
| | 1529 | Reserved | | | |
| | 1530 | Reserved | | | |
| | 1531 | Reserved | | | |
| | 1532 | Reserved | | | |
| | 1533 | Reserved | | | |
| | 1534 | Reserved | | | |
| | 1535 | Reserved | | | |
| C0 | 1536 | Reserved | | | |
| | 1537 | Reserved | | | |
| | 1538 | Reserved | | | |
| | 1539 | Reserved | | | |
| | 1540 | Reserved | | | |
| | 1541 | Reserved | | | |
| | 1542 | Reserved | | | |
| | 1543 | Reserved | | | |
| C1 | 1544 | Reserved | | | |
| | 1545 | Reserved | | | |
| | 1546 | Reserved | | | |
| | 1547 | Reserved | | | |
| | 1548 | Reserved | | | |
| | 1549 | Reserved | | | |
| | 1550 | Reserved | | | |
| | 1551 | Reserved | | | |
| C2 | 1552 | Reserved | | | |
| | 1553 | Reserved | | | |
| | 1554 | Reserved | | | |
| | 1555 | Reserved | | | |
| | 1556 | Reserved | | | |
| | 1557 | Reserved | | | |
| | 1558 | Reserved | | | |
| | 1559 | Reserved | | | |
| C3 | 1560 | Reserved | | | |
| | 1561 | Reserved | | | |
| | 1562 | Reserved | | | |
| | 1563 | Reserved | | | |
| | 1564 | Reserved | | | |
| | 1565 | Reserved | | | |
| | 1566 | Reserved | | | |
| | 1567 | Reserved | | | |
| C4 | 1568 | Reserved | | | |
| | 1569 | Reserved | | | |
| | 1570 | Reserved | | | |
| | 1571 | Reserved | | | |
| | 1572 | Reserved | | | |
| | 1573 | Reserved | | | |
| | 1574 | Reserved | | | |
| | 1575 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| C5 | 1576 | Reserved | | | |
| | 1577 | Reserved | | | |
| | 1578 | Reserved | | | |
| | 1579 | Reserved | | | |
| | 1580 | Reserved | | | |
| | 1581 | Reserved | | | |
| | 1582 | Reserved | | | |
| | 1583 | Reserved | | | |
| C6 | 1584 | Reserved | | | |
| | 1585 | Reserved | | | |
| | 1586 | Reserved | | | |
| | 1587 | Reserved | | | |
| | 1588 | Reserved | | | |
| | 1589 | Reserved | | | |
| | 1590 | Reserved | | | |
| | 1591 | Reserved | | | |
| C7 | 1592 | Reserved | | | |
| | 1593 | Reserved | | | |
| | 1594 | Reserved | | | |
| | 1595 | Reserved | | | |
| | 1596 | Reserved | | | |
| | 1597 | Reserved | | | |
| | 1598 | Reserved | | | |
| | 1599 | Reserved | | | |
| C8 | 1600 | Reserved | | | |
| | 1601 | Reserved | | | |
| | 1602 | Reserved | | | |
| | 1603 | Reserved | | | |
| | 1604 | Reserved | | | |
| | 1605 | Reserved | | | |
| | 1606 | Reserved | | | |
| | 1607 | Reserved | | | |
| C9 | 1608 | Reserved | | | |
| | 1609 | Reserved | | | |
| | 1610 | Reserved | | | |
| | 1611 | Reserved | | | |
| | 1612 | Reserved | | | |
| | 1613 | Reserved | | | |
| | 1614 | Reserved | | | |
| | 1615 | Reserved | | | |
| CA | 1616 | Reserved | | | |
| | 1617 | Reserved | | | |
| | 1618 | Reserved | | | |
| | 1619 | Reserved | | | |
| | 1620 | Reserved | | | |
| | 1621 | Reserved | | | |
| | 1622 | Reserved | | | |
| | 1623 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| CB | 1624 | Reserved | | | |
| | 1625 | Reserved | | | |
| | 1626 | Reserved | | | |
| | 1627 | Reserved | | | |
| | 1628 | Reserved | | | |
| | 1629 | Reserved | | | |
| | 1630 | Reserved | | | |
| | 1631 | Reserved | | | |
| CC | 1632 | Reserved | | | |
| | 1633 | Reserved | | | |
| | 1634 | Reserved | | | |
| | 1635 | Reserved | | | |
| | 1636 | Reserved | | | |
| | 1637 | Reserved | | | |
| | 1638 | Reserved | | | |
| | 1639 | Reserved | | | |
| CD | 1640 | Reserved | | | |
| | 1641 | Reserved | | | |
| | 1642 | Reserved | | | |
| | 1643 | Reserved | | | |
| | 1644 | Reserved | | | |
| | 1645 | Reserved | | | |
| | 1646 | Reserved | | | |
| | 1647 | Reserved | | | |
| CE | 1648 | Reserved | | | |
| | 1649 | Reserved | | | |
| | 1650 | Reserved | | | |
| | 1651 | Reserved | | | |
| | 1652 | Reserved | | | |
| | 1653 | Reserved | | | |
| | 1654 | Reserved | | | |
| | 1655 | Reserved | | | |
| CF | 1656 | Reserved | | | |
| | 1657 | Reserved | | | |
| | 1658 | Reserved | | | |
| | 1659 | Reserved | | | |
| | 1660 | Reserved | | | |
| | 1661 | Reserved | | | |
| | 1662 | Reserved | | | |
| | 1663 | Reserved | | | |
| D0 | 1664 | Reserved | | | |
| | 1665 | Reserved | | | |
| | 1666 | Reserved | | | |
| | 1667 | Reserved | | | |
| | 1668 | Reserved | | | |
| | 1669 | Reserved | | | |
| | 1670 | Reserved | | | |
| | 1671 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| D1 | 1672 | Reserved | | | |
| | 1673 | Reserved | | | |
| | 1674 | Reserved | | | |
| | 1675 | Reserved | | | |
| | 1676 | Reserved | | | |
| | 1677 | Reserved | | | |
| | 1678 | Reserved | | | |
| | 1679 | Reserved | | | |
| D2 | 1680 | Reserved | | | |
| | 1681 | Reserved | | | |
| | 1682 | Reserved | | | |
| | 1683 | Reserved | | | |
| | 1684 | Reserved | | | |
| | 1685 | Reserved | | | |
| | 1686 | Reserved | | | |
| | 1687 | Reserved | | | |
| D3 | 1688 | Reserved | | | |
| | 1689 | Reserved | | | |
| | 1690 | Reserved | | | |
| | 1691 | Reserved | | | |
| | 1692 | Reserved | | | |
| | 1693 | Reserved | | | |
| | 1694 | Reserved | | | |
| | 1695 | Reserved | | | |
| D4 | 1696 | Reserved | | | |
| | 1697 | Reserved | | | |
| | 1698 | Reserved | | | |
| | 1699 | Reserved | | | |
| | 1700 | Reserved | | | |
| | 1701 | Reserved | | | |
| | 1702 | Reserved | | | |
| | 1703 | Reserved | | | |
| D5 | 1704 | Reserved | | | |
| | 1705 | Reserved | | | |
| | 1706 | Reserved | | | |
| | 1707 | Reserved | | | |
| | 1708 | Reserved | | | |
| | 1709 | Reserved | | | |
| | 1710 | Reserved | | | |
| | 1711 | Reserved | | | |
| D6 | 1712 | Reserved | | | |
| | 1713 | Reserved | | | |
| | 1714 | Reserved | | | |
| | 1715 | Reserved | | | |
| | 1716 | Reserved | | | |
| | 1717 | Reserved | | | |
| | 1718 | Reserved | | | |
| | 1719 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| D7 | 1720 | Reserved | | | |
| | 1721 | Reserved | | | |
| | 1722 | Reserved | | | |
| | 1723 | Reserved | | | |
| | 1724 | Reserved | | | |
| | 1725 | Reserved | | | |
| | 1726 | Reserved | | | |
| | 1727 | Reserved | | | |
| D8 | 1728 | Reserved | | | |
| | 1729 | Reserved | | | |
| | 1730 | Reserved | | | |
| | 1731 | Reserved | | | |
| | 1732 | Reserved | | | |
| | 1733 | Reserved | | | |
| | 1734 | Reserved | | | |
| | 1735 | Reserved | | | |
| D9 | 1736 | Reserved | | | |
| | 1737 | Reserved | | | |
| | 1738 | Reserved | | | |
| | 1739 | Reserved | | | |
| | 1740 | Reserved | | | |
| | 1741 | Reserved | | | |
| | 1742 | Reserved | | | |
| | 1743 | Reserved | | | |
| DA | 1744 | Reserved | | | |
| | 1745 | Reserved | | | |
| | 1746 | Reserved | | | |
| | 1747 | Reserved | | | |
| | 1748 | Reserved | | | |
| | 1749 | Reserved | | | |
| | 1750 | Reserved | | | |
| | 1751 | Reserved | | | |
| DB | 1752 | Reserved | | | |
| | 1753 | Reserved | | | |
| | 1754 | Reserved | | | |
| | 1755 | Reserved | | | |
| | 1756 | Reserved | | | |
| | 1757 | Reserved | | | |
| | 1758 | Reserved | | | |
| | 1759 | Reserved | | | |
| DC | 1760 | Reserved | | | |
| | 1761 | Reserved | | | |
| | 1762 | Reserved | | | |
| | 1763 | Reserved | | | |
| | 1764 | Reserved | | | |
| | 1765 | Reserved | | | |
| | 1766 | Reserved | | | |
| | 1767 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| DD | 1768 | Reserved | | | |
| | 1769 | Reserved | | | |
| | 1770 | Reserved | | | |
| | 1771 | Reserved | | | |
| | 1772 | Reserved | | | |
| | 1773 | Reserved | | | |
| | 1774 | Reserved | | | |
| | 1775 | Reserved | | | |
| DE | 1776 | Reserved | | | |
| | 1777 | Reserved | | | |
| | 1778 | Reserved | | | |
| | 1779 | Reserved | | | |
| | 1780 | Reserved | | | |
| | 1781 | Reserved | | | |
| | 1782 | Reserved | | | |
| | 1783 | Reserved | | | |
| DF | 1784 | Reserved | | | |
| | 1785 | Reserved | | | |
| | 1786 | Reserved | | | |
| | 1787 | Reserved | | | |
| | 1788 | Reserved | | | |
| | 1789 | Reserved | | | |
| | 1790 | Reserved | | | |
| | 1791 | Reserved | | | |
| E0 | 1792 | Reserved | | | |
| | 1793 | Reserved | | | |
| | 1794 | Reserved | | | |
| | 1795 | Reserved | | | |
| | 1796 | Reserved | | | |
| | 1797 | Reserved | | | |
| | 1798 | Reserved | | | |
| | 1799 | Reserved | | | |
| E1 | 1800 | Reserved | | | |
| | 1801 | Reserved | | | |
| | 1802 | Reserved | | | |
| | 1803 | Reserved | | | |
| | 1804 | Reserved | | | |
| | 1805 | Reserved | | | |
| | 1806 | Reserved | | | |
| | 1807 | Reserved | | | |
| E2 | 1808 | Reserved | | | |
| | 1809 | Reserved | | | |
| | 1810 | Reserved | | | |
| | 1811 | Reserved | | | |
| | 1812 | Reserved | | | |
| | 1813 | Reserved | | | |
| | 1814 | Reserved | | | |
| | 1815 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| E3 | 1816 | Reserved | | | |
| | 1817 | Reserved | | | |
| | 1818 | Reserved | | | |
| | 1819 | Reserved | | | |
| | 1820 | Reserved | | | |
| | 1821 | Reserved | | | |
| | 1822 | Reserved | | | |
| | 1823 | Reserved | | | |
| E4 | 1824 | Reserved | | | |
| | 1825 | Reserved | | | |
| | 1826 | Reserved | | | |
| | 1827 | Reserved | | | |
| | 1828 | Reserved | | | |
| | 1829 | Reserved | | | |
| | 1830 | Reserved | | | |
| | 1831 | Reserved | | | |
| E5 | 1832 | Reserved | | | |
| | 1833 | Reserved | | | |
| | 1834 | Reserved | | | |
| | 1835 | Reserved | | | |
| | 1836 | Reserved | | | |
| | 1837 | Reserved | | | |
| | 1838 | Reserved | | | |
| | 1839 | Reserved | | | |
| E6 | 1840 | Reserved | | | |
| | 1841 | Reserved | | | |
| | 1842 | Reserved | | | |
| | 1843 | Reserved | | | |
| | 1844 | Reserved | | | |
| | 1845 | Reserved | | | |
| | 1846 | Reserved | | | |
| | 1847 | Reserved | | | |
| E7 | 1848 | Reserved | | | |
| | 1849 | Reserved | | | |
| | 1850 | Reserved | | | |
| | 1851 | Reserved | | | |
| | 1852 | Reserved | | | |
| | 1853 | Reserved | | | |
| | 1854 | Reserved | | | |
| | 1855 | Reserved | | | |
| E8 | 1856 | Reserved | | | |
| | 1857 | Reserved | | | |
| | 1858 | Reserved | | | |
| | 1859 | Reserved | | | |
| | 1860 | Reserved | | | |
| | 1861 | Reserved | | | |
| | 1862 | Reserved | | | |
| | 1863 | Reserved | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| E9 | 1864 | Reserved | | | |
| | 1865 | Reserved | | | |
| | 1866 | Reserved | | | |
| | 1867 | Reserved | | | |
| | 1868 | Reserved | | | |
| | 1869 | Reserved | | | |
| | 1870 | Reserved | | | |
| | 1871 | Reserved | | | |
| EA | 1872 | Reserved | | | |
| | 1873 | Reserved | | | |
| | 1874 | Reserved | | | |
| | 1875 | Reserved | | | |
| | 1876 | Reserved | | | |
| | 1877 | Reserved | | | |
| | 1878 | Reserved | | | |
| | 1879 | Reserved | | | |
| EB | 1880 | Reserved | | | |
| | 1881 | Reserved | | | |
| | 1882 | Reserved | | | |
| | 1883 | Reserved | | | |
| | 1884 | Reserved | | | |
| | 1885 | Reserved | | | |
| | 1886 | Reserved | | | |
| | 1887 | Reserved | | | |
| EC | 1888 | Reserved | | | |
| | 1889 | Reserved | | | |
| | 1890 | Reserved | | | |
| | 1891 | Reserved | | | |
| | 1892 | Reserved | | | |
| | 1893 | Reserved | | | |
| | 1894 | Reserved | | | |
| | 1895 | Reserved | | | |
| ED | 1896 | Reserved | | | |
| | 1897 | Reserved | | | |
| | 1898 | Reserved | | | |
| | 1899 | Reserved | | | |
| | 1900 | Reserved | | | |
| | 1901 | Reserved | | | |
| | 1902 | Reserved | | | |
| | 1903 | Reserved | | | |
| EE | 1904 | Reserved | | | |
| | 1905 | Reserved | | | |
| | 1906 | Reserved | | | |
| | 1907 | Reserved | | | |
| | 1908 | Reserved | | | |
| | 1909 | Reserved | | | |
| | 1910 | Reserved | | | |
| | 1911 | Reserved | | | |

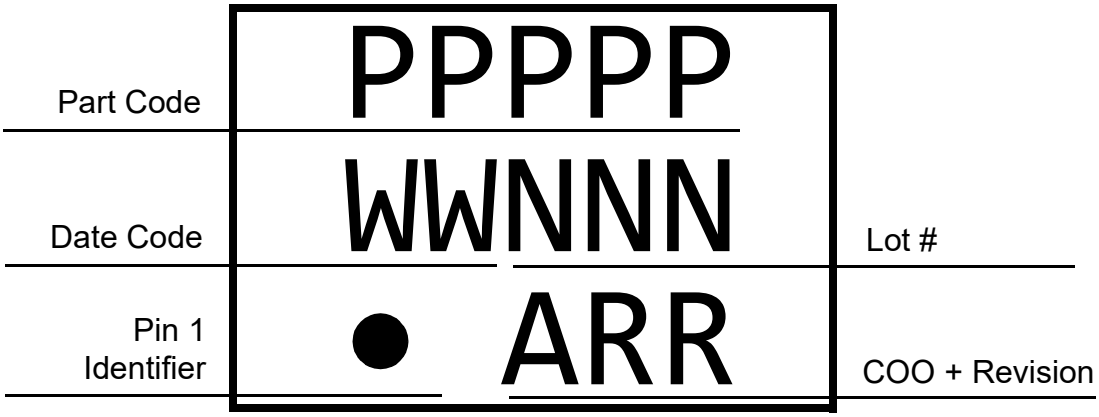
| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| EF | 1912 | Reserved | | | |
| | 1913 | Reserved | | | |
| | 1914 | Reserved | | | |
| | 1915 | Reserved | | | |
| | 1916 | Reserved | | | |
| | 1917 | Reserved | | | |
| | 1918 | Reserved | | | |
| | 1919 | Reserved | | | |
| F0 | 1920 | Reserved | | | |
| | 1921 | Reserved | | | |
| | 1922 | Reserved | | | |
| | 1923 | Reserved | | | |
| | 1924 | Reserved | | | |
| | 1925 | Reserved | | | |
| | 1926 | Reserved | | | |
| | 1927 | Reserved | | | |
| F1 | 1928 | Reserved | | | |
| | 1929 | Reserved | | | |
| | 1930 | Reserved | | | |
| | 1931 | Reserved | | | |
| | 1932 | Reserved | | | |
| | 1933 | Reserved | | | |
| | 1934 | Reserved | | | |
| | 1935 | Reserved | | | |
| F2 | 1936 | Reserved | | | |
| | 1937 | Reserved | | | |
| | 1938 | Reserved | | | |
| | 1939 | Reserved | | | |
| | 1940 | Reserved | | | |
| | 1941 | Reserved | | | |
| | 1942 | Reserved | | | |
| | 1943 | Reserved | | | |
| F3 | 1944 | Reserved | | | |
| | 1945 | Reserved | | | |
| | 1946 | Reserved | | | |
| | 1947 | Reserved | | | |
| | 1948 | Reserved | | | |
| | 1949 | Reserved | | | |
| | 1950 | Reserved | | | |
| | 1951 | Reserved | | | |
| F4 | 1952 | GPO0 I2C output expender data | | | |
| | 1953 | GPO0 I2C output expender select | 0: GPO0 output come from matrix<br>1: GPO0 output is register | | |
| | 1954 | GPIO6 I2C output expender data | | | |
| | 1955 | GPIO6 I2C output expender select | 0: GPIO6 output come from matrix<br>1: GPIO6 output is register | | |
| | 1956 | GPIO7 I2C output expender data | | | |
| | 1957 | GPIO7 I2C output expender select | 0: GPIO7 output come from matrix<br>1: GPIO7 output is register | | |
| | 1958 | GPIO8 I2C output expender data | | | |
| | 1959 | GPIO8 I2C output expender select | 0: GPIO8 output come from matrix<br>1: GPIO8 output is register | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| F5 | 1960 | Reserved | | | |
| | 1961 | Reserved | | | |
| | 1962 | Reserved | | | |
| | 1963 | Reserved | | | |
| | 1964 | Reserved | | | |
| | 1965 | Reserved | | | |
| | 1966 | Reserved | | | |
| | 1967 | Reserved | | | |
| F6 | 1968 | Reserved | | | |
| | 1969 | | | | |
| | 1970 | | | | |
| | 1971 | | | | |
| | 1972 | | | | |
| | 1973 | | | | |
| | 1974 | | | | |
| | 1975 | | | | |
| F7 | 1976 | Reserved | | | |
| | 1977 | | | | |
| | 1978 | | | | |
| | 1979 | | | | |
| | 1980 | | | | |
| | 1981 | | | | |
| | 1982 | | | | |
| | 1983 | | | | |
| F8 | 1984 | Reserved | | | |
| | 1985 | | | | |
| | 1986 | | | | |
| | 1987 | | | | |
| | 1988 | | | | |
| | 1989 | | | | |
| | 1990 | | | | |
| | 1991 | | | | |
| F9 | 1992 | Reserved | | | |
| | 1993 | Reserved | | | |
| | 1994 | Reserved | | | |
| | 1995 | | | | |
| | 1996 | Reserved | | | |
| | 1997 | | | | |
| | 1998 | | | | |
| | 1999 | | | | |
| FA | 2000 | Reserved | | | |
| | 2001 | | | | |
| | 2002 | | | | |
| | 2003 | | | | |
| | 2004 | | | | |
| | 2005 | | | | |
| | 2006 | | | | |
| | 2007 | | | | |

| Address | | Signal Function | Register Bit Definition | I²C Interface | |
|---|---|---|---|---|---|
| Byte | Register Bit | | | Read | Write |
| FB | 2008 | Reserved | | | |
| | 2009 | | | | |
| | 2010 | | | | |
| | 2011 | | | | |
| | 2012 | | | | |
| | 2013 | | | | |
| | 2014 | | | | |
| | 2015 | | | | |
| FC | 2016 | Reserved | | | |
| | 2017 | | | | |
| | 2018 | | | | |
| | 2019 | | | | |
| | 2020 | | | | |
| | 2021 | | | | |
| | 2022 | | | | |
| | 2023 | | | | |
| FD | 2024 | Reserved | | | |
| | 2025 | | | | |
| | 2026 | | | | |
| | 2027 | | | | |
| | 2028 | Reserved | | | |
| | 2029 | Reserved | | | |
| | 2030 | Reserved | | | |
| | 2031 | Reserved | | | |
| FE | 2032 | Reserved | | | |
| | 2033 | Reserved | | | |
| | 2034 | Reserved | | | |
| | 2035 | Reserved | | | |
| | 2036 | Reserved | | | |
| | 2037 | Reserved | | | |
| | 2038 | Reserved | | | |
| | 2039 | Reserved | | | |
| FF | 2040 | Reserved | | | |
| | 2041 | | | | |
| | 2042 | | | | |
| | 2043 | | | | |
| | 2044 | | | | |
| | 2045 | | | | |
| | 2046 | | | | |
| | 2047 | | | | |

# 19 Package Top Marking Definitions

## 19.1 MSTQFN 20L 1.6 MM X 3 MM 0.4P FC PACKAGE

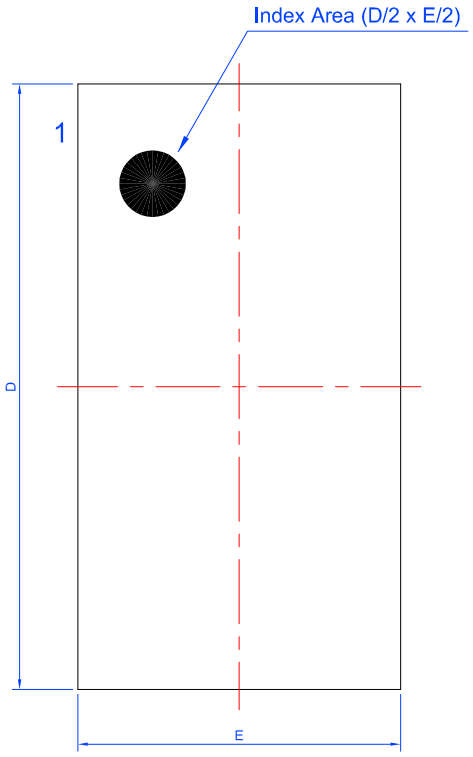



PPPPP - Part ID Field identifies the specific device configuration
WW - Date Code Field: Coded date of manufacture
NNN - Lot Code: Designates Lot #
A - Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR - Revision Code: Device Revision

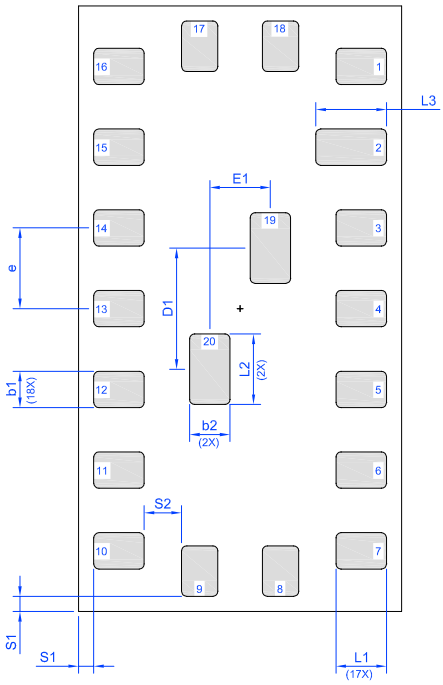
# 20 Package Information

## 20.1 PACKAGE OUTLINES MSTQFN 20L 1.6 MM X 3.0 MM X 0.4 MM 0.4P FC PACKAGE

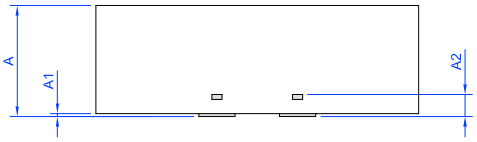
**JEDEC MO-220**
**IC Net Weight: 0.0064 g**




**Marking View**




**BTM View**




**Side View**

Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.00 | - | 0.01 | E | 1.55 | 1.60 | 1.65 |
| A2 | 0.11 REF | | | e | 0.40 BSC | | |
| b1 | 0.13 | 0.18 | 0.23 | L1 | 0.20 | 0.25 | 0.30 |
| b2 | 0.15 | 0.20 | 0.25 | L2 | 0.30 | 0.35 | 0.40 |
| S1 | 0.075 REF | | | L3 | 0.30 | 0.35 | 0.40 |
| S2 | 0.185 REF | | | D1 | 0.60 BSC | | |
| | | | | E1 | 0.30 BSC | | |

## 21 MSTQFN Handling

Be sure to handle MSTQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle MSTQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

## 22 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 $mm^3$ (nominal) for MSTQFN 20L Package. More information can be found at www.jedec.org.

## 23 Ordering Information

| Part Number | Type |
|---|---|
| SLG46867M | 20-pin MSTQFN |
| SLG46867MTR | 20-pin MSTQFN - Tape and Reel (3k units) |

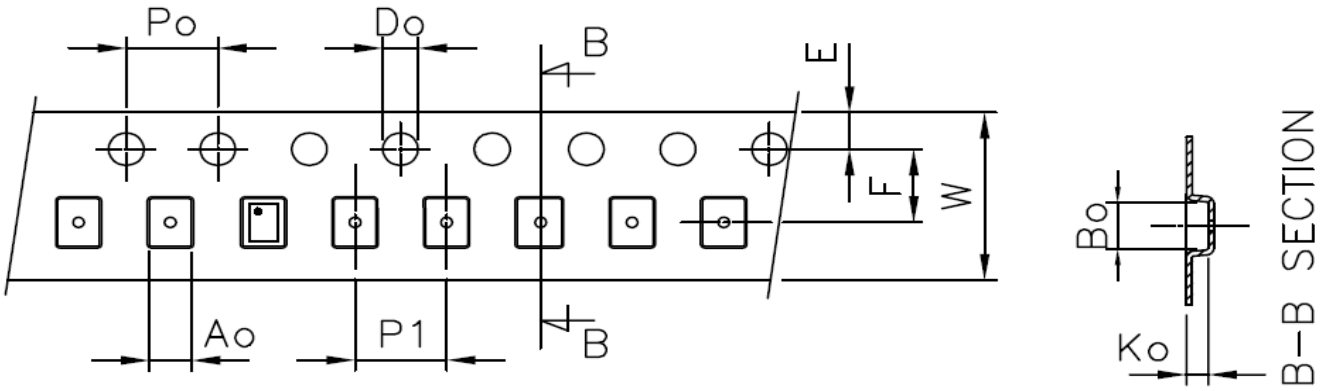
### 23.1 TAPE AND REEL SPECIFICATIONS

| Package Type | # of Pins | Nominal Package Size (mm) | Max Units | | Reel & Hub Size (mm) | Leader (min) | | Trailer (min) | | Tape Width (mm) | Part Pitch (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length (mm) | Pockets | Length (mm) | | |
| MSTQFN 20L 1.6 mm x 3 mm 0.4P FC Green | 20 | 1.6x3.0x0.55 | 3000 | 3000 | 178/60 | 100 | 400 | 100 | 400 | 8 | 4 |

### 23.2 CARRIER TAPE DRAWING AND DIMENSIONS

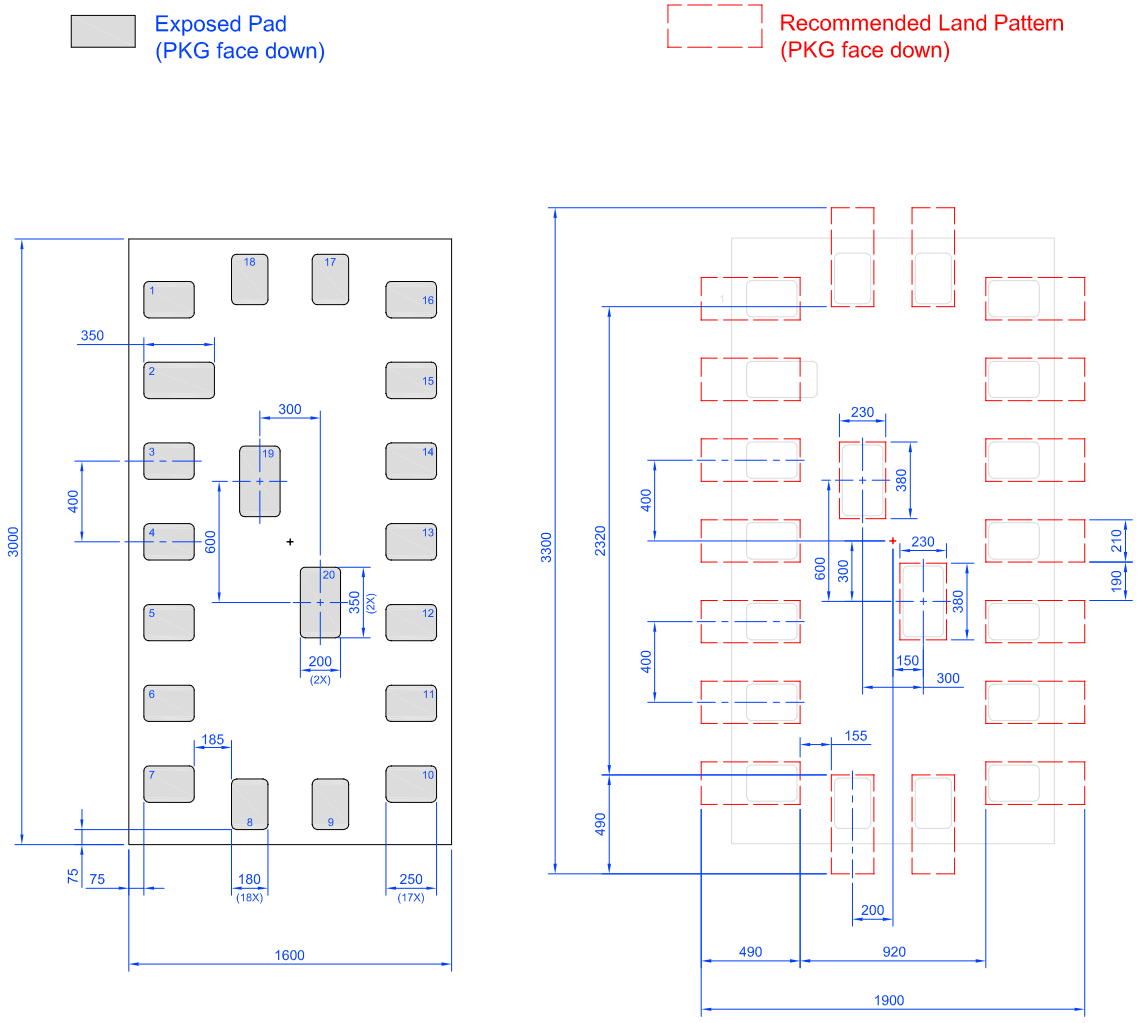
| Package Type | Pocket BTM Length (mm) | Pocket BTM Width (mm) | Pocket Depth (mm) | Index Hole Pitch (mm) | Pocket Pitch (mm) | Index Hole Diameter (mm) | Index Hole to Tape Edge (mm) | Index Hole to Pocket Center (mm) | Tape Width (mm) |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| MSTQFN 20L 1.6 mm x 3 mm 0.4P FC Green | 1.78 | 3.18 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |

### 23.3 MSTQFN 20L



# 24 Layout Guidelines

## 24.1 MSTQFN 20L 1.6 MM X 3.0 MM X 0.4 MM 0.4P FC PACKAGE




**Marking View**

**Unit:** µm

## Glossary

| | |
|---|---|
| ACK | Acknowledge bit |
| ACMP | Analog Comparator |
| ACMPH | Analog Comparator High Speed |
| ACMPL | Analog Comparator Low Power |
| BG | Bandgap |
| CLK | Clock |
| CMO | Connection matrix output |
| CNT | Counter |
| DFF | D flip-flop |
| DLY | Delay |
| EC | Electrical Characteristics |
| ESD | Electrostatic discharge |
| EV | End Value |
| FSM | Finite State Machine |
| GPI | General Purpose Input |
| GPIO | General Purpose Input/Output |
| GPO | General Purpose Output |
| IN | Input |
| IO | Input/Output |
| LPF | Low Pass Filter |
| LSB | Least Significant Bit |
| LUT | Look-Up Table |
| LV | Low Voltage |
| MSB | Most Significant Bit |
| MUX | Multiplexer |
| NPR | Non-Volatile Memory Read/Write/Erase Protection |
| nRST | Reset |
| NVM | Non-Volatile Memory |
| OD | Open Drain |
| OE | Output Enable |
| OSC | Oscillator |
| OTP | One-Time-Programmable |
| OUT | Output |
| PD | Power Down |
| PGEN | Pattern Generator |
| POR | Power-On Reset |
| PP | Push Pull |
| PWR | Power |

| | |
|---|---|
| PWR_SW_ON | Power Switch On |
| P DLY | Programmable Delay |
| R/W | Read/Write |
| SCL | $I^2C$ Clock Input |
| SDA | $I^2C$ Data Input/Output |
| SLA | Slave Address |
| SMT | With Schmitt Trigger |
| SV | nSET Value |
| SW | Switch |
| TS | Temperature Sensor |
| VRef | Voltage Reference |
| WOSMT | Without Schmitt Trigger |
| WS | Wake and Sleep Controller |

## Revision History

| Revision | Date | Description |
|---|---|---|
| 3.2 | 9-Aug-2018 | Fixed typos |
| 3.1 | 7-Jun-2018 | Fixed typos<br>Fixed Package Marking Spec<br>Updated package weight |
| 3.0 | 25-May-2018 | Final version |

## Status Definitions

| Version | Datasheet Status | Product Status | Definition |
|---|---|---|---|
| 1.[n] | Target | Development | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| 2.[n] | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
| 3.[n] | Final | Production | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com. |
| 4.[n] | Obsolete | Archived | This datasheet contains the specifications for discontinued products. The information is provided for reference only. |

## Disclaimer



## RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

# Contacting Dialog Semiconductor

**United Kingdom (Headquarters)**
*Dialog Semiconductor (UK) LTD*
Phone: +44 1793 757700

**Germany**
*Dialog Semiconductor GmbH*
Phone: +49 7021 805-0

**The Netherlands**
*Dialog Semiconductor B.V.*
Phone: +31 73 640 8822

**Email:**
enquiry@diasemi.com

**North America**
*Dialog Semiconductor Inc.*
Phone: +1 408 845 8500

**Japan**
*Dialog Semiconductor K. K.*
Phone: +81 3 5769 5100

**Taiwan**
*Dialog Semiconductor Taiwan*
Phone: +886 281 786 222

**Web site:**
www.dialog-semiconductor.com

**Hong Kong**
*Dialog Semiconductor Hong Kong*
Phone: +852 2607 4271

**Korea**
*Dialog Semiconductor Korea*
Phone: +82 2 3469 8200

**China (Shenzhen)**
*Dialog Semiconductor China*
Phone: +86 755 2981 3669

**China (Shanghai)**
*Dialog Semiconductor China*
Phone: +86 21 5424 9058