PLESSEY
Semiconductors

SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

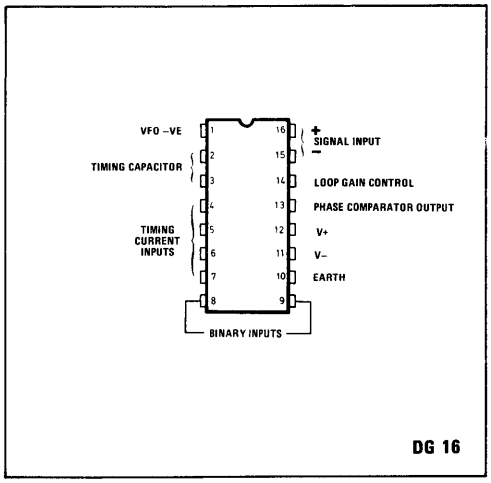

Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	0°C to +70°C
Supply Currents	1.5mA typ.

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	–55° to +175°C
Operating temperature	–55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	mA	I_{14} = 0

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

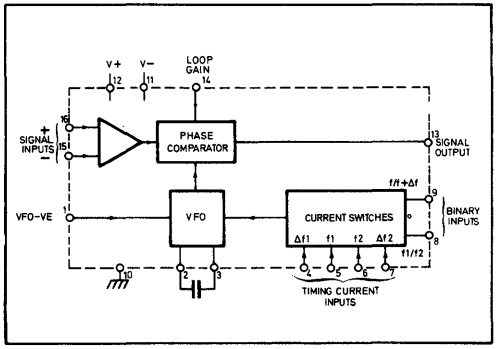

Fig. 2 SL652C block diagram

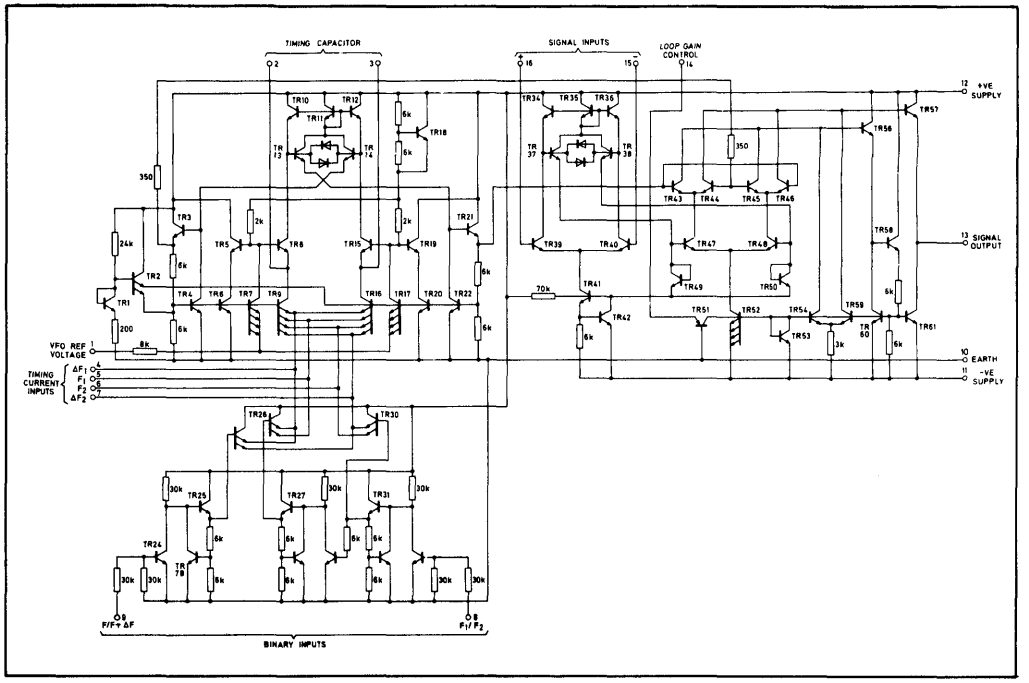

Fig. 3 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 5 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

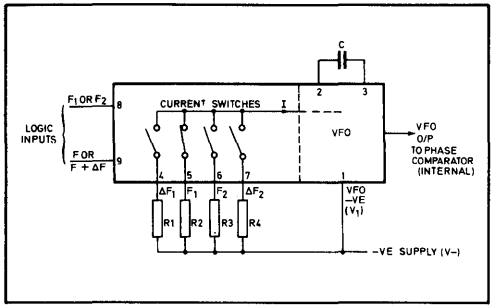

Fig. 4 VFO and binary interface

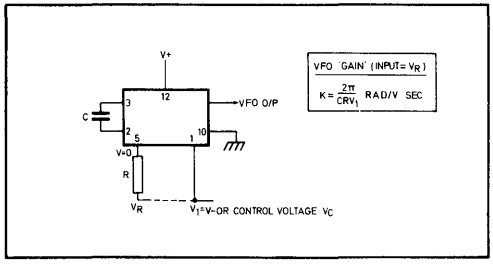

Fig. 5 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 6):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16}-V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16}-V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

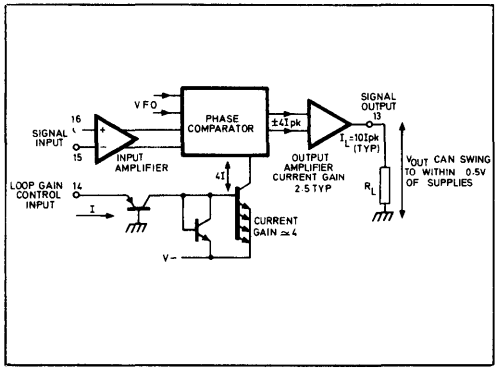

Fig 6. Phase comparator