SL38160

Programmable 4-PLL CG with VCXO and SSCG

Key Features

- 4 Programmable PLLs with up to 5 Clock Outputs
- Programmable VCXO and SSCG options
- Wide 2.5V to 3.3V +/-10% power supply range
- Low power dissipation and low jitter
- Programmable Center or Down Spread Modulation from 0.25 to 5.0%
- 8 to 48 MHz external crystal range
- 8 to 166 MHz external clock input range
- Programmable 1 to 200 MHz clock output range
- Integrated internal voltage regulator
- FS1/2 functions
- Programmable CL at XIN and XOUT pins
- Programmable output rise and fall times
- 16-pin TSSOP package with commercial and industrial temperature ranges

Applications

- DTV
- STB and DVD-R/W
- Printers, MFPs, Digital Copiers
- Routers and Servers
- General Purpose Frequency Synthesising

Description

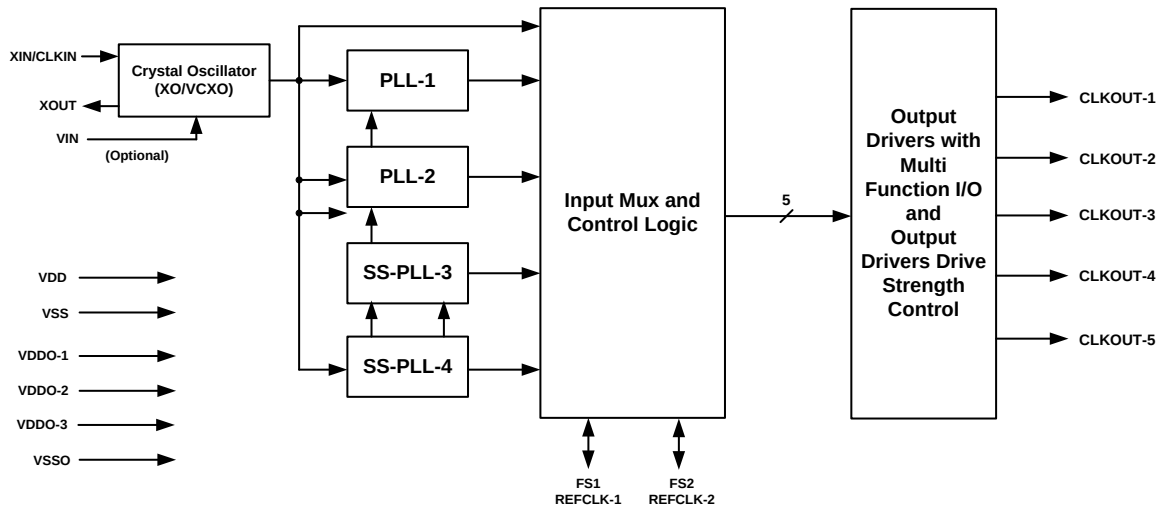
The SL38160 4 PLL programmable low power Clock Generator with SSCG and VCXO functions used for reducing Electromagnetic Interference (EMI) and general purpose frequency synthesizing. The product is designed using SpectraLinear proprietary programmable **EProClock™** phase-locked loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and modulate the input clock. The modulated clock can significantly reduce the measured EMI levels, and leading to the compliance with regulatory agency requirements.

Up to 5 output clock frequencies, spread %, output rise and fall times for each clock outputs, crystal load, spread modulation frequency and FS1/2 functions can be programmed to meet the needs of wide range of applications. The SL38160 operates from 2.5V to 3.3V, +/-10% power supply voltage range. The product is offered in 16-pin TSSOP package with commercial and industrial grades.

Benefits

- Complete VCXO with +/-120ppm typical pull range
- Peak EMI reduction of 8 to 16 dB
- Fast time-to-market
- Cost Reduction
- Reduction of PCB layers
- Eleminates the need for XOs and VCXOs

Block Diagram



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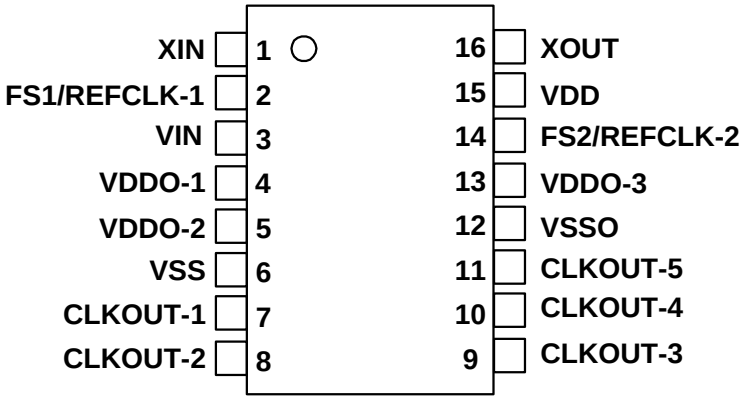
Pin Configuration



16-Pin TSSOP Package

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	XIN/CLKIN	Input	Crystal oscillator input in VCXO and Xo mode or external clock input in XO mode only. Oscillator powered by VDD.
2	FS1 or REFCLK-1	Input	OE (output Enable).
3	VIN	Input	VCXO control pin VIN. This pin is not used and is not connected (n/c) in crystal oscillator mode.
4	VDDO-1	Power	3.3V to 2.5V +/-10% Positive Power Supply. VDDO-1 powers clock output drivers for CLKOUT1/2. VDD≥VDDO.
5	VDDO-2	Power	3.3V to 2.5V +/-10% Positive Power Supply. VDDO-1 powers clock output driver for CLKOUT3. VDD≥VDDO.
6	VSS	Power	VDD power ground.
7	CLKOUT-1	Output	Programmable clock output-1, this pin can be programmed as synthesized clock output with or without spread or REFOUT and is powered by VDD-1.
8	CLKOUT-2	Output	Programmable clock output-2, this pin can be programmed as synthesized clock output with or without spread or REFOUT and powered by VDDO-1.
9	CLKOUT-3	Output	Programmable clock output-3, this pin can be programmed as synthesized clock output with or without spread or REFOUT and powered by VDDO-2.
10	CLKOUT-4	Output	Programmable clock output-4, this pin can be programmed as synthesized clock output with or without spread or REFOUT and powered by VDDO-3.

11	CLKOUT-5	Output	Programmable clock output-5, this pin can be programmed as synthesized clock output with or without spread or REFOUT and powered by VDDO-3.
12	VSSO	Power	VDDO-1/2/3 power ground.
13	VDDO-2	Power	3.3V to 2.5V +/-10% Positive Power Supply. VDD-2 powers clock output drivers for CLKOUT4/5. VDD≥VDDO.
14	FS2 or REFCLK-2	Input	Function Select FS2 input. This pin can be programmed in XO mode as REFCLK which is the buffered output of input crystal or CLKIN.
15	VDD	Power	3.3V to 2.5V +/-10% Positive Power Supply. Powers only digital core, PLLs and oscillator.
16	XOUT	Output	Crystal oscillator output. Oscillator powered by VDD.

General Description

The primary source of EMI from digital circuits is the system clock and all the other synchronous clock and control signals derived from the system clock. The well know techniques of filtering (suppression) and shielding (containment), while effective, can cost money, board space and longer development time.

A more effective and efficient technique to reduce EMI is Spread Spectrum Clock Generator (SSCG) technique to control and reduce EMI emissions. Instead of using constant clock frequency, the SSCG technique modulates the system clock with much smaller frequency, to reduce EMI emissions at its source: The System Clock.

The SL38160 is a Spread Spectrum Clock Generator (SSCG) IC used for the purpose of reducing electromagnetic interference (EMI) found in today's high-speed digital electronic systems.

The devices use a SpectraLinear proprietary phase-locked loop (PLL) and Spread Spectrum Technologies (SST) to synthesize and modulate (spread) the system clock such that the energy is spread out over a wider bandwidth. This reduces the peak radiated emissions at the fundamental and the harmonics. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency requirements and improve time-to-market without degrading system performance.

The SL38160 is available in 16-pin TSSOP packages with a Commercial Temperature range of 0 to 70°C and Industrial Temperature range of –40 to 85°C.

Refer to 28-pin TSSOP package version of SL38160, called SL38000, for up to nine programmable outputs and additional control functions

Input Frequency Range

The input frequency range is from 8.0 to 48.0 MHz for crystals in XO Mode. If an external driven clock is used, the input frequency range is from 3 to 166 MHz.
In VCXO mode pullable crystal range is 13 to 30MHz.

Output Frequency Range

The five clock outputs can be programmed as CLKOUT, SSCLK or REFCLK. If VDD=VDDO=3.3V, output frequency range is 3 to 200MHz with CL=15pF-max. If VDD=3.3V and VDDO=2.5V, output frequency range for CLKOUT-2/3/4/5 is 3 to 166MHz. REFCLK is the buffered output of the oscillator and can be programmed from 0.25 to 48MHz in XO mode and 25 to 30MHz in VCXO mode.

Programmable Output Rise and Fall Times

The each output clock drivers can be programmed independently for different frequencies and load conditions to improve signal integrity and EMI radiation levels. Refer Table 1 for available seven rise and fall time program values.

Programmable CL (Crystal Load) in XO Mode

The SL38160 provides programmable on-chip capacitors at XIN/CLKIN (Pin-1) and XOUT (Pin-16). The resolution of this programmable capacitor is 6-bits with LSB value of 0.5pF. When all bits are off the pin capacitance is CXIN=CXOUT =8.5pF (minimum value). When all bits are on the pin capacitance at these pins is CXIN=CXOUT=40pF (maximum value).
The values of CXIN and CXOUT based on the CL (Crystal Load Capacitor) can be calculated as:
CXIN=CXOUT=2CL-C_{PCB}.

In addition, if an external clock is used, the capacitance at Pin-1 (CLKIN) can programmed to control the edge rate of this input clock, providing additional EMI control.

Programmable Modulation Frequency

The Spread Spectrum Clock (SSC) modulation default value is 31.5 kHz. The higher values of 60, 90 and 120 kHz can also be programmed. Less than 30 kHz modulation frequency is not recommended to stay out of the range audio frequency bandwidth.

Spread Percent (%)

The spread percent (%) value is programmable from +/-0.25% to +/-2.5% (center spread) or -0.5% to -5.0% (down spread) for all input and SSCLK frequencies. It is possible to program smaller or larger values of spread percent for certain frequencies. Contact SLI if these non-standard spread percent values are required.

VDD/VDDO

SL38160 provides two separate VDDO1 and VDDO-2 power pins to power CLKOUT-1/-2/-3 and CLKOUT-3/-4 clock output drivers respectively. VDD pin powers digital core, PLLs and crystal oscillator in both XO and VCXO modes. VDD and VDD0 can be 2.5V to 3.3V +/-10% where VDD≥VDDO.

XO/VCXO Modes

SL38160 can be programmed to operate in XO or VCXO mode. If XO mode is selected external crystal can be 8 to 48MHz. Refer to Table 3 for recommended XO crystal specifications.
In VCXO mode 25 to 30 MHz pullable crystal must be used. Refer to Table 4 for pullable VCXO crystal specifications.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD	**VDD and VDDO**	**-0.5**	**4.2**	**V**
Supply voltage, VDDO	**VDDO≤VDD**	**-**	**VDD**	**V**
All Inputs and Outputs		**-0.5**	**VDD+0.5**	**V**
Ambient Operating Temperature	**In operation, C-Grade**	**0**	**70**	**°C**
Ambient Operating Temperature	**In operation, I-Grade**	**-40**	**85**	**°C**
Storage Temperature	**No power is applied**	**-65**	**150**	**°C**
Junction Temperature	**In operation, power is applied**	**-**	**125**	**°C**
Soldering Temperature		**-**	**260**	**°C**
ESD Rating (Human Body Model)	**JEDEC22-A114D**	**-4,000**	**4,000**	**V**
ESD Rating (Charge Device Model)	**JEDEC22-C101C**	**-1,500**	**1,500**	**V**
ESD Rating (Machine Model)	**JEDEC22-A115D**	**-250**	**250**	**V**

DC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD=VDDO=2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	2.5V to 3.3V +/-10%	2.25	3.3	3.63	V
Operating Voltage	VDDO	2.5V to 3.3V +/-10%, VDD≥VDDO.	2.25	3.3	3.63	
Output High Voltage	VOH1	IOH=-6mA , Pins programmed as CLKOUT/REFOUT	VDD-0.5	-	-	V
Output Low Voltage	VOL1	IOL=6mA , Pins programmed as CLKOUT/REFOUT	-	-	0.5	V
Operating Supply Current	IDD1	FIN=27MHz and all 5 clocks are at 33MHz and CL=0, VDD=VDDO=3.3V	-	TBD	TBD	mA
Operating Supply Current	IDD2	FIN=27MHz and all 5 clocks are at 33MHz and CL=0, VDD=VDDO=2.5V	-	TBD	TBD	mA
Operating Supply Current	IDD3	FIN=27MHz and all 5 clocks are at 66MHz and CL=0 VDD=VDDO=3.3V	-	TBD	TBD	mA
Operating Supply Current	IDD3	FIN=27MHz and all 5 clocks are at 66MHz and CL=0 VDD=VDDO=2.5V	-	TBD	TBD	mA
Programmable XO mode, Input Crystal Load (CL) Capacitance at Pins 1 and 16	Cin Cout	Minimum setting value	-	12	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (C-Grade)

Unless otherwise stated VDD=VDD= 2.5 to 3.3V+/-10%, CL=15pF and Ambient Temperature range 0 to +70°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	XO Mode, Fundamental Crystal	8	-	48	MHz
Input Frequency Range	FIN2	VCXO Mode, Pullable Crystal	13	27	30	MHz
Input Frequency Range	FIN3	External clock input, Pin 1	3	-	166	MHz
Output Frequency Range	FOUT1	Programmable CLKOUT, Pins 7, 8, 9,10 and 11, VDD=VDDO=3.3V	3	-	200	MHz
Output Frequency Range	FOUT2	Programmable CLKOUT, Pins 8, 9,10 and 11, VDD=VDDO=2.5V	3	-	166	MHz
Output Frequency Range	FOUT3	Programmable REFCLK, Pins 7, 8, 9,10 and 1, crystal input mode is used	0.25	-	48	MHz
Output Frequency Range	FOUT4	Programmable REFCLK, Pins 7, 8, 9,10 and 1, crystal input mode and CLKIN is used	0.25	-	166	MHz
Output Duty Cycle	DC1	CLKOUT, Pins 7, 8, 9,10 and 11	45	50	55	%
Output Duty Cycle	DC2	REFCLK, Pins 7, 8, 9,10 and 11	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	30	50	70	%
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=27MHz crystal, all 5 clocks are programmed at 33MHz, CL=10pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=27MHz, all 5 clocks are programmed at 66MHz, CL=10pF	-	TBD	TBD	ps
Power supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
PLL Lock Time	tPLL	Time from VDD reaching minimum specified value to valid output frequencies at all outputs	-	7.5	9.0	ms
Spread Percent Range	SPR-1	Center Spread	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread	-5.0	-	-0.25	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz
VCXO Pull Range	ΔFVCXO	VCXO Crystal Pull Range	+/-110	+/-120	-	ppm

DC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD=VDDO=2.5V to 3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85°C

Description	Symbol	Condition	Min	Typ	Max	Unit
Operating Voltage	VDD	2.5V to 3.3V +/-10%	2.25	3.3	3.63	V
Operating Voltage	VDDO	2.5V to 3.3V +/-10%, VDD≥VDDO.	2.25	3.3	3.63	
Output High Voltage	VOH1	IOH=-6mA , Pins programmed as CLKOUT/REFOUT	VDD-0.5	-	-	V

Output Low Voltage	VOL1	IOL=6mA , Pins programmed as CLKOUT/REFOUT	-	-	0.5	V
Operating Supply Current	IDD1	FIN=27MHz and all 5 clocks are at 33MHz and CL=0, VDD=VDDO=3.3V	-	TBD	TBD	mA
Operating Supply Current	IDD2	FIN=27MHz and all 5 clocks are at 33MHz and CL=0, VDD=VDDO=2.5V	-	TBD	TBD	mA
Operating Supply Current	IDD3	FIN=27MHz and all 5 clocks are at 66MHz and CL=0 VDD=VDDO=3.3V	-	TBD	TBD	mA
Operating Supply Current	IDD3	FIN=27MHz and all 5 clocks are at 66MHz and CL=0 VDD=VDDO=2.5V	-	TBD	TBD	mA
Programmable XO mode, Input Crystal Load (CL) Capacitance at Pins 1 and 16	Cin Cout	Minimum setting value	-	12	-	pF
		Maximum setting value	-	40	-	pF
		Resolution (programming steps)	-	0.5	-	pF
Load Capacitance	CL	All CLKOUT outputs	-	-	15	pF

AC Electrical Characteristics (I-Grade)

Unless otherwise stated VDD=VDD= 2.5 to 3.3V+/-10%, CL=15pF and Ambient Temperature range -40 to +85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency Range	FIN1	XO Mode, Fundamental Crystal	8	-	48	MHz
Input Frequency Range	FIN2	VCXO Mode, Pullable Crystal	13	27	30	MHz
Input Frequency Range	FIN3	External clock input, Pin 1	3	-	166	MHz
Output Frequency Range	FOUT1	Programmable CLKOUT, Pins 7, 8, 9,10 and 11, VDD=VDDO=3.3V	3	-	200	MHz
Output Frequency Range	FOUT2	Programmable CLKOUT, Pins 8, 9,10 and 11, VDD=VDDO=2.5V	3	-	166	MHz
Output Frequency Range	FOUT3	Programmable REFCLK, Pins 7, 8, 9,10 and 1, crystal input mode is used	0.25	-	48	MHz
Output Frequency Range	FOUT4	Programmable REFCLK, Pins 7, 8, 9,10 and 1, crystal input mode and CLKIN is used	0.25	-	166	MHz
Output Duty Cycle	DC1	CLKOUT, Pins 7, 8, 9,10 and 11	45	50	55	%
Output Duty Cycle	DC2	REFCLK, Pins 7, 8, 9,10 and 11	45	50	55	%
Input Duty Cycle	DCIN	Clock Input, Pin 3	30	50	70	%
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ1	FIN=27MHz crystal, all 5 clocks are programmed at 33MHz, CL=10pF	-	TBD	TBD	ps
Cycle-to-Cycle Jitter (SSCLK – Pins 4/6/7/8)	CCJ2	FIN=27MHz, all 5 clocks are programmed at 66MHz, CL=10pF	-	TBD	TBD	ps

Power supply Ramp Time	tPSR	Time for VDD reaching minimum specified value and monolithic power supply ramp	-	-	12	ms
PLL Lock Time	tPLL	Time from VDD reaching minimum specified value to valid output frequencies at all outputs	-	7.5	9.0	ms
Spread Percent Range	SPR-1	Center Spread	+/-0.125	-	+/-2.5	%
Spread Percent Range	SPR-2	Down Spread	-5.0	-	-0.25	%
Modulation Frequency	FMOD	Programmable, 31.5 kHz standard	25	31.5	120	kHz
VCXO Pull Range	ΔFVCXO	VCXO Crystal Pull Range	+/-110	+/-120	-	ppm

Clock Output	Frequency Selection Pins	Selected Number of Frequencies
TBD	**TBD**	**TBD**
TBD	**TBD**	**TBD**
TBD	**TBD**	**TBD**
TBD	**TBD**	**TBD**

Table 1. Frequency Selection Options for Clock Outputs

Programmable Output Clock (CLKOUT) Rise and Fall Times

The output clock rise and fall times (tr/tf) of each clock output can be programmed independently to match drive level to load impedance.

Programming Code	VDDO=3.3V CL=15pF	VDDO=2.5V CL=15pF	Unit
000	4.00	4.80	ns
001	2.00	2.60	ns
010	1.40	1.80	ns
011	1.10	1.40	ns
100	0.85	1.10	ns
101	0.70	0.90	ns
110	0.55	0.70	ns

Table 2. Programmable CLKOUT Rise and Fall Times

Notes:

1. All typical values are at respective nominal VDD values.
2. The worst case rise and fall times variations are +/- 20% for C-Grade and +/-30% for I-grade.

Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between all VDD and VSS pins on PCB. Place the capacitor on the component side of the PCB as close to the VDD pins as possible. The PCB trace to the VDD pins and to the GND via should be kept as short as possible Do not use vias between the decoupling capacitor and the VDD pins.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs (CLKOUT or REFCLK pins) and the load is over 1 ½ inch. The nominal impedance of the all clock outputs are about 25 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the SSCLK output as possible.

Crystal and Crystal Load (XO Mode): Use only parallel resonant fundamental crystals. DO NOT USE higher overtone crystals. To meet the crystal initial accuracy specification (in ppm); the internal on-chip programmable capacitors PCin and PCout must be programmed to match the crystal load requirement. These values are given by the formula below:

$$PCin(pF) = PCout(pF) = [(CL(pF) - Cp(pF)/2)] \times 2$$

Where CL is crystal load capacitor as given by the crystal datasheet and Cp(pF) is the compensation factor for the total parasitic capacitance at XIN or XOUT pin including PCB related parasitic capacitance.

As an example; if a crystal with CL=18pF is used and Cp=4pF, by using the above formula, PCin=PCout=[(18-(4/2)] x 2 = 32pF. Programming PCin and PCout to 32pF assures that this crystal sees an equivalent load of 18pF and no other external crystal load capacitor is needed. Deviating from the crystal load specification could cause an increase in frequency accuracy in ppm. Refer to the Table 5 for the recommended crystal specifications.

Recommended External Crystal Specifications (XO Version)

Parameter	Description	Min	Typ	Max	Unit	Comments
FNOM	Nominal Crystal Frequency Range	8	-	48	MHz	Fundamental Mode – AT Cut
CL	Nominal Crystal Load	6	12	18	pF	Load for +/-0 ppm Fo resonance value
R1,1	Equivalent Series Resistance	20	40	100	Ohm	F-Range: 8.0 to 12.999 MHz
R1,2	Equivalent Series Resistance	12.5	25	60	Ohm	F-Range: 13.0 to 19.999 MHz
R1,3	Equivalent Series Resistance	10	20	50	Ohm	F-Range: 20.0 to 48.000 MHz
DL1,1	Crystal Drive Level	-	-	200	µW	F-Range: 8.0 to 19.999 MHz
DL1,2	Crystal Drive Level	-	-	150	µW	F-Range: 20.0 to 48.000 MHz
Co1	Shunt Capacitance	-	4	5.4	pF	SMD Xtals
Co2	Shunt Capacitance	-	5	7.2	pF	Through Hole (Leaded) Xtals

Table 3. Crystal Specifications (XO Version)

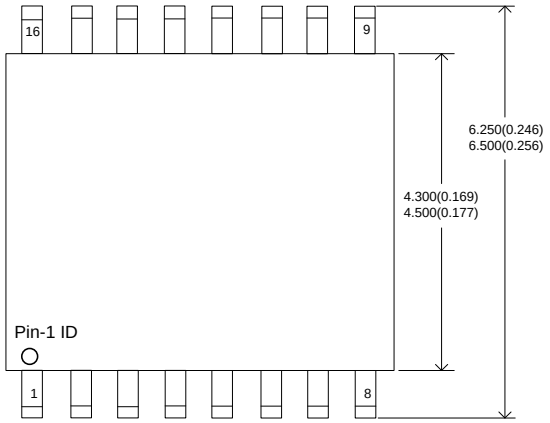
Recommended External Pullable Crystal Specifications (VCXO Version)

Parameter	Description	Min	Typ	Max	Unit	Comments
FNOM	Nominal Crystal Frequency Range	13	27	30	MHz	Fundamental Mode – AT Cut
CL	Nominal Crystal Load	11.4	12	12.6	pF	Load for +/-0 ppm Fo resonance value
R1-1	Equivalent Series Resistance	12.5	25	60	Ohm	F-Range: 13.0 to 19.999 MHz
R1-2	Equivalent Series Resistance	10	20	50	Ohm	F-Range: 20.0 to 30.000 MHz
DL1-2	Crystal Drive Level	-	-	200	µW	F-Range: 13.000 to 19.999 MHz
DL1-2	Crystal Drive Level	-	-	150	µW	F-Range: 20.000 to 30.000 MHz
Co-1	Shunt Capacitance	-	4	5.4	pF	SMD Xtals
Co-2	Shunt Capacitance	-	5	7.2	pF	Through Hole (Leaded) Xtals

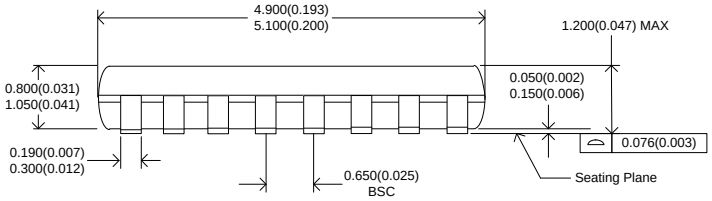
Table 4. Crystal Specifications (VCXO Version)

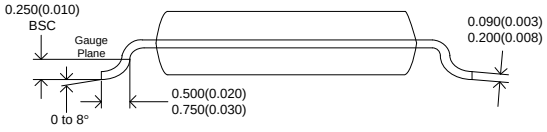
Package Outline and Package Dimensions

16-Pin TSSOP Package (4.4mm)



Dimensions are in milimeters (inches)
Top line: (MIN) and Bottom line: (Max)





Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	**Still air**	-	80	-	°C/W
	θ JA	**1m/s air flow**	-	70	-	°C/W
	θ JA	**3m/s air flow**	-	68	-	°C/W
Thermal Resistance Junction to Case	θ JC	**Independent of air flow**	-	36	-	°C/W

Ordering Information [1]

Ordering Number [2]	Marking	Shipping Package	Package	Temperature
SL38160ZC-XXX	SL38160ZC-XXX	Tube	16-pin TSSOP	0 to 70°C
SL38160ZC-XXXT	SL38160ZC-XXXT	Tape and Reel	16-pin TSSOP	0 to 70°C
SL38160ZI-XXX	SL38160ZI-XXX	Tube	16-pin TSSOP	-40 to 85°C
SL38160ZI-XXXT	SL38160ZI-XXXT	Tape and Reel	16-pin TSSOP	-40 to 85°C

Notes:

1. All SLI products are RoHS compliant.
2. “XXX” is “Dash” number and will be assigned by SLI for final programmed samples and production units based on customer programming requirements.