ADVANCE DATA SHEET

SKY77176 AutoSmart™ Dual-Band Power Amplifier Module for CDMA/PCS (824–849 MHz and 1850–1910 MHz)

Applications

- Digital cellular (CDMA)
- Personal Communications Services (PCS)
- Wireless local loop (WLL)

Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V
- Low V_{REF}
  - 2.85 V, nominal
- Low I_{REF}
  - less than 1 mA
- Good linearity
- High efficiency
- Large dynamic range
- 12-pin package
  - 3 mm x 5 mm x 1.0 mm
- Power down control
- InGaP
- IS95/CDMA2000/EVDO

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Description

The SKY77176 AutoSmart™ Power Amplifier Module (PAM) is a fully matched, 12-pin surface mount module developed for Code Division Multiple Access (CDMA) / Personal Communications Services (PCS) and Wireless Local Loop (WLL) applications.

AutoSmart™ power amplifier technology internally adjusts the RF transistor bias level throughout the dynamic operating range to minimize battery current consumption and ensure sufficient linear performance to meet CDMA system requirements. The result is a significant savings in average battery current without the complications of a system-supplied mode function signal or analog bias control. AutoSmart™ response time is more than adequate for RF access probe and discontinuous transmission operation. Mode control is included to permit high-bias operation (disable AutoSmart™) during high data transmission using CDMA2000 or 1xEVDO.

This small and efficient module packs full coverage of the 824–849 MHz and 1850–1910 MHz bandwidths into a single compact package. The device meets the stringent IS95 CDMA linearity requirements up to and exceeding 28 dBm output power. The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. Output match to a 50-ohm load is realized off-chip and within the module package to optimize efficiency and power performance.

The SKY77176 AutoSmart™ PAM is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the SKY77176 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the 3.2 to 4.2 volt range. Power down is accomplished by setting the voltage on the low current reference pin to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

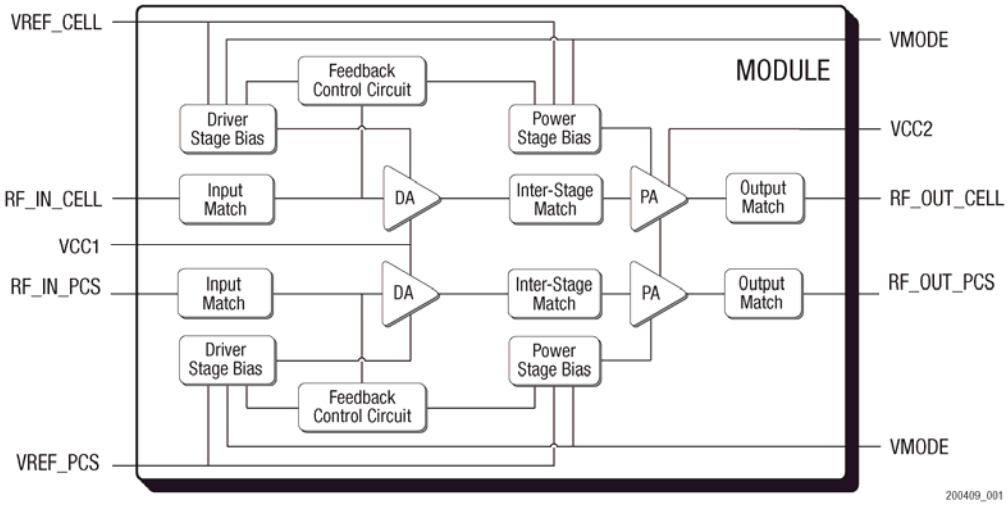


Figure 1. Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the SKY77176 Power Amplifier. Table 1 lists the absolute maximum ratings, while Table 2 lists the recommended operating conditions for achieving the electrical performance listed in Table 4 (CDMA Cellular) and Table 5 (CDMA PCS). Table 3 presents a truth table for disable and band selection.

Table 1. Absolute Maximum Ratings [1]

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
CW RF Input Power		P_{IN}	—	0.0	7.0	dBm
Supply Voltage		V_{CC}	—	3.4	6.0	Volts
Digital Control Voltage		V_{MODE}	0	2.5	3.0	Volts
Reference Voltage		V_{REF}	—	2.85	3.0	Volts
Case Temperature [2]	Operating	T_C	–30	25	+110	°C
	Storage	T_{STG}	–55	—	+125	

1 No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

2 Case Operating Temperature refers to the temperature of the GROUND PAD at the underside of the package.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Output Power	CDMA Cell	P_O	—	—	28.0	dBm
	CDMA PCS		—	—	28.5	
Operating Frequency	CDMA Cell	F_O	824.0	836.5	849.0	MHz
	CDMA PCS		1850.0	1880.0	1910.0	
Supply Voltage		V_{CC} [1]	3.2	3.4	4.2	Volts
		V_{MODE}	3.2	3.4	4.2	
V_{MODE} Control Range	Data Mode	V_{MODE}	—	0.0	0.5	Volts
	Autobias		2.5	3.0	—	
Reference Voltages		V_{REF_CELL} V_{REF_PCS}	2.75	2.85	2.95	Volts
Case Operating Temperature		T_O	–30	+25	+85	°C

1 Recommended minimum V_{CC} for maximum output power is indicated. V_{CC} down to 0.5 V may be used for backed-off output when using DC/DC converter to conserve battery current.

Table 3. Band Select Truth Table

Band Selection	V_{REF_CELL}	V_{REF_PCS}
Cellular	2.85 V	0.0 V
PCS	0.0 V	2.85 V
Power Down (disable)	0.0 V	0.0 V

Table 4. Electrical Specifications for CDMA Cell Nominal Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain Conditions	Digital Mode	G_{LOW}	$P_{O\_D} \leq 0$ dBm	—	21.0	—	dB
		G_{HIGH}	$P_{O\_D} = 28$ dBm	—	28.0	—	
	Analog Mode	G_P	$P_{O\_A} = 31$ dBm	—	27.0	—	
Power Added Efficiency ($V_{CC} = 3.4$ V)	Digital Mode	PAE_{D_LOW}	$P_{O\_D} = 16$ dBm	—	9	—	%
		PAE_{D_HIGH}	$P_{O\_D} = 28$ dBm	—	40	—	
	Analog Mode	PAE_a	$P_{O\_A} = 31$ dBm	—	55	—	
Total Supply Current		I_{CC_LOW}	$P_{O\_D} = 16$ dBm	—	130	—	mA
		I_{CC_HIGH}	$P_{O\_D} = 28$ dBm	—	450	—	
Total Supply Current in Power-down Mode		I_{PD}	$V_{CC} = 3.4$ V $V_{REF} = 0$ V	—	2.0	—	µA
Quiescent Current		I_{CQ}		—	20	—	mA
Reference Current		I_{REF}		—	1.0	—	mA
Adjacent Channel Power [2,3]	885 kHz offset	ACP1	$P_{O\_D} \leq 28$ dBm	—	–49	—	dBc
	1.98 MHz offset	ACP2		—	–60	—	
Harmonic Suppression	Second	fo2	$P_{O\_D} \leq 31$ dBm	—	–35	—	dBc
	Third	fo3		—	–55	—	
Noise Power in RX Band 869-894 MHz		RxBN	$P_{O\_D} \leq 28$ dBm	—	–139	—	dBm/Hz
Noise Figure		NF		—	4.0	—	dB
Input Voltage Standing Wave Ratio		VSWR		—		2.0:1	
Stability (Spurious output)		S	5:1 VSWR all phases	—	—	–70.0	dBc
Ruggedness—No damage [4]		Ru	$P_{O\_D} \leq 28$ dBm	10:1	—	—	VSWR
Turn On Time [5]	DC	$T_{ON}DC$		—	40	—	µs
	RF	$T_{ON}RF$		—	5	—	
Turn Off Time [5]	DC	$T_{OFF}DC$		—	40	—	µs
	RF	$T_{OFF}RF$		—	5	—	

[1] Per Table 2 over dynamic range up to 28 dBm output power, unless otherwise specified.

[2] ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

[3] For CDMA2000 test configured as [PCH @ –3.75 dB, DCCH–9600 bps @ 0 dB; SCHO–9600 bps @ 0 dB] and other test configurations that yield a peak-to-average up to 4.5 dB for CCDF = 1%, up to 1. dB power back off from the maximum listed for IS95 may be required to meet specified maximum ACP performance under worst-case conditions.

[4] All phases, time = 10 seconds.

[5] $T_{ON}DC$ is time required to reach stable quiescent bias (±10%) after V_{REF} is switched high.
$T_{OFF}DC$ is time required for battery to decrease to < 100 µA after V_{REF} is switched low.
After I_{CQ} is stable, The $T_{ON}RF$ is time to reach final output power (±1 dB) once RF input is applied.
$T_{OFF}RF$ is time required for P_O to drop 30 dB once RF input is removed.

Table 5. Electrical Specifications for CDMA PCS Nominal Operating Conditions [1]

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain Conditions		G_{LOW}	$P_O \leq 0$ dBm	—	23.0	—	dB
		G_{HIGH}	$P_O = 28$ dBm	—	28.0	—	
Power Added Efficiency ($V_{CC} = 3.4$ V)		PAE_{D_LOW}	$P_O = 16$ dBm	—	10	—	%
		PAE_{D_HIGH}	$P_O = 28$ dBm	—	40	—	
Total Supply Current		I_{CC_LOW}	$P_O = 16$ dBm	—	120	—	mA
		I_{CC_HIGH}	$P_O = 28$ dBm	—	470	—	
Total Supply Current in Power-down Mode		I_{PD}	$V_{CC} = 3.4$ V $V_{REF} = 0$ V	—	2.0	—	µA
Quiescent Current		I_{CQ}		—	20	—	mA
Reference Current		I_{REF}		—	1.0	—	mA
Adjacent Channel Power	1.25 MHz offset	ACP1	—	—	–50	—	dBc
	1.98 MHz offset	ACP2	—	—	–55	—	
Harmonic Suppression	Second	fo2	$P_O \leq 28$ dBm	—	–55	—	dBc
	Third	fo3		—	–45	—	
Noise Power in RX Band 1930-1990 MHz		RxBN	$P_O \leq 28$ dBm	—	–139	—	dBm/Hz
Noise Figure		NF		—	4.0	—	dB
Input Voltage Standing Wave Ratio		VSWR		—		2.0:1	
Stability (Spurious output)		S	5:1 VSWR all phases	—	—	–70.0	dBc
Ruggedness—No damage [2]		Ru	$P_O \leq 28$ dBm	10:1	—	—	VSWR
Turn On Time [3]	DC	$T_{ON}DC$	—	—	40	—	µs
	RF	$T_{ON}RF$	—	—	5	—	
Turn Off Time [3]	DC	$T_{OFF}DC$	—	—	40	—	µs
	RF	$T_{OFF}RF$	—	—	5	—	

[1] Per Table 2 over dynamic range up to 28 dBm output power, unless otherwise specified.

[2] All phases, time = 10 seconds.

[3] $T_{ON}DC$ is time required to reach stable quiescent bias (±10%) after V_{REF} is switched high.
$T_{OFF}DC$ is time required for battery to decrease to < 100 µA after V_{REF} is switched low.
After I_{CQ} is stable, The $T_{ON}RF$ is time to reach final output power (±1 dB) once RF input is applied.
$T_{OFF}RF$ is time required for P_O to drop 30 dB once RF input is removed.

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the SKY77176, the evaluation board schematic and evaluation board assembly diagram are included for preliminary analysis and design. Figure 2 shows the basic schematic diagram of the Evaluation Board Assembly for the 824 to 849 MHz and the 1850 to 1910 MHz ranges shown in Figure 3.

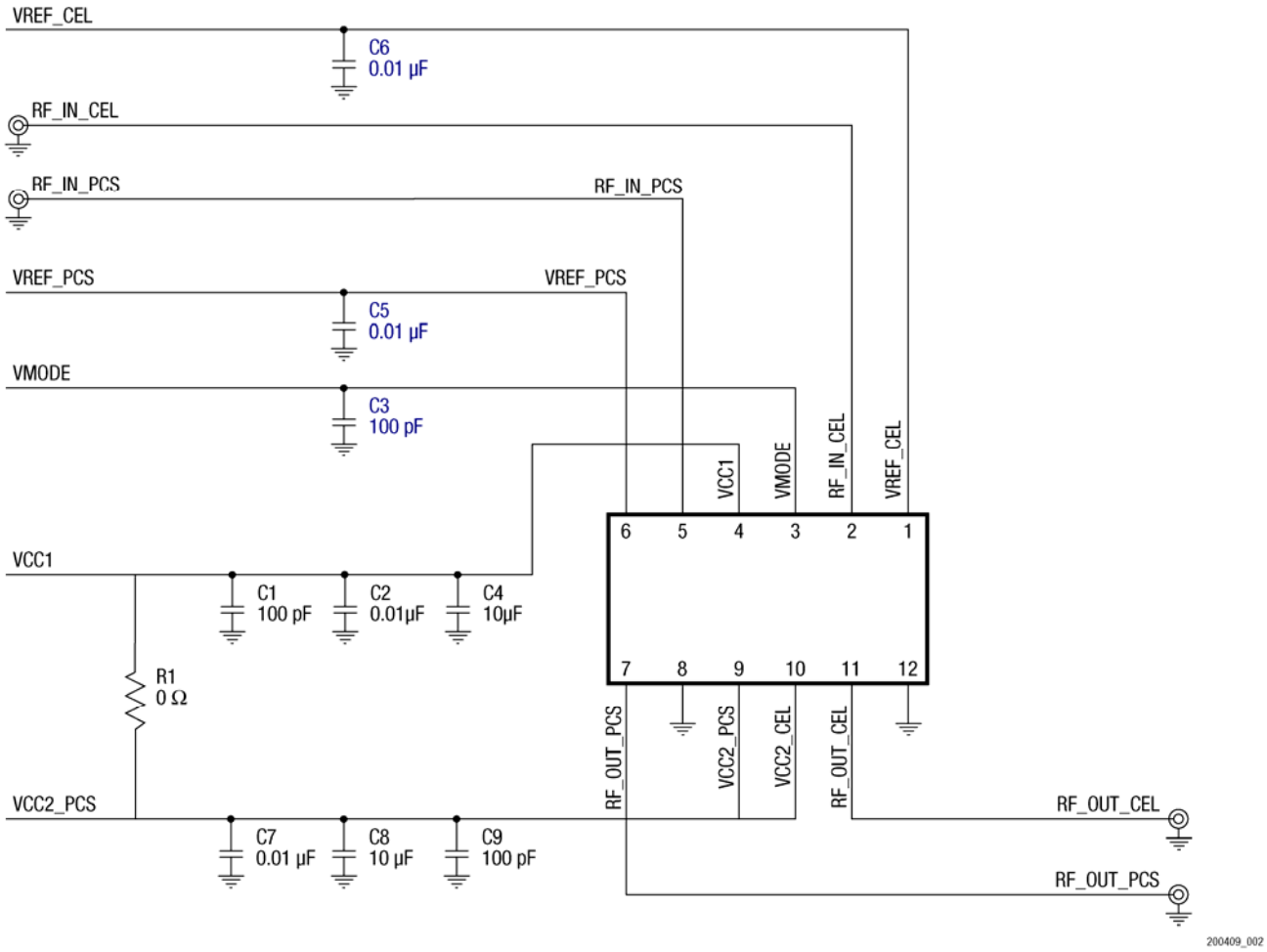
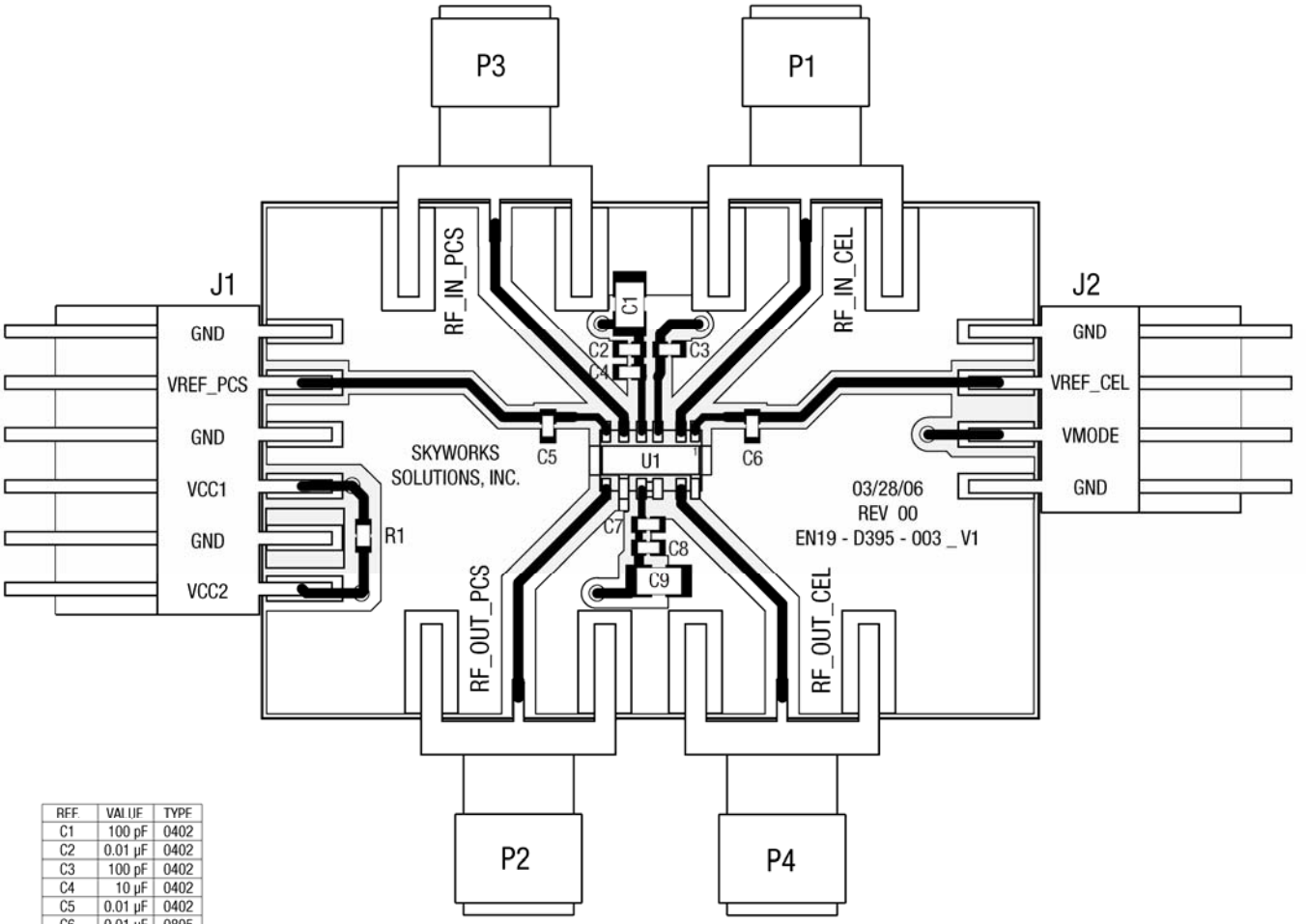


Figure 2. Evaluation Board Schematic



REF	VALUE	TYPE
C1	100 pF	0402
C2	0.01 µF	0402
C3	100 pF	0402
C4	10 µF	0402
C5	0.01 µF	0402
C6	0.01 µF	0805
C7	0.01 µF	0402
C8	10 µF	0402
C9	100 pF	0805
R1	0 Ω	0402

Figure 3. Evaluation Board Assembly Diagram

Package Dimensions and Pad Descriptions

The SKY77176 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 4 is a mechanical drawing of the pin layout for this package. Figure 5 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals. Figure 6 shows the pin names and the pin numbering convention, which starts with pin 1 in the upper left and increments counter-clockwise around the package. Figure 7 illustrates typical case markings.

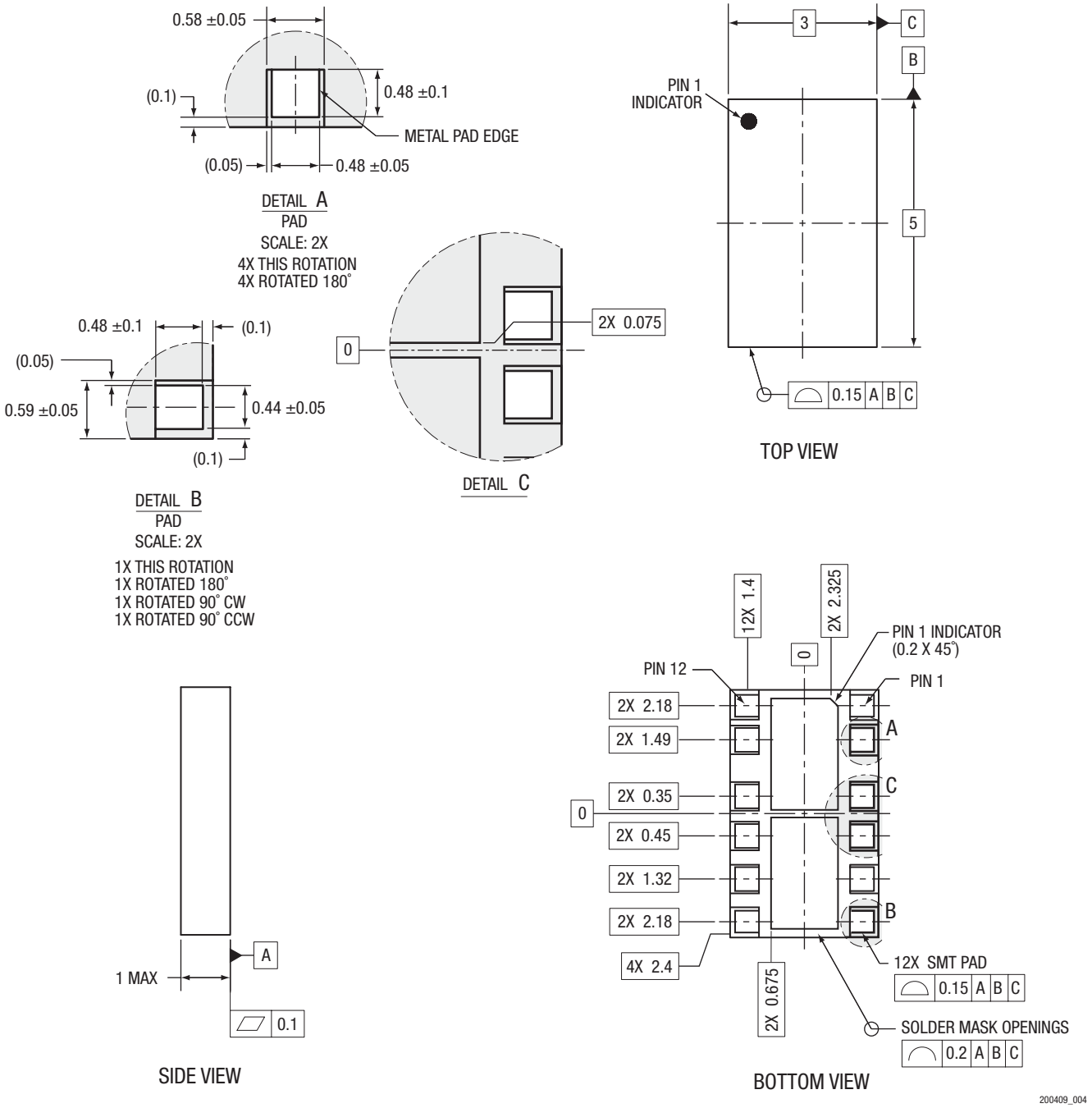
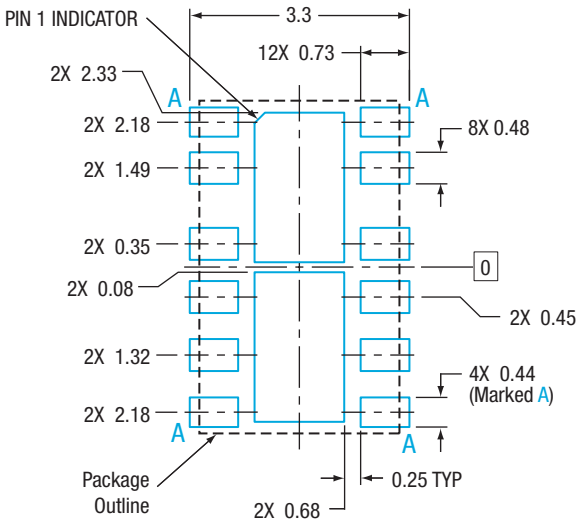
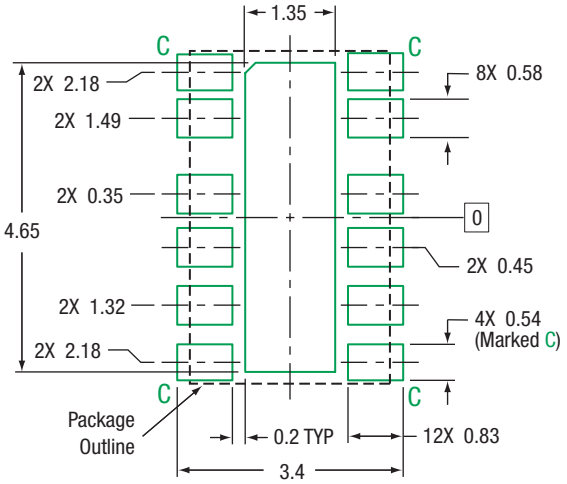


Figure 4. SKY77176 Package Dimensional Drawing (All Views)

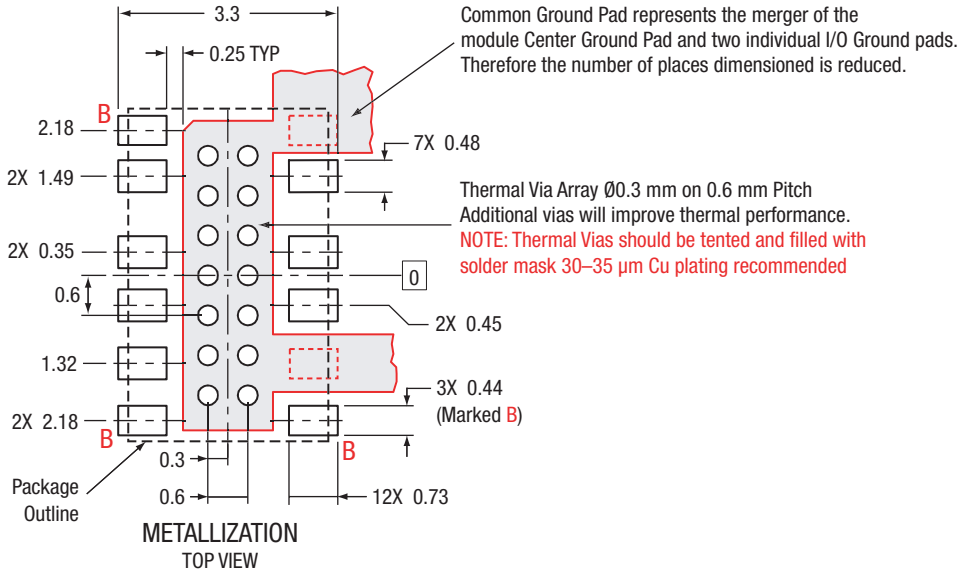


STENCIL APERTURE
TOP VIEW

Stencil aperture size for Center Ground Pad should be 80%-100% (by area) of the Solder Mask Opening package.



SOLDER MASK OPENING
TOP VIEW



METALLIZATION
TOP VIEW

All dimensions are in millimeters.

200409_005

Figure 5. Phone PCB Layout Footprint for 3 x 5, 12-Pad Package – SKY77176

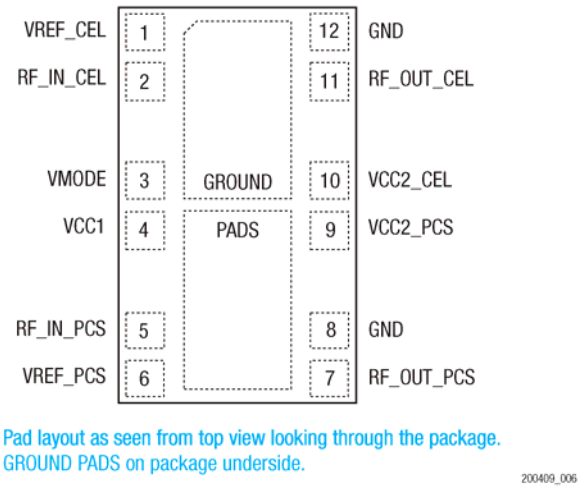


Figure 6. SKY77176 Pad Configuration and Pad Names (Top View)

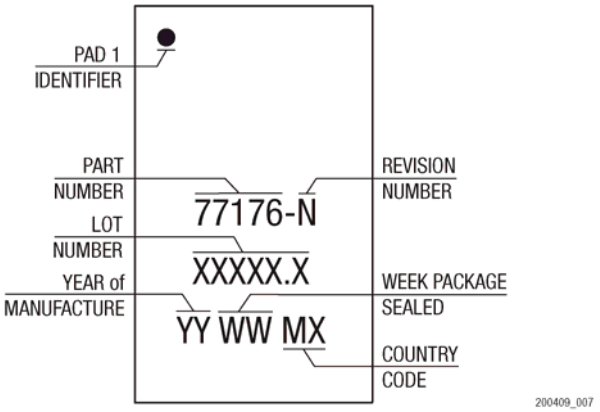


Figure 7. Typical Case Markings

Package and Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77176 is capable of withstanding an MSL3/250 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second; maximum temperature should not exceed 250 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 250 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks Application Note: *PCB Design and SMT Assembly/Rework*, Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020*.

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to Skyworks Application Note: *Tape and Reel Information – RF Modules*, Document Number 101568.

Electrostatic Discharge Sensitivity

The SKY77176 is a Class 1C device. Figure 8 lists the Electrostatic Discharge (ESD) immunity level for each pin of the SKY77176 product. The numbers in Figure 8 specify the ESD threshold level for each pin where the I-V curve between the pin and ground starts to show degradation.

The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pin, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

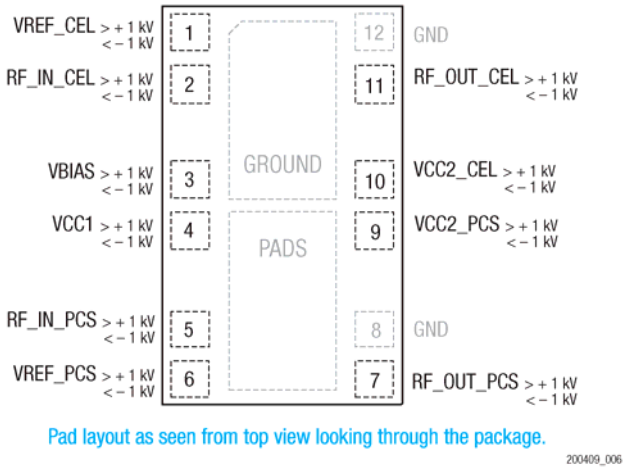


Figure 8. SKY77176 ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after “the pin fails the electrical specification limits” or “the pin becomes completely non-functional”. Skyworks employs most stringent criteria and fails devices as soon as the pin begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed below.

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Antistatic ID Badges
- Protective Workstation
  - Dissipative Table Top
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Solder Conductive Suckers
  - Static Sensors
- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than 10^9 Ω to GND)
- Protective Packaging and Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders

Ordering Information

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
SKY77176	SKY77176			–30 °C to +85 °C

Revision History

Revision	Level	Date	Description
A		November 17, 2007	Initial Issue – Preliminary Information

References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Application Note: Tape and Reel Information – RF Modules Document Number 101568

JEDEC Standard J–STD–020