KODENSHI AUK

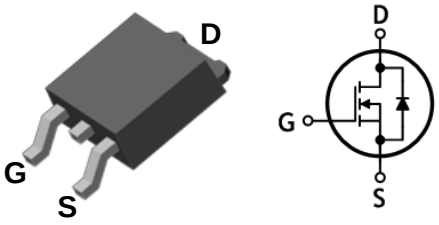
SJMN380R65D

Super Junction MOSFET

N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: V_{DS}=700V (@T_J=150°C)
- Low drain-source On resistance: $R_{DS(on)}$=0.38Ω (Max.)
- Ultra low gate charge: Qg=20nC(Typ.)
- RoHS compliant device
- 100% avalanche tested

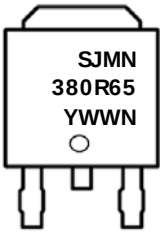


TO-252

Ordering Information

Part Number	Marking	Package
SJMN380R65D	SJMN380R65	TO-252

Marking Information



Column 1, 2: Device Code
Column 3: Production Information
e.g.) YWWN
-. YWW: Date Code (year, week)
-. N: Management Code

Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		650	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) (Note 1)	I_D	T_c=25°C	11	A
		T_c=100°C	7	A
Drain current (Pulsed) (Note 1)	I_{DM}		44	A
Single pulsed avalanche energy (Note 2)	E_{AS}		135	mJ
Repetitive avalanche current (Note 1)	I_{AR}		5	A
Repetitive avalanche energy (Note 1)	E_{AR}		7.6	mJ
Power dissipation	P_D		76	W
Diode dv/dt ruggedness (Note 3)	dv/dt		15	V/ns
MOSFET dv/dt ruggedness (Note 4)	dv/dt		50	V/ns
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.64	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	2	3	4	V
Drain-source cut-off current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	uA
		V_{DS}=650V, T_J=125°C	-	-	100	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=5.5A	-	0.31	0.38	Ω
Internal gate resistance	R_g	f=1MHz, Open drain	-	21	-	Ω
Input capacitance	C_{iss}	V_{DS}=25V, V_{GS}=0V, f=1MHz	-	787	-	pF
Output capacitance	C_{oss}		-	431	-	
Reverse transfer capacitance	C_{rss}		-	24	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	V_{DS}=350V, I_D=11A, R_G=25Ω	-	17	-	ns
Rise time (Note 5)	t_r		-	14	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	40	-	
Fall time (Note 5)	t_f		-	5	-	
Total gate charge (Note 6)	Q_g	V_{DS}=400V, V_{GS}=10V, I_D=7A	-	20	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	6.5	-	
Gate-drain charge (Note 6)	Q_{gd}		-	5	-	

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	11	A
Source current (Pulsed)	I_{SM}		-	-	33	A
Forward voltage	V_{SD}	V_{GS}=0V, I_S=11A	-	-	1.2	V
Reverse recovery time (Note 5, 6)	t_{rr}	I_S=11A, V_{GS}=0V, dI_S/dt=100A/us	-	326	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	2.8	-	uC

Note:
1. Calculated continuous current based on maximum allowable junction temperature
2. L=10mH, I_{AS}=5A, V_{DD}=50V, Starting T_J=25°C
3. I_S≤11A, V_{DS}≤400V, dIs/dt≤100A/us, T_J=25°C
4. V_{DS}≤400V, I_S≤11A
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width≤300us, Duty cycle≤2%

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

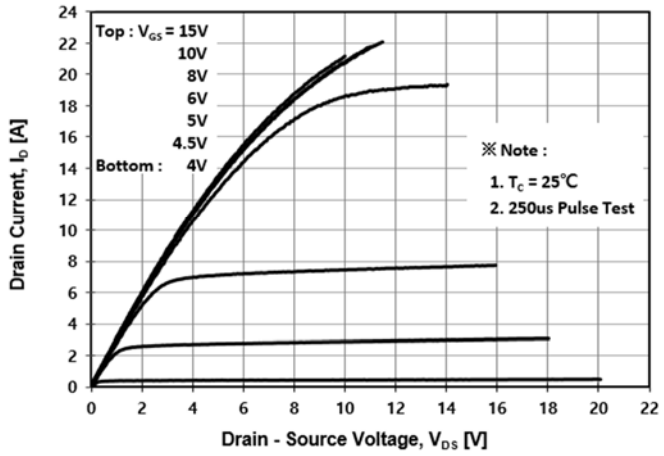


Fig. 2 Typical Transfer Characteristics

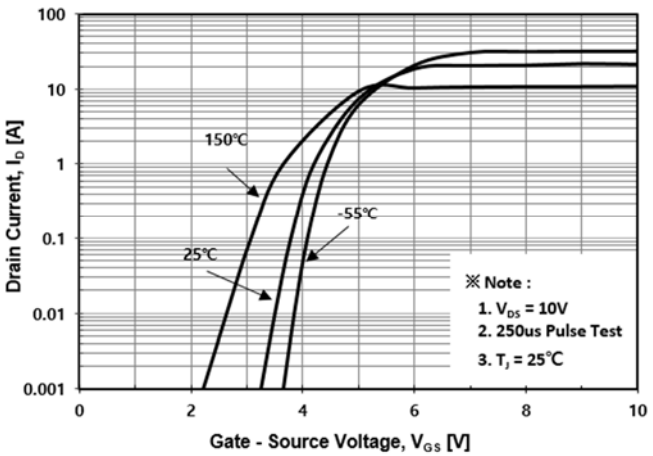


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

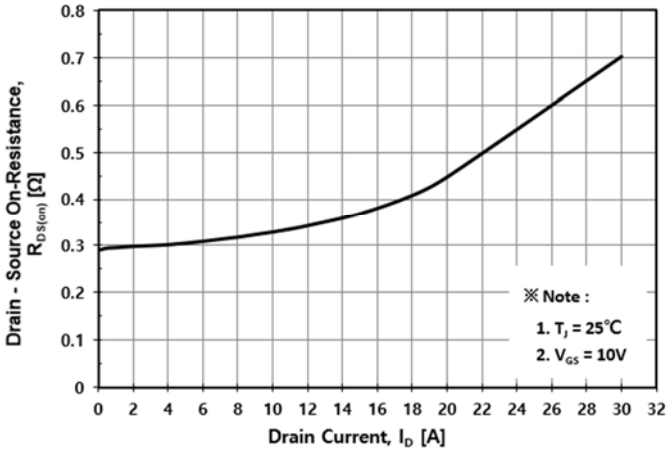


Fig. 4 Body Diode Forward Voltage Variation with Source Current

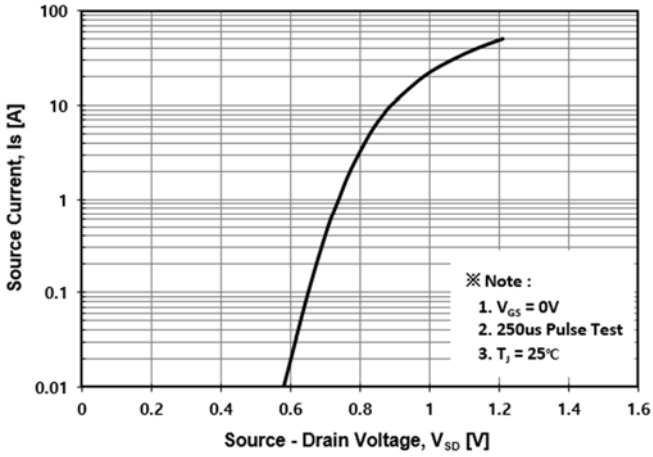


Fig. 5 Typical Capacitance Characteristics

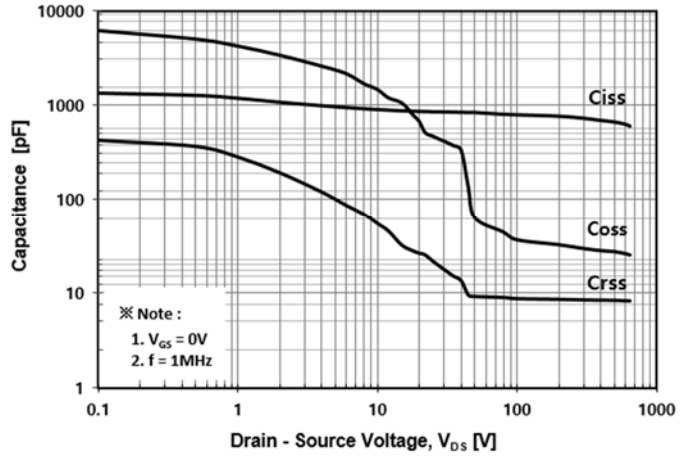


Fig. 6 Typical Total Gate Charge Characteristics

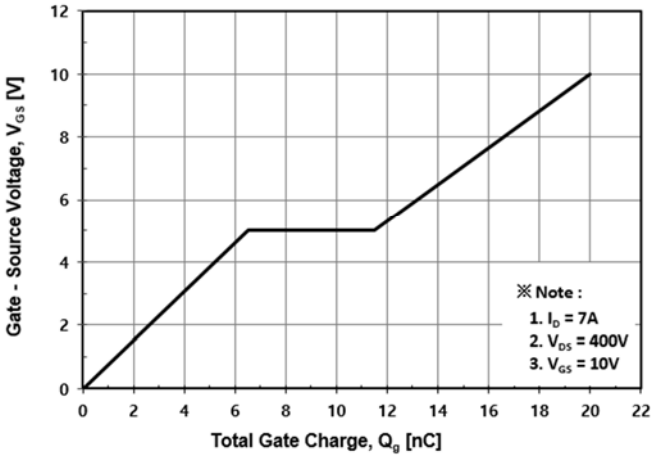


Fig. 7 Breakdown Voltage Variation vs. Temperature

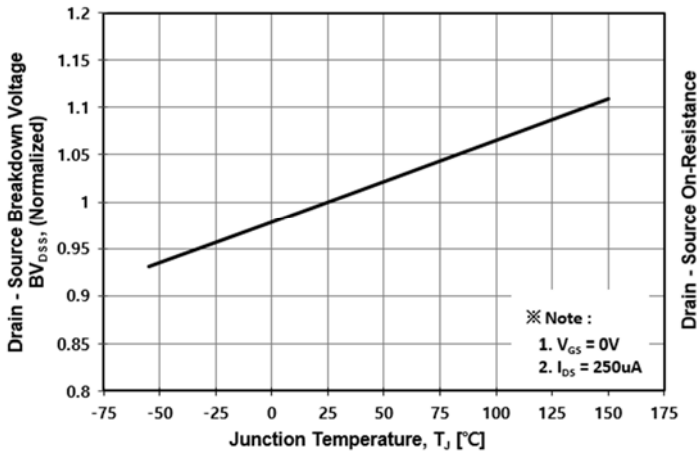


Fig. 8 On-Resistance Variation vs. Temperature

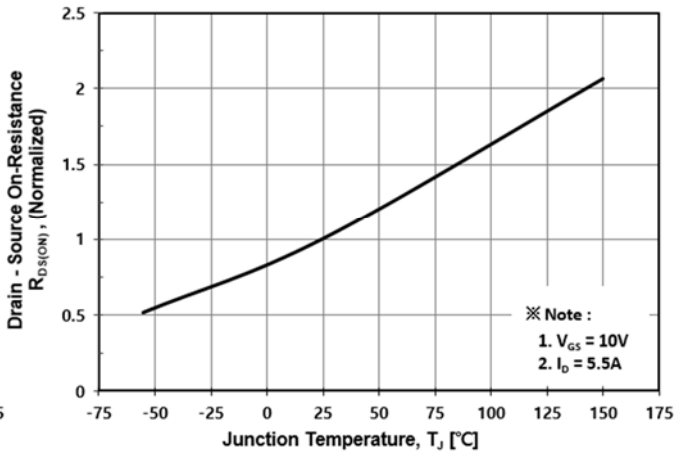


Fig. 9 Maximum Drain Current vs. Case Temperature

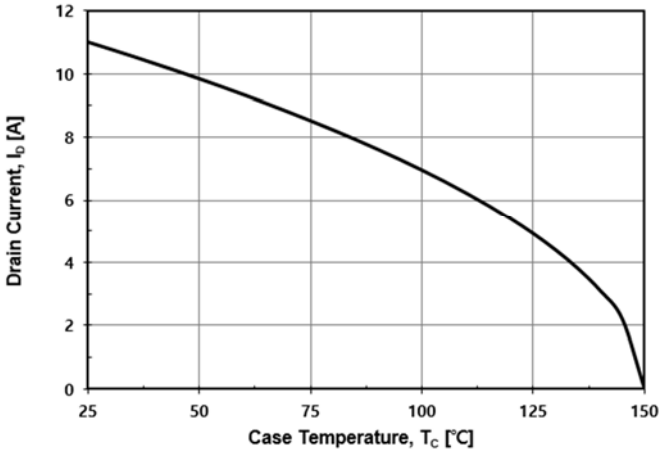


Fig. 10 Maximum Safe Operating Area

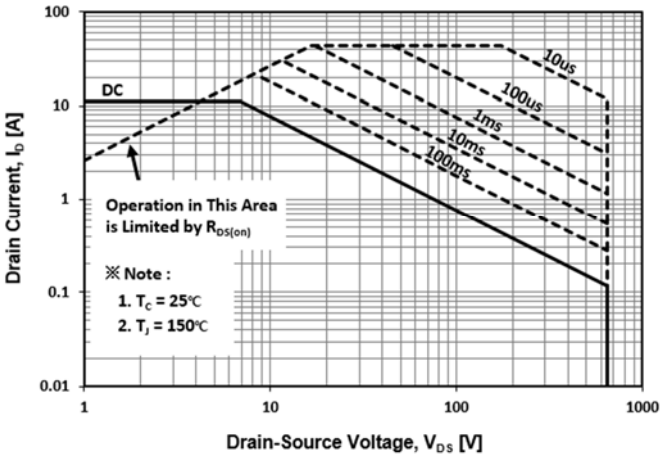


Fig. 11 Transient Thermal Impedance

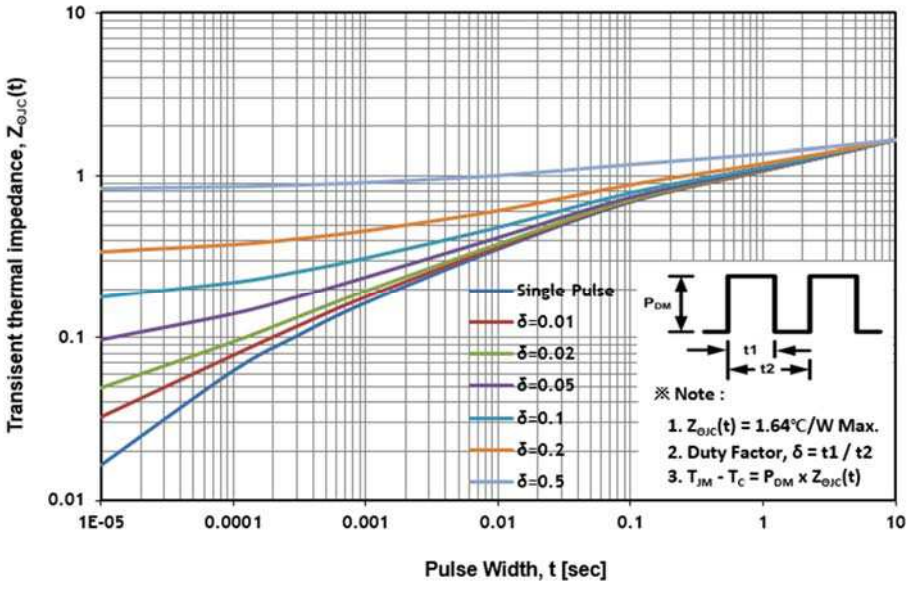
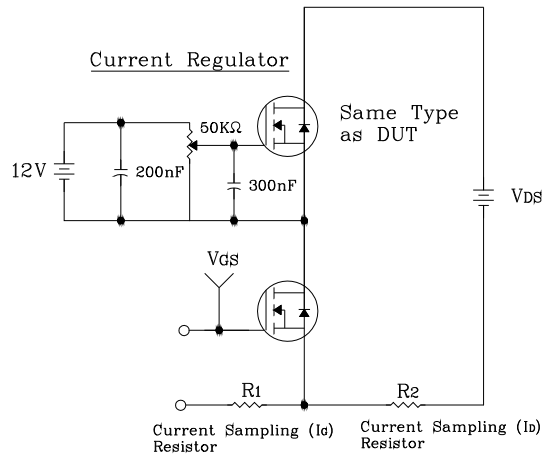


Fig. 12 Gate Charge Test Circuit & Waveform



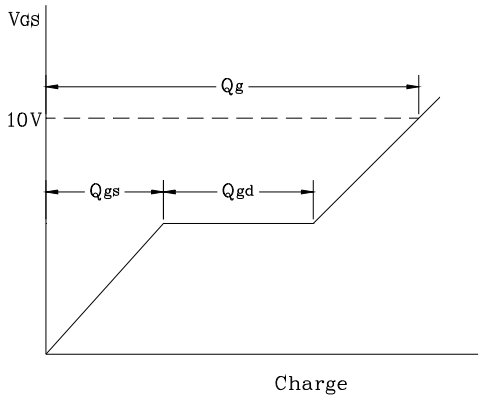
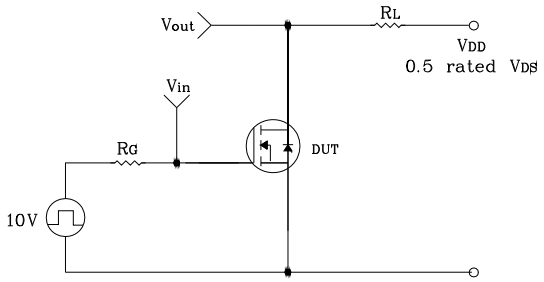


Fig. 13 Resistive Switching Test Circuit & Waveform



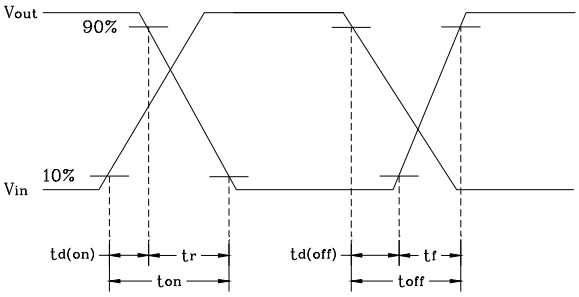
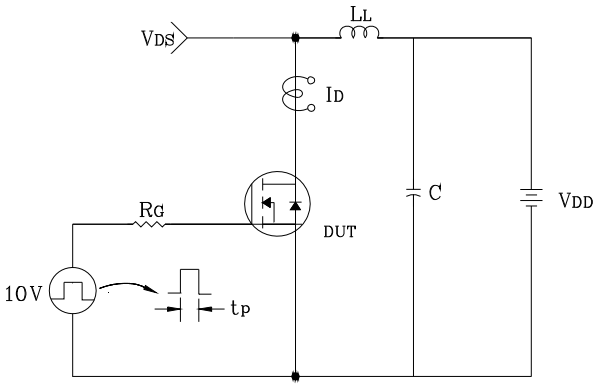


Fig. 14 E_{AS} Test Circuit & Waveform



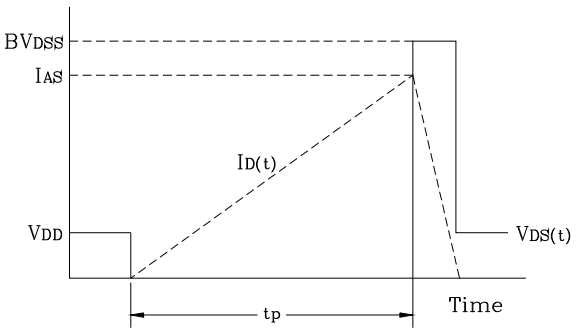
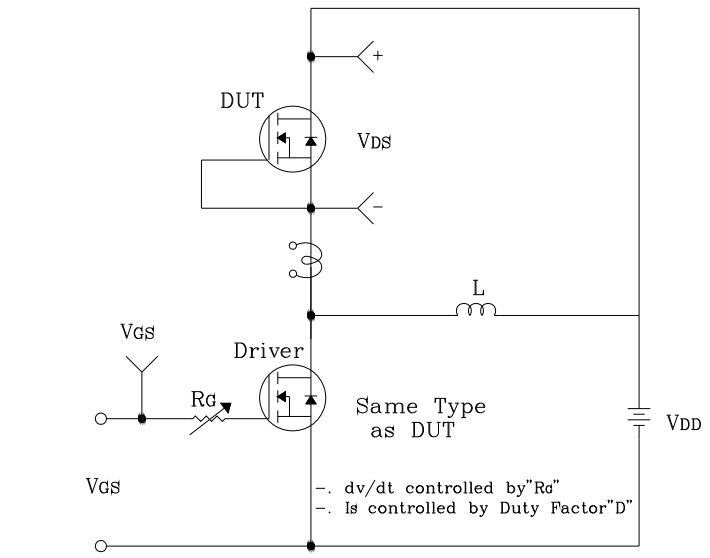
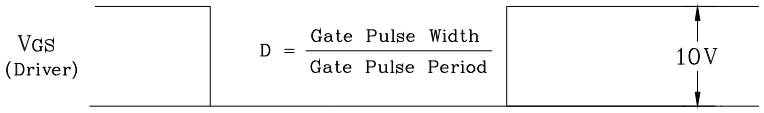
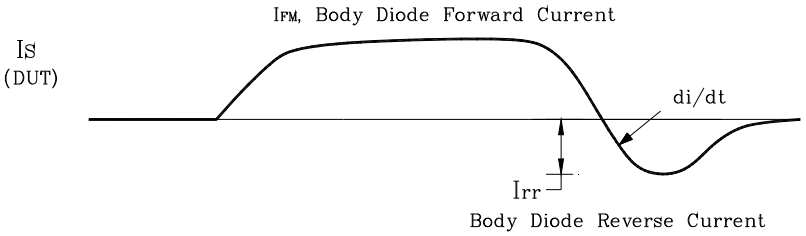
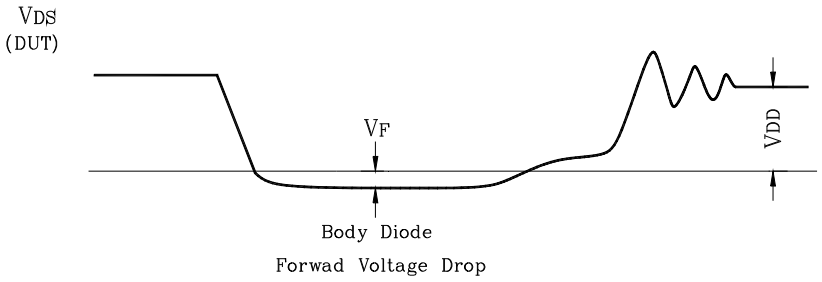


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

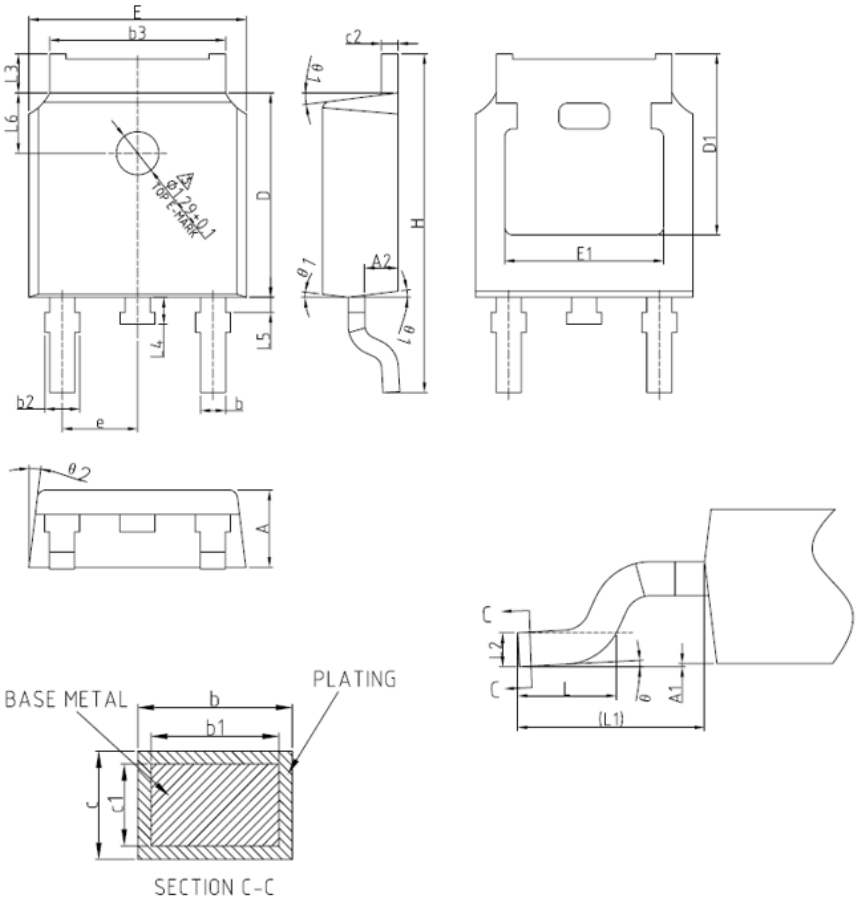








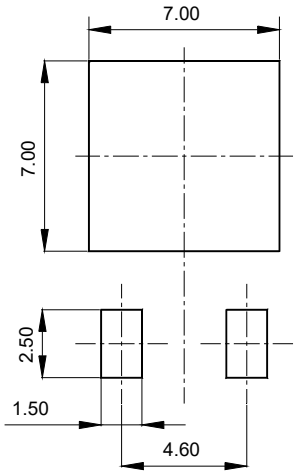
Package Outline Dimensions



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	2.20	2.30	2.38
	A1	0	–	0.10
⚠	A2	0.90	1.01	1.10
	b	0.72	–	0.85
	b1	0.71	0.76	0.81
	b2	0.72	–	0.90
	b3	5.13	5.33	5.46
	c	0.47	–	0.60
	c1	0.46	0.51	0.56
	c2	0.47	–	0.60
	D	6.00	6.10	6.20
	D1	5.25	–	–
	E	6.50	6.60	6.70
	E1	4.70	–	–
	e	2.186	2.286	2.386
	H	9.80	10.10	10.40
	L	1.40	1.50	1.70
	L1	2.90REF		
	L2	0.51BSC		
	L3	0.90	–	1.25
	L4	0.60	0.80	1.00
	L5	0.15	–	0.75
	L6	1.80REF		
	θ	0°	–	8°
⚠	θ 1	5°	7°	9°
⚠	θ 2	5°	7°	9°

Recommended Land Pattern [unit: mm]



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