

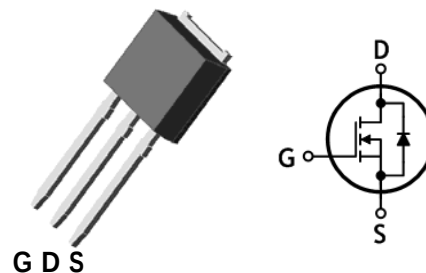
N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=650V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.34\Omega$ (Typ.)
- Low input capacitance and gate charge
- RoHS compliant device
- 100% avalanche tested

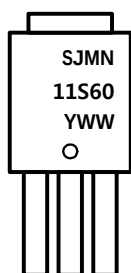
Ordering Information

Part Number	Marking	Package
SJMN11S60I	SJMN11S60	I-PAK



I-PAK

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 -. Y: Year Code
 -. WW : Week Code

Absolute maximum ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	600	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) (Note 1)	I_D	$T_C=25^{\circ}C$	11
		$T_C=100^{\circ}C$	7
Drain current (Pulsed) (Note 1)	I_{DM}	33	A
Single pulsed avalanche energy (Note 2)	E_{AS}	294	mJ
Avalanche current (Note 1)	I_{AS}	3.5	A
Power dissipation	P_D	83	W
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55-150	$^{\circ}C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.5	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62	

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2.5	-	4.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=480\text{V}$, $T_J=125^{\circ}\text{C}$	-	-	10	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.5\text{A}$	-	0.34	0.38	Ω
Gate resistance	R_g	$f=1\text{MHz}$, Open drain	-	4	-	Ω
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	628	-	pF
Output capacitance	C_{oss}		-	220	-	
Reverse transfer capacitance	C_{rss}		-	6.5	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DS}=400\text{V}$, $I_D=7\text{A}$, $R_G=25\Omega$	-	47	-	ns
Rise time (Note 3,4)	t_r		-	75	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	110	-	
Fall time (Note 3,4)	t_f		-	35	-	
Total gate charge (Note 3)	Q_g	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=11\text{A}$	-	11	15	nC
Gate-source charge (Note 3)	Q_{gs}		-	5	-	
Gate-drain charge (Note 3)	Q_{gd}		-	2.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	11	A
Source current (Pulsed)	I_{SM}		-	-	33	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=11\text{A}$	-	-	1.5	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=11\text{A}$, $V_{DD}=100\text{V}$, $V_{GS}=0\text{V}$ $di_S/dt=100\text{A}/\mu\text{s}$	-	400	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	3.6	-	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=40\text{mH}$, $I_{AS}=3.5\text{A}$, $V_{DD}=100\text{V}$, Starting $T_J=25^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Guaranteed by design, not subject to production testing

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

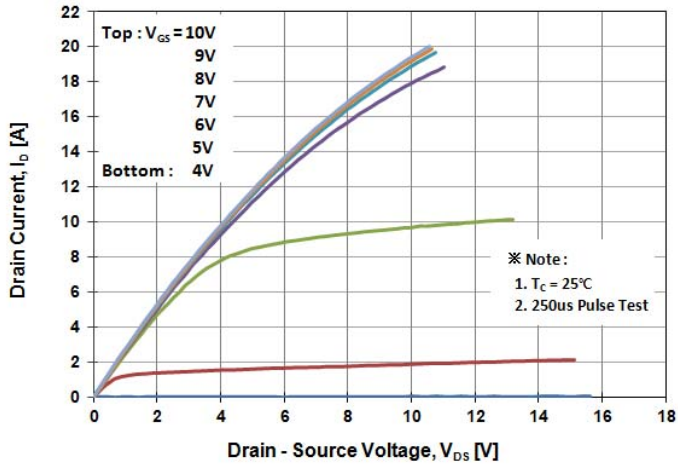


Fig. 2 Typical Output Characteristics

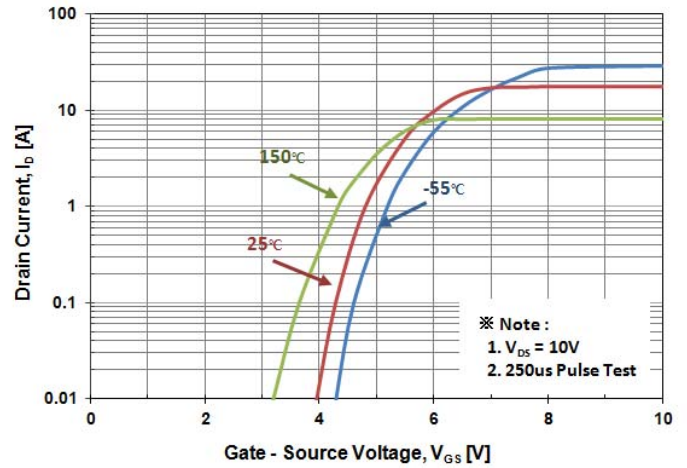


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

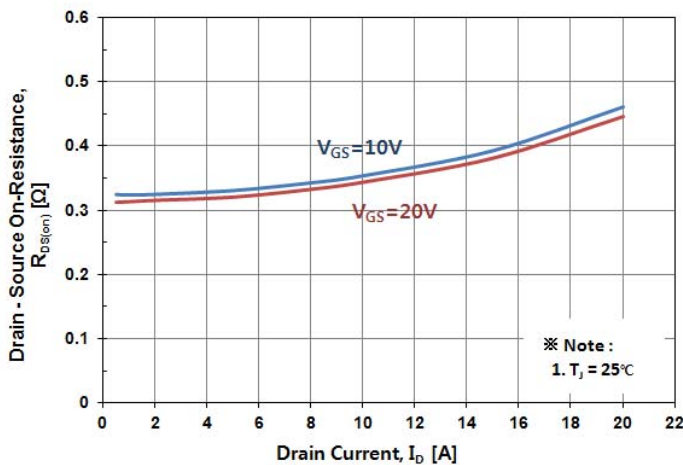


Fig. 4 Body Diode Forward Voltage Variation with Source Current

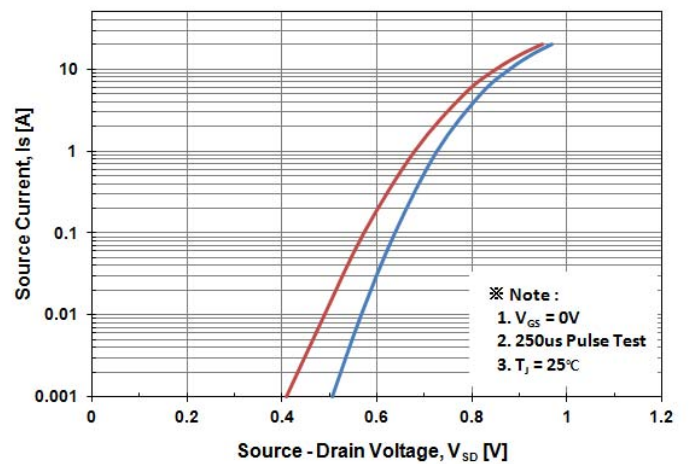


Fig. 5 Typical Capacitance Characteristics

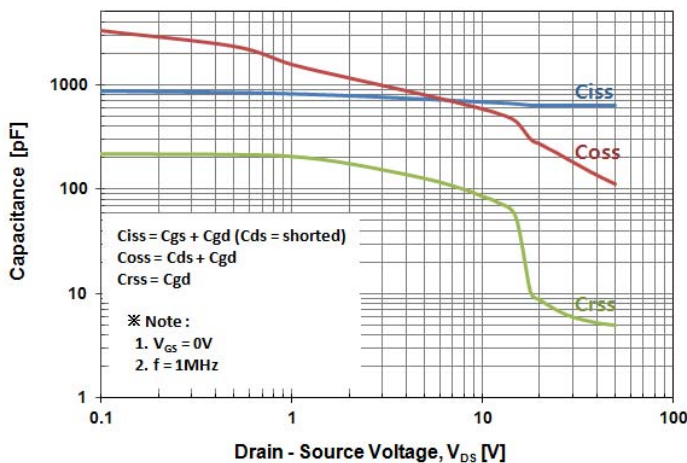


Fig. 6 Typical Total Gate Charge Characteristics

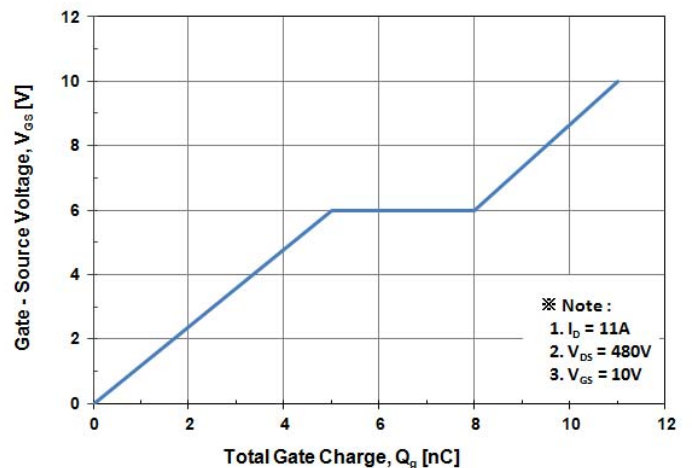


Fig. 7 Breakdown Voltage Variation vs. Temperature

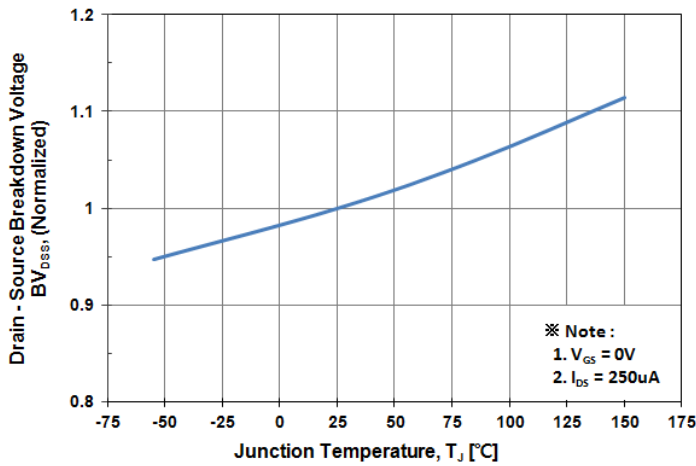


Fig. 8 On-Resistance Variation vs. Temperature

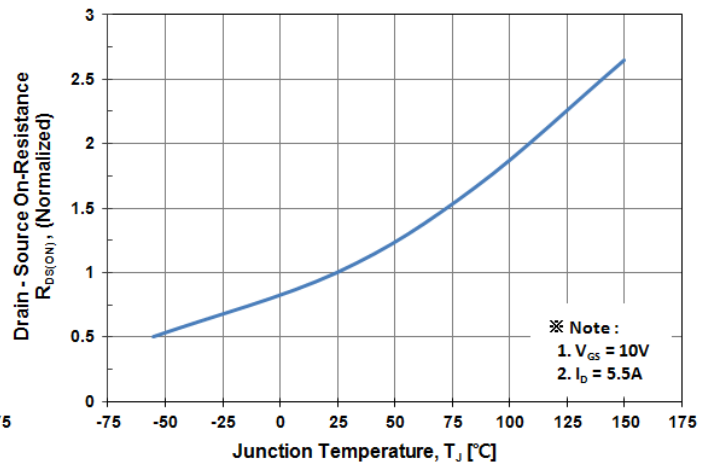


Fig. 9 Maximum Drain Current vs. Case Temperature

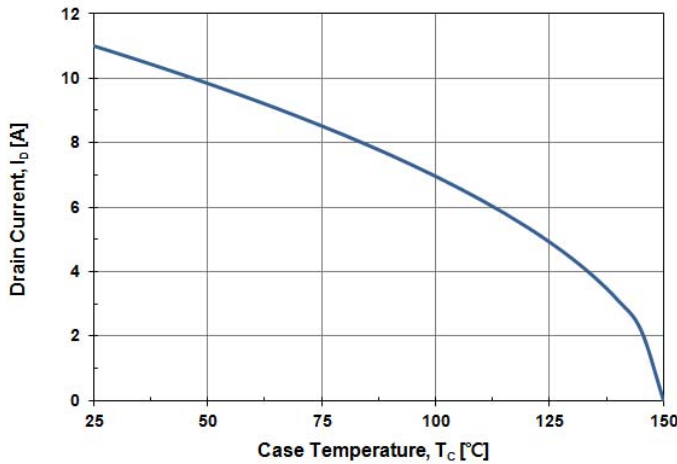


Fig. 10 Maximum Safe Operating Area

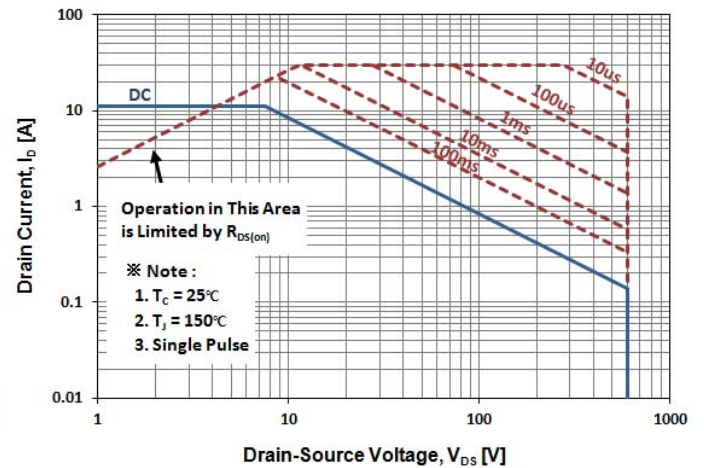


Fig. 11 Transient Thermal Impedance

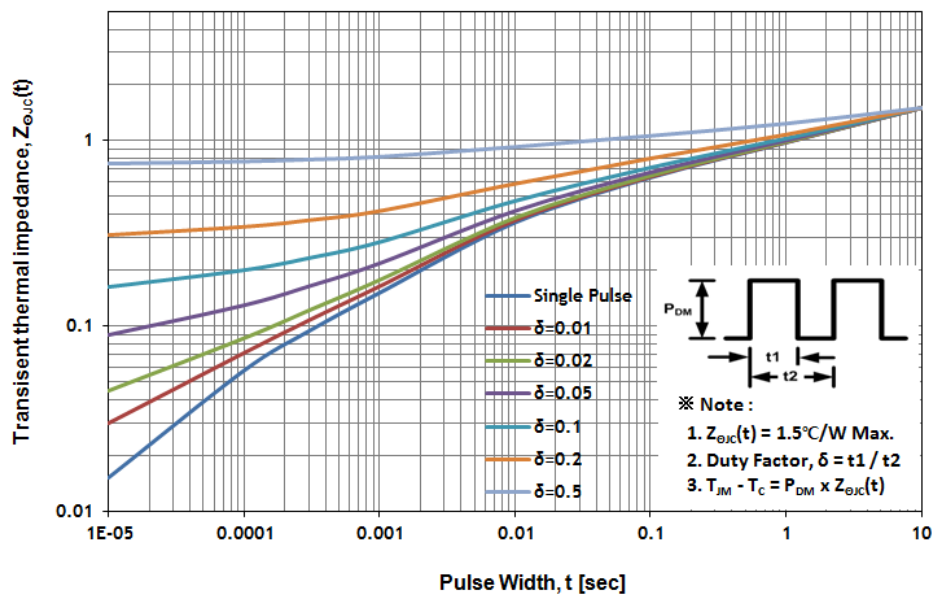


Fig. 12 Gate Charge Test Circuit & Waveform

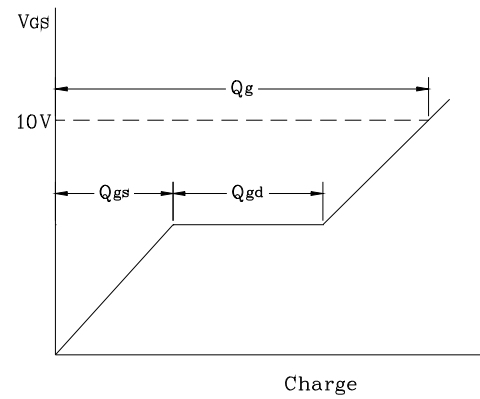
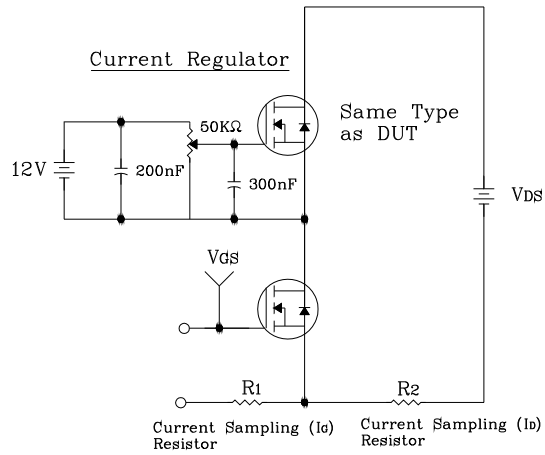


Fig. 13 Resistive Switching Test Circuit & Waveform

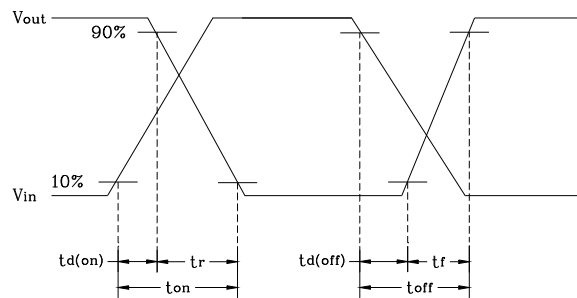
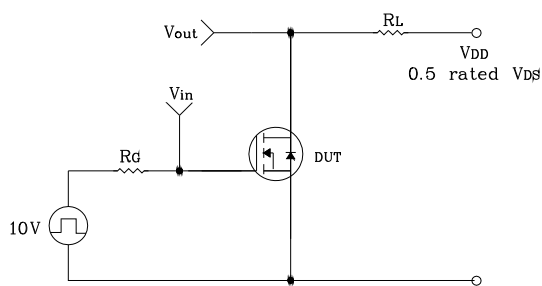


Fig. 14 E_{AS} Test Circuit & Waveform

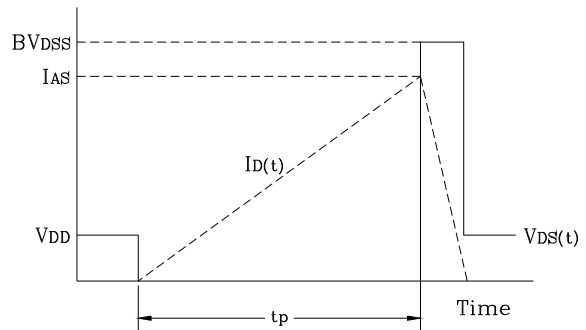
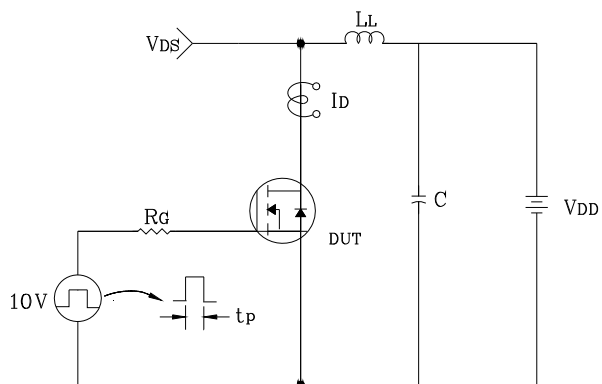
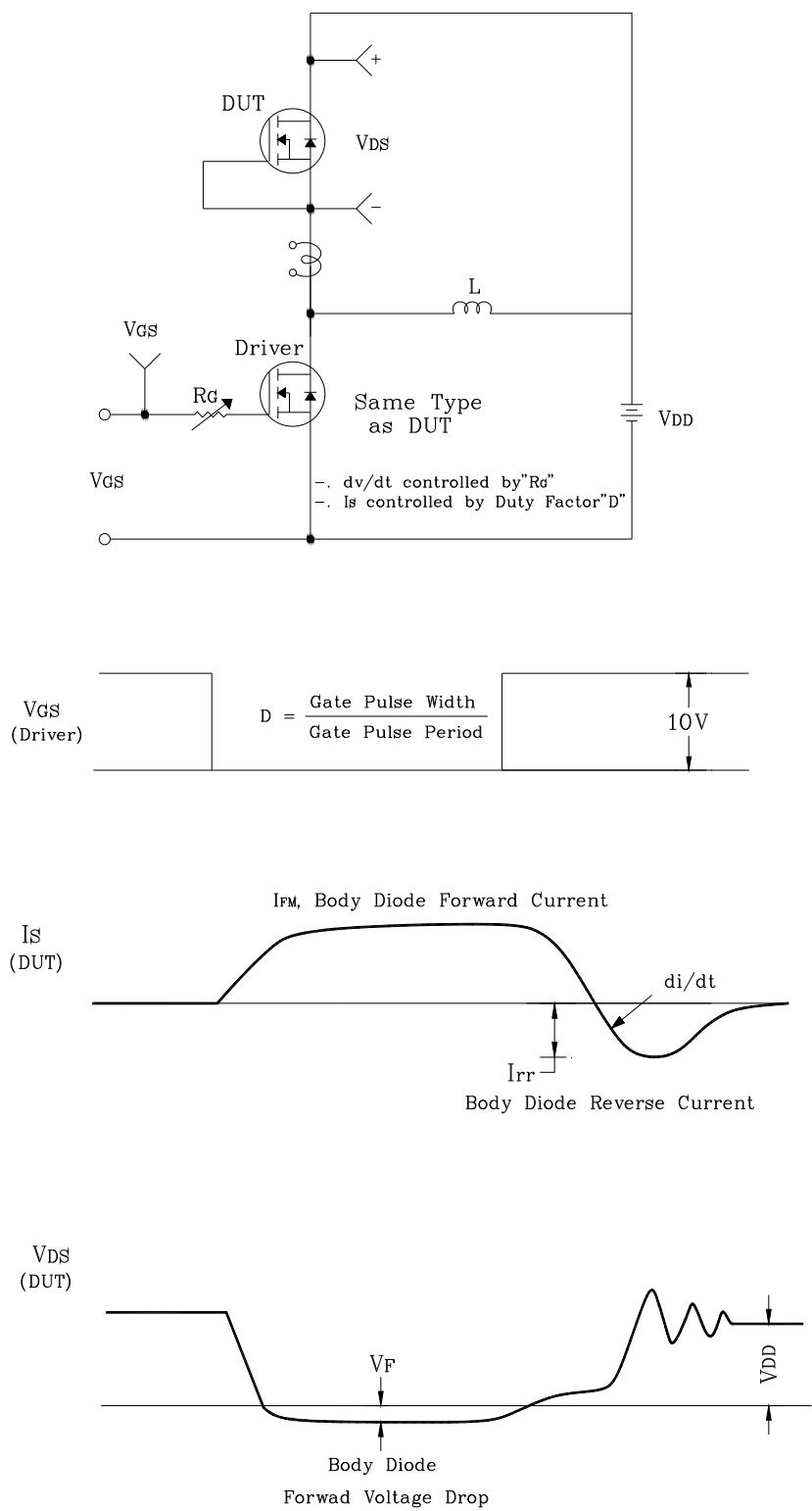
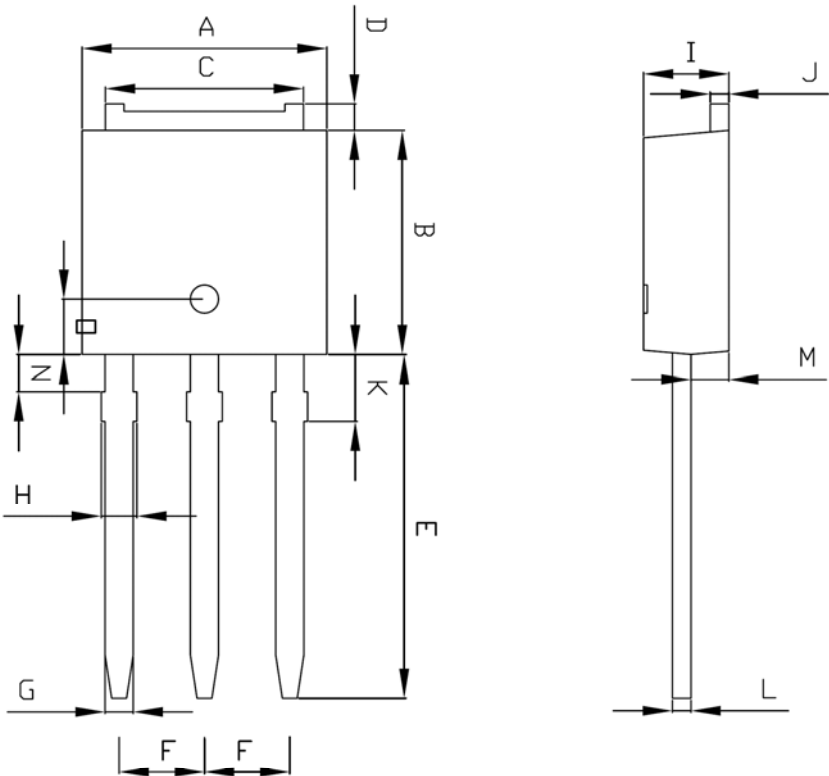


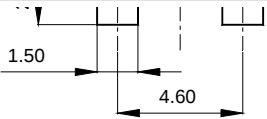
Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	6.40	6.60	6.80	
B	5.90	6.10	6.30	
C	5.04	5.34	5.64	
D	0.50	0.70	0.90	
E	9.00	9.30	9.60	
F	2.10	2.30	2.50	
G	0.66	0.76	0.86	
H	0.96 MAX			
I	2.20	2.30	2.40	
J	0.40	0.50	0.60	
K	1.60	1.80	2.00	
L	0.40	0.50	0.60	
M	0.72	1.02	1.32	
N	0.90	1.00	1.10	
O	1.50			



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