

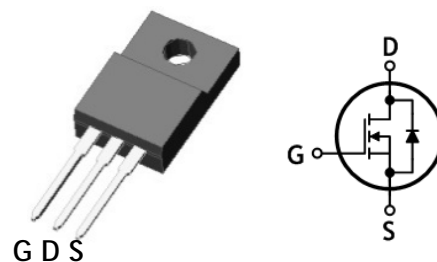
## N-Channel Super Junction MOSFET

### Features

- Drain- Source voltage:  $V_{DS}=700V$  (@ $T_J=150^{\circ}C$ )
- Low drain-source On resistance:  $R_{DS(on)}=0.6\Omega$  (Typ.)
- Ultra low gate charge:  $Q_g=8nC$ (Typ.)
- RoHS compliant device
- 100% avalanche tested

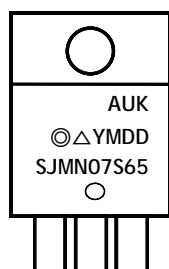
### Ordering Information

Part Number	Marking	Package
SJMN07S65FD	SJMN07S65	TO-220F-3L



TO-220F-3L

### Marking Information



Column 1: Manufacturer  
Column 2: Production Information  
e.g.) ◎△YMDD  
-.. ◎△: Factory Management Code  
-.. YMDD: Date Code (Year, Month, Daily)  
Column 3: Device Code

### Absolute maximum ratings ( $T_C=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	650	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	V
Drain current (DC) (Note 1)	$I_D$	$T_C=25^{\circ}C$	7
		$T_C=100^{\circ}C$	4.4
Drain current (Pulsed) (Note 1)	$I_{DM}$	28	A
Single pulsed avalanche energy (Note 2)	$E_{AS}$	141	mJ
Avalanche current (Note 1)	$I_{AS}$	2	A
Power dissipation	$P_D$	35	W
Junction temperature	$T_J$	150	$^{\circ}C$
Storage temperature range	$T_{stg}$	-55-150	$^{\circ}C$

\* Limited only maximum junction temperature

## Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.57	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 80	

Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu\text{A}$ , $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$ , $V_{DS}=V_{GS}$	2.5	3.5	4.5	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=650\text{V}$ , $V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS}=520\text{V}$ , $T_J=125^{\circ}\text{C}$	-	-	10	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$	-	0.6	0.7	$\Omega$
Input capacitance	$C_{iss}$	$V_{DS}=25\text{V}$ , $V_{GS}=0\text{V}$ , $f=1\text{MHz}$	-	375	-	pF
Output capacitance	$C_{oss}$		-	140	-	
Reverse transfer capacitance	$C_{rss}$		-	7	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DS}=400\text{V}$ , $I_D=3.5\text{A}$ , $R_G=25\Omega$	-	38	-	ns
Rise time (Note 3,4)	$t_r$		-	73	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	92	-	
Fall time (Note 3,4)	$t_f$		-	37	-	
Total gate charge (Note 3)	$Q_g$	$V_{DS}=520\text{V}$ , $V_{GS}=10\text{V}$ , $I_D=3.5\text{A}$	-	8	13	nC
Gate-source charge (Note 3)	$Q_{gs}$		-	3.5	-	
Gate-drain charge (Note 3)	$Q_{gd}$		-	2	-	

Source-Drain Diode Ratings and Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	7	A
Source current (Pulsed)	$I_{SM}$		-	-	18	A
Forward voltage	$V_{SD}$	$V_{GS}=0\text{V}$ , $I_S=7\text{A}$	-	-	1.5	V
Reverse recovery time (Note 3,4)	$t_{rr}$	$I_S=7\text{A}$ , $V_{GS}=0\text{V}$ , $V_{DS}=100\text{V}$ $di_S/dt=100\text{A}/\mu\text{s}$	-	430	-	ns
Reverse recovery charge (Note 3,4)	$Q_{rr}$		-	2.8	-	$\mu\text{C}$

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2.  $L=60\text{mH}$ ,  $I_{AS}=2\text{A}$ ,  $V_{DD}=100\text{V}$ , Starting  $T_J=25^{\circ}\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$ , Duty cycle $\leq 2\%$
4. Guaranteed by design, not subject to production testing

## Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

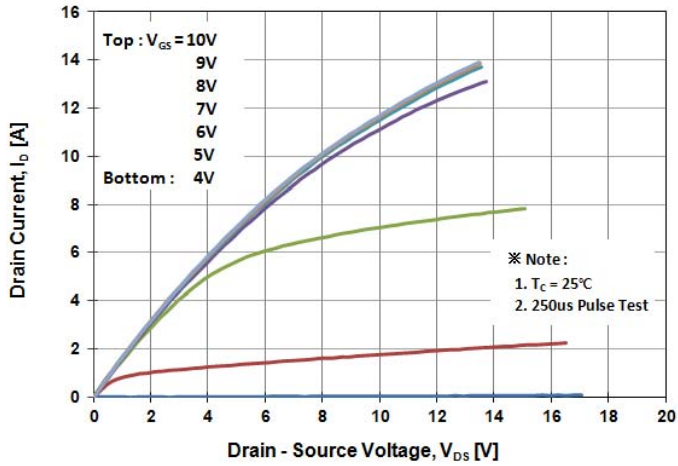


Fig. 2 Typical Output Characteristics

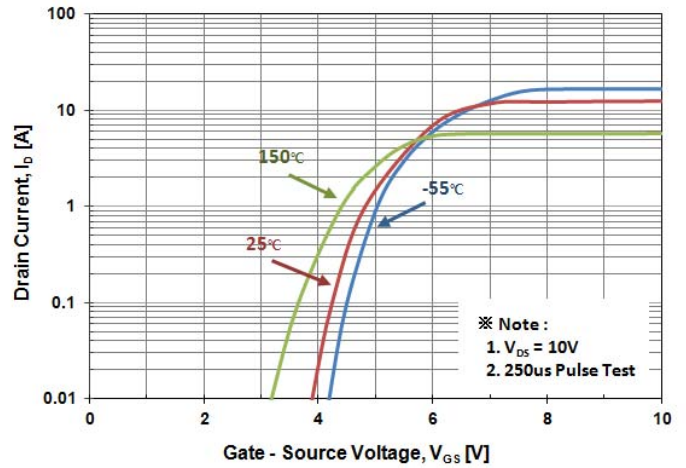


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

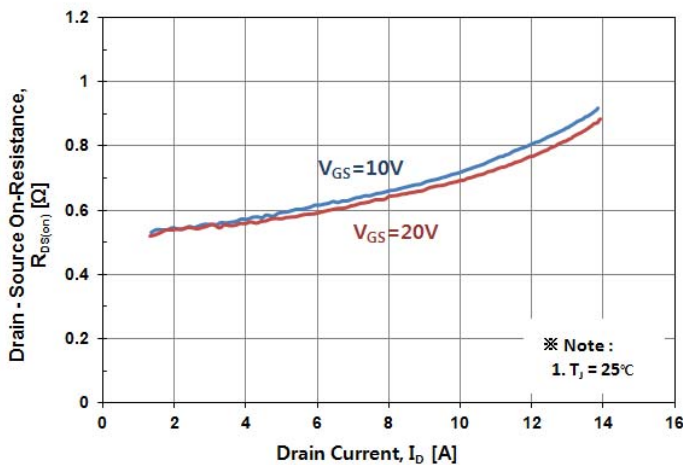


Fig. 4 Body Diode Forward Voltage Variation with Source Current

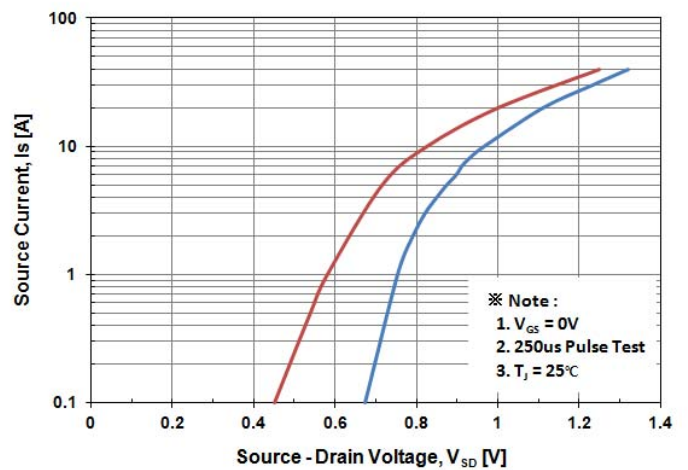


Fig. 5 Typical Capacitance Characteristics

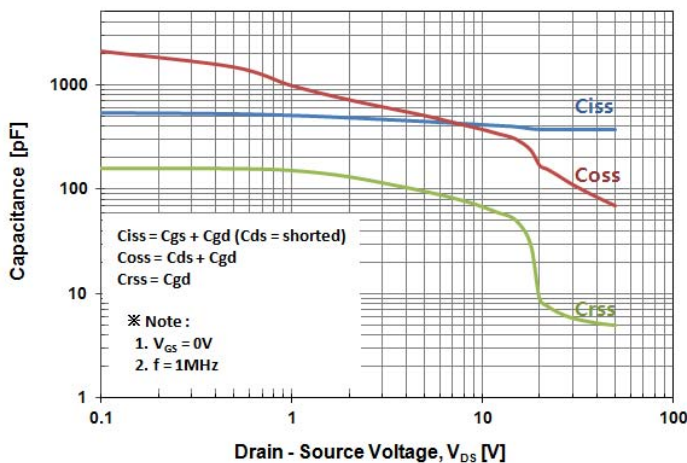


Fig. 6 Typical Total Gate Charge Characteristics

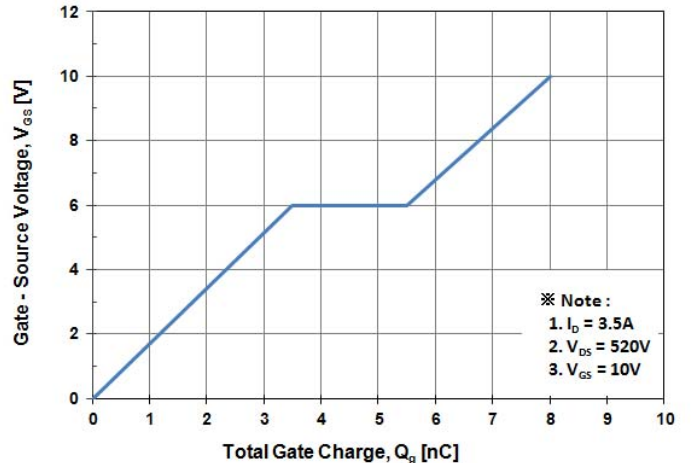


Fig. 7 Breakdown Voltage Variation vs. Temperature

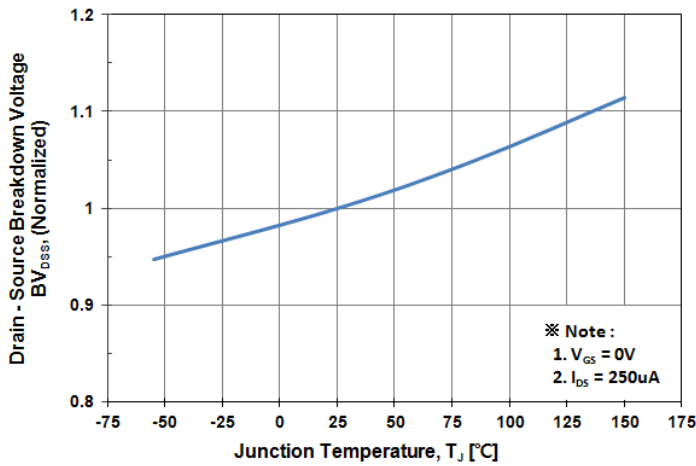


Fig. 8 On-Resistance Variation vs. Temperature

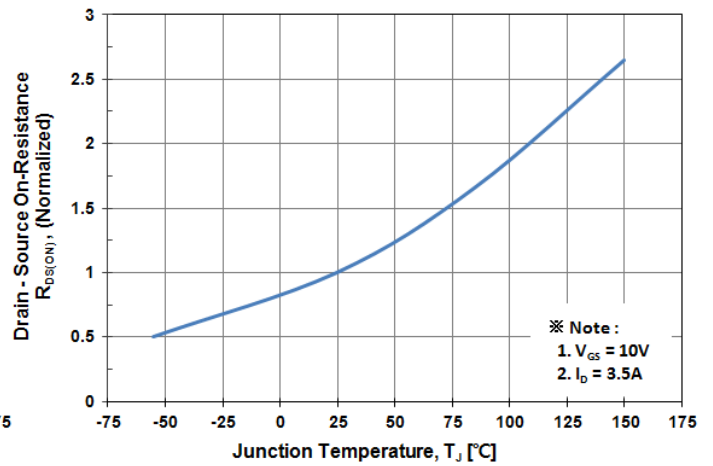


Fig. 9 Maximum Drain Current vs. Case Temperature

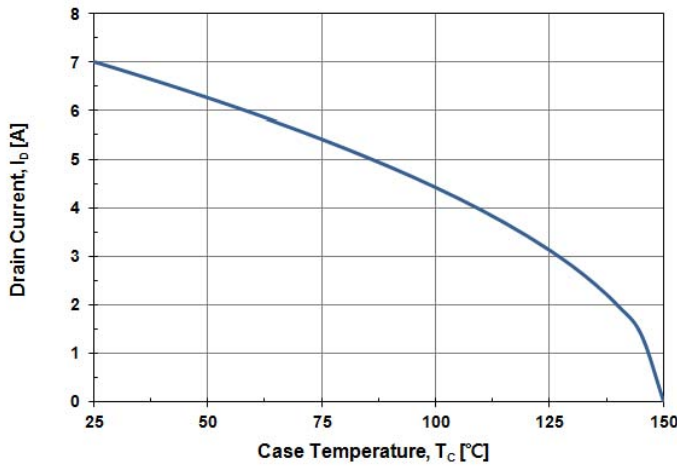


Fig. 10 Maximum Safe Operating Area

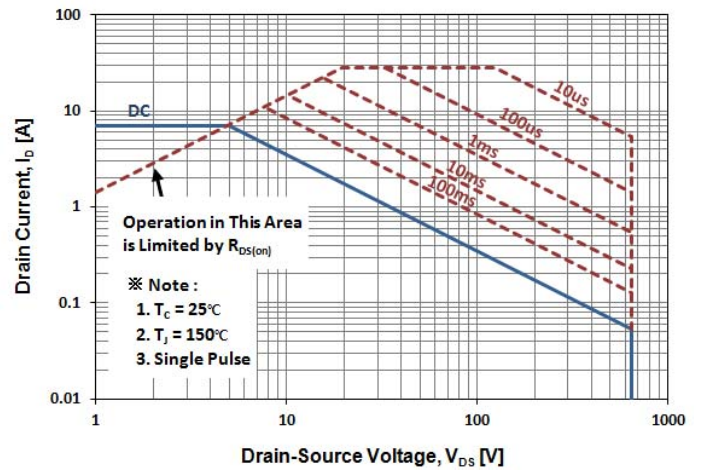


Fig. 11 Transient Thermal Impedance

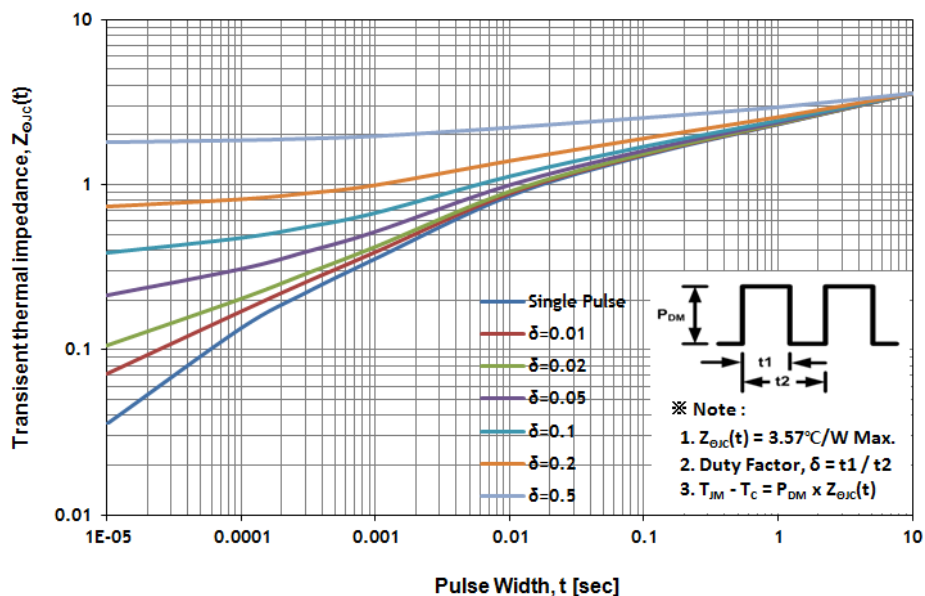


Fig. 12 Gate Charge Test Circuit & Waveform

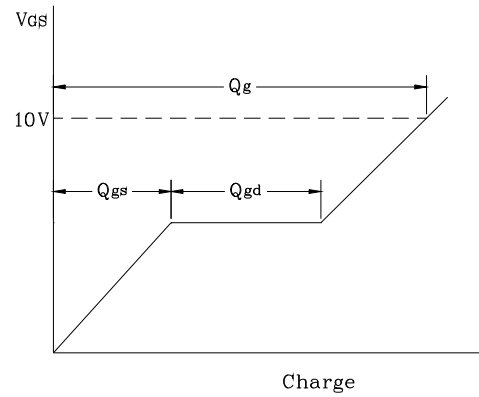
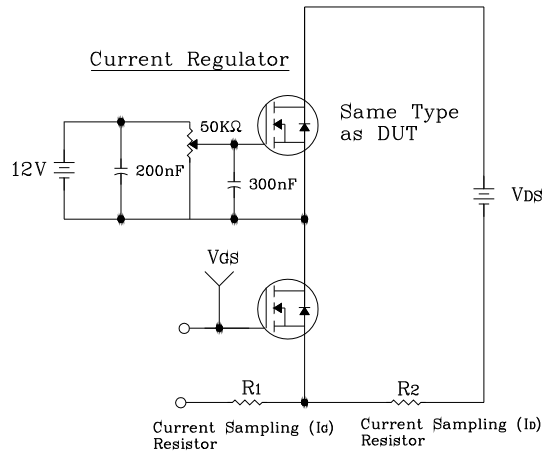


Fig. 13 Resistive Switching Test Circuit & Waveform

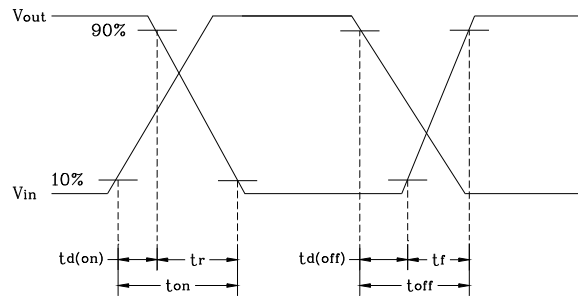
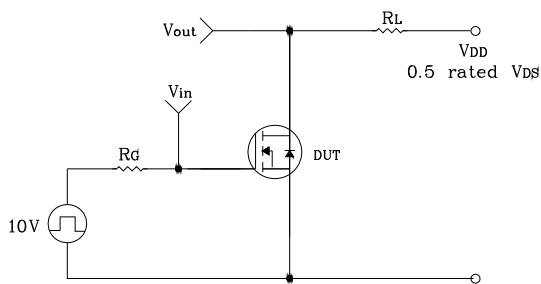


Fig. 14  $E_{AS}$  Test Circuit & Waveform

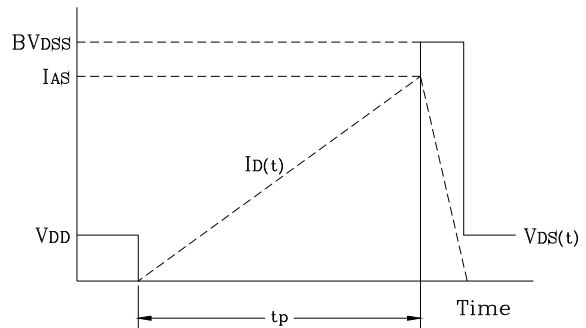
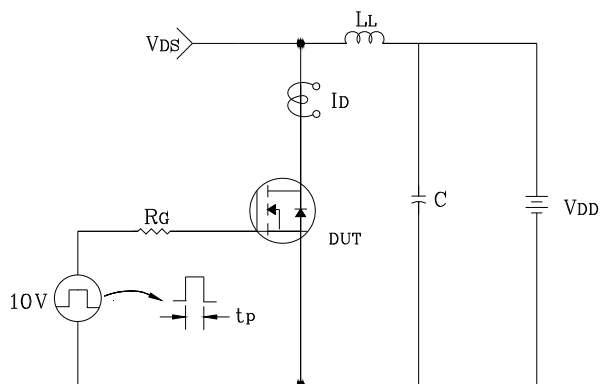
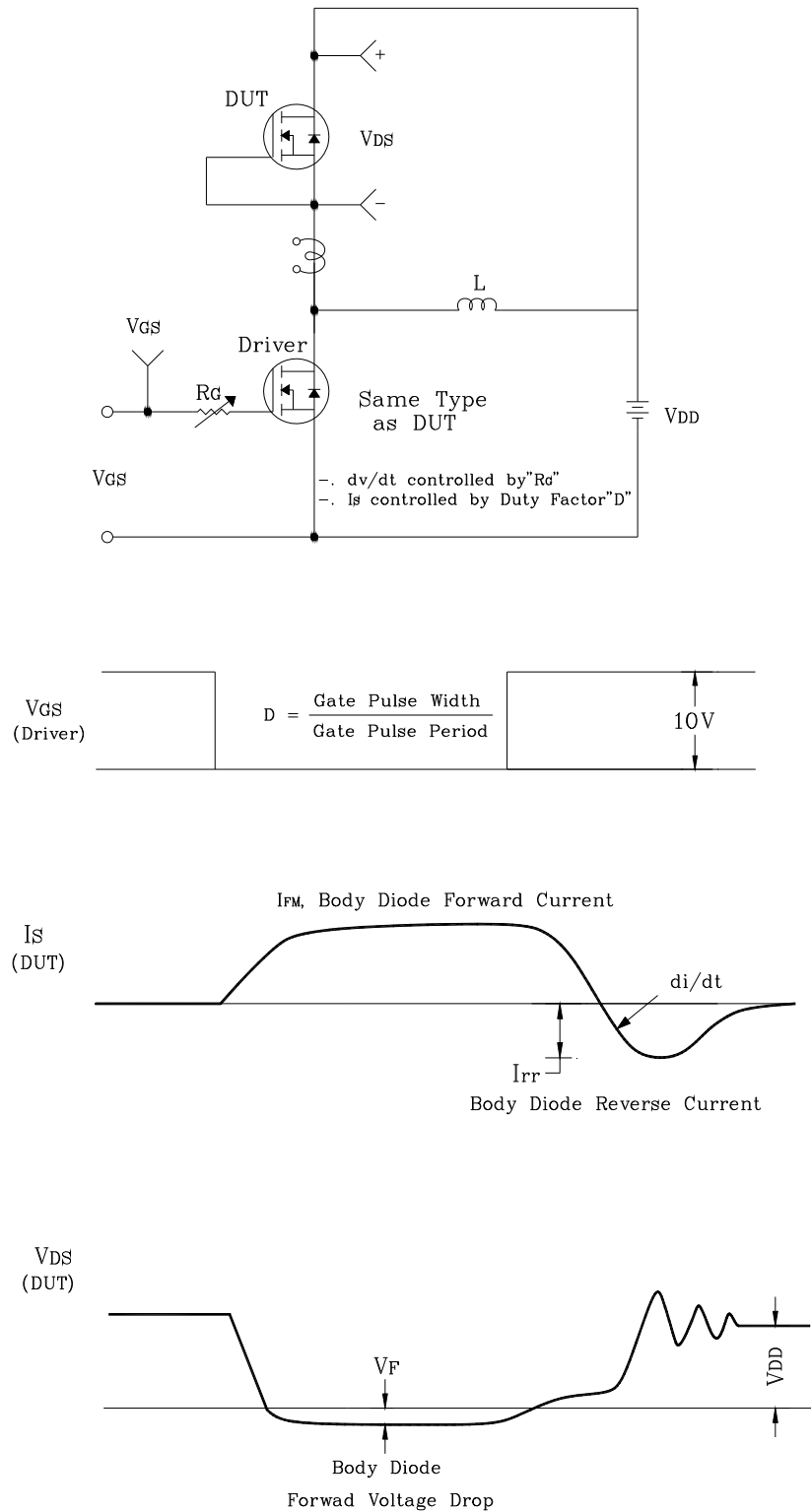
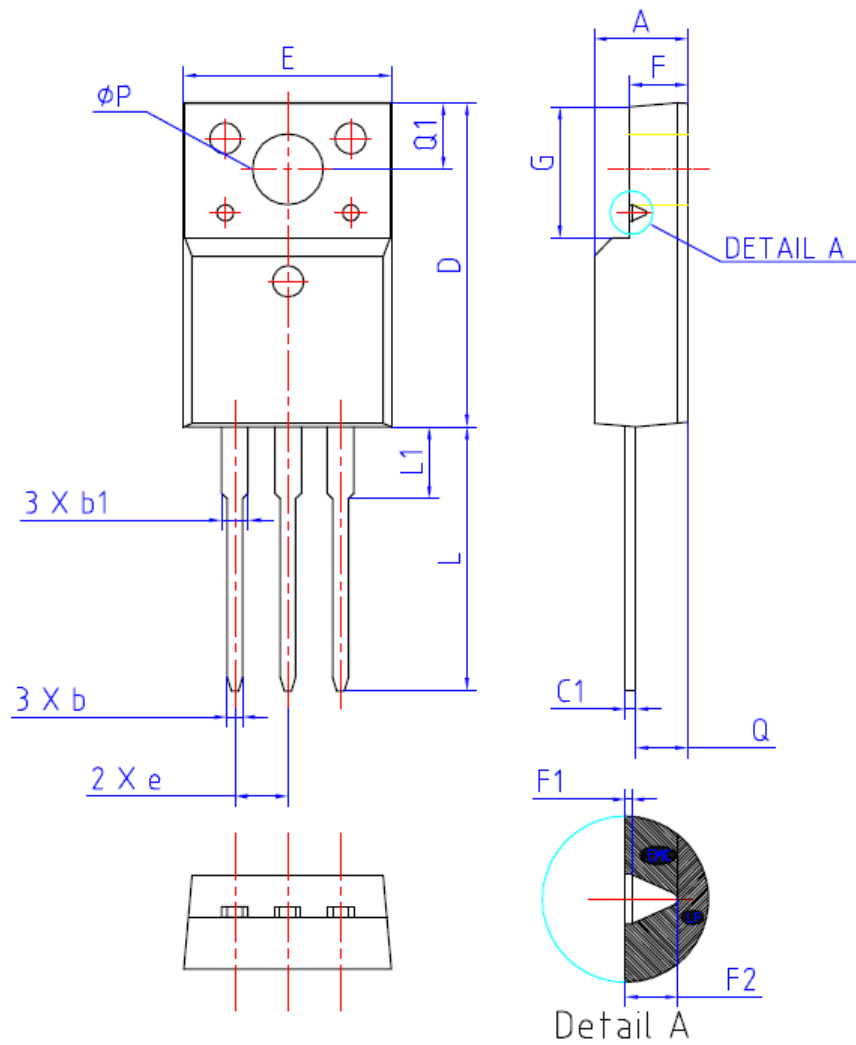


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.50	4.70	4.90	
b	0.70	0.80	0.90	
b1	1.33	1.40	1.47	
C1	0.45	0.50	0.60	
D	15.67	15.87	16.07	
E	9.96	10.16	10.36	
e	2.54BSC			
F	2.34	2.54	2.74	
F1	(0.10 REF)			
F2	(0.84 REF)			
G	6.48	6.68	6.88	
L	12.78	12.98	13.18	
L1	3.03	3.23	3.43	
Q	2.56	2.76	2.96	
Q1	3.10	3.30	3.50	
ØP	3.08	3.18	3.28	

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