

Vishay Siliconix

Dual N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)		
20	0.053 at V _{GS} = 4.5 V	4.5			
	0.063 at V _{GS} = 2.5 V	4.5	4.1 nC		
	0.077 at V _{GS} = 1.8 V	4.5			

FEATURES

- · Halogen-free
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package

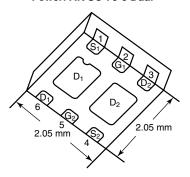
· Load Switch for Portable Applications

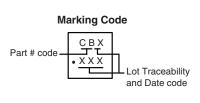
- Small Footprint Area
- Low On-Resistance

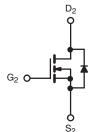
APPLICATIONS



PowerPAK SC-70-6 Dual







N-Channel MOSFET

N-Channel MOSFET

Ordering Information: SiA914DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	20	V	
Gate-Source Voltage		V_{GS}	± 8	v	
	T _C = 25 °C		4.5 ^a		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	4.5 ^a		
Continuous Diain Current (1) = 130 C)	T _A = 25 °C	ן טי [4.5 ^{a, b, c}		
	T _A = 70 °C		3.8 ^{b, c}	Α	
Pulsed Drain Current		I _{DM}	20		
Continuous Source-Drain Diode Current	T _C = 25 °C		4.5 ^a		
	T _A = 25 °C	I _S	1.6 ^{b, c}		
Maximum Power Dissipation	T _C = 25 °C		6.5		
	T _C = 70 °C	P _D	5	w	
	T _A = 25 °C	l 'b [1.9 ^{b, c}	VV	
	T _A = 70 °C	1	1.2 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol Typical		Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	52	65	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16] 0,11	

Notes:

- a. Package limitedb. Surface Mounted on 1" x 1" FR4 board.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 110 °C/W

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-						
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			٧	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L 050A		19		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_{J}$	I _D = 250 μA		- 2.8			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	0.4		1.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			- 1		
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	- 20			Α	
	(,	$V_{GS} = 4.5 \text{ V}, I_D = 3.7 \text{ A}$		0.043	0.053	Ω	
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, I_D = 3.4 \text{ A}$		0.052	0.063		
Drain-Source On-State Resistance ^a		V _{GS} = 1.8 V, I _D = 1.1 A		0.062	0.077		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 3.7 A		15		S	
Dynamic ^b	•						
Input Capacitance	C _{iss}			400		pF	
Output Capacitance	C _{oss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		70			
Reverse Transfer Capacitance	C _{rss}			40			
•		$V_{DS} = 10 \text{ V}, V_{GS} = 8 \text{ V}, I_D = 4.8 \text{ A}$		7	11.5		
Total Gate Charge	Q_g			4.1	7	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 4.8 \text{ A}$		0.65			
Gate-Drain Charge	Q _{gd}			0.8			
Gate Resistance	R_g	f = 1 MHz		2.5		Ω	
Turn-on Delay Time	t _{d(on)}			5	10		
Rise Time	t _r	V -10 V B - 26 O		32	50		
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 10 \text{ V}, R_L = 2.6 \Omega$ $I_D \cong 3.8 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$		30	45		
Fall Time	t _f	D = 0.07, *GEN = 1.0 *, * · · · · · · · · · · · · · · · · ·		53	80		
Turn-on Delay Time	t _{d(on)}			5	10	ns	
Rise Time	t _r	$V_{DD} = 10 \text{ V, R}_{L} = 2.6 \Omega$		12	20	1	
Turn-Off Delay Time	t _{d(off)}	$V_{DD} = 10 \text{ V}, R_L = 2.6 \Omega$ $I_D \cong 3.8 \text{ A}, V_{GEN} = 8 \text{ V}, R_q = 1 \Omega$		15	25	-	
Fall Time	t _f	D = 0.0 A, VGEN = 0 V, Fig = 1.32		10	15		
Drain-Source Body Diode Characteristic	s			•	•		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.5		
Pulse Diode Forward Current	I _{SM}				20	A	
Body Diode Voltage	V_{SD}	$I_S = 3.8 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			15	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			8.5	20	nC	
Reverse Recovery Fall Time	t _a	$I_F = 3.8 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		10		ns	
Reverse Recovery Rise Time	t _b			5			

Notes:

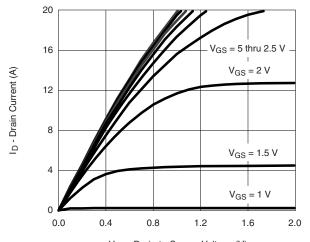
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



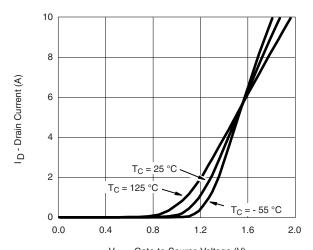
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

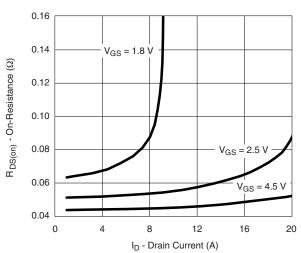


V_{DS} - Drain-to-Source Voltage (V)

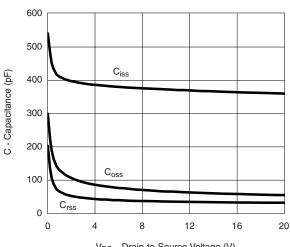
Output Characteristics



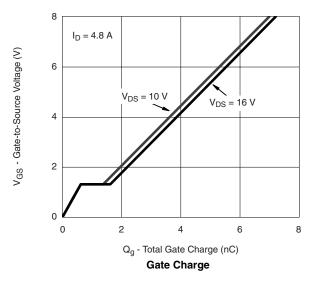
V_{GS} - Gate-to-Source Voltage (V) **Transfer Characteristics**

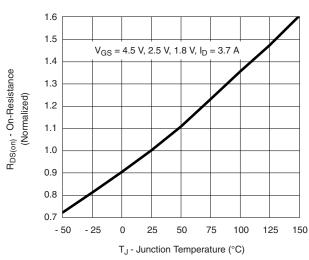


On-Resistance vs. Drain Current and Gate Voltage



V_{DS} - Drain-to-Source Voltage (V) **Capacitance**





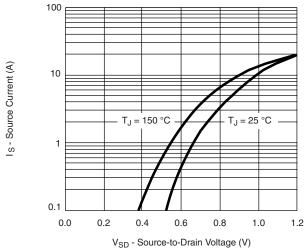
On-Resistance vs. Junction Temperature

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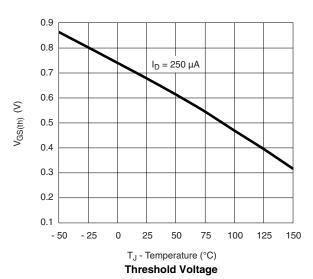
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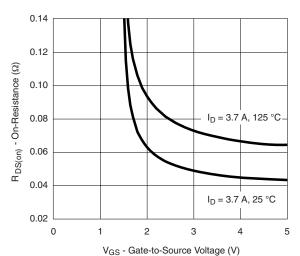
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

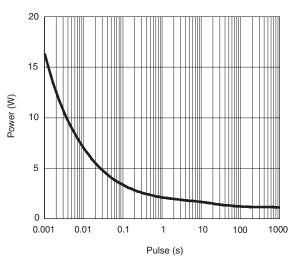


Source-Drain Diode Forward Voltage

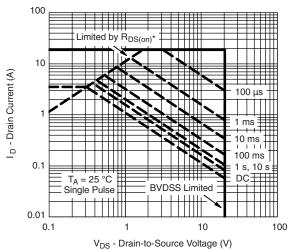




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



* V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

Safe Operating Area, Junction-to-Ambient

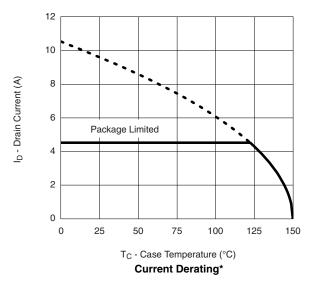
Power Dissipation (W)

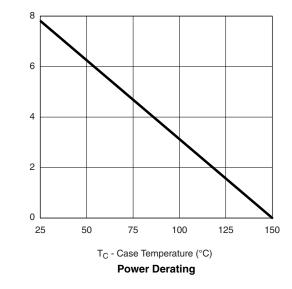




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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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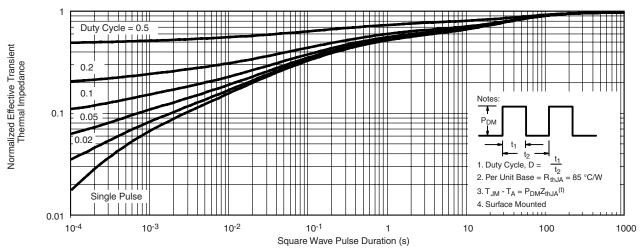
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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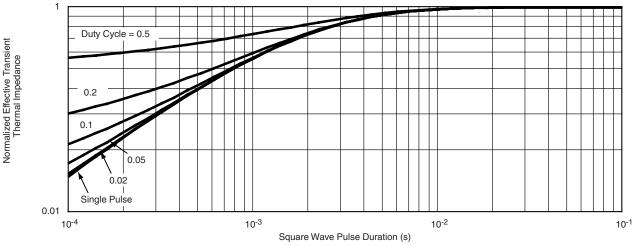
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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