HALOGEN

FREE



Vishay Siliconix

# N-Channel 8 V (D-S) MOSFET

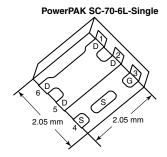
PRODUCT SUMMARY									
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$ Max.	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)						
	0.0094 at V <sub>GS</sub> = 4.5 V	12							
	0.0105 at V <sub>GS</sub> = 2.5 V	12							
8	0.0125 at V <sub>GS</sub> = 1.8 V	12	15 nC						
	0.0180 at V <sub>GS</sub> = 1.5 V	12							
	0.0360 at V <sub>GS</sub> = 1.2 V	12							

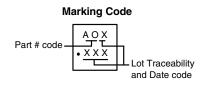
#### **FEATURES**

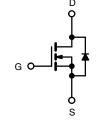
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
- 100 % R<sub>q</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

### **APPLICATIONS**

- Load Switch for Portable Applications such as Smart Phones, Tablet PCs and Mobile Computing
  - Low Voltage Gate Drive
  - Low Voltage Drop
  - Power Switch for ICs







Ordering Information: SiA436DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Unit	Limit	Symbol	Parameter				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	V	8	$V_{DS}$	Drain-Source Voltage				
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	<b>一                                    </b>	± 5	$V_{GS}$		Gate-Source Voltage			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		·-						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	<del></del>	·=	I <sub>D</sub>		Continuous Drain Current (T <sub>J</sub> = 150 °C)			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	A	12 <sup>a, b, c</sup>						
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		50	I <sub>DM</sub>	Pulsed Drain Current (t = 300 μs)				
$ \begin{array}{c c} \hline T_C = 70 \ ^{\circ}C \\ \hline T_A = 25 \ ^{\circ}C \\ \hline T_A = 70 \ ^{\circ}C \\ \end{array} \qquad \begin{array}{c c} P_D & 12 \\ \hline 3.5^{b, \ c} \\ \hline 2.2^{b, \ c} \\ \end{array} $		<del></del>	Is		Continuous Source-Drain Dioge Current			
$ T_{A} = 25  ^{\circ}\text{C}                                   $					Maximum Power Dissipation			
	W	3.5 <sup>b, c</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C				
Operating surrouser and storage reinperature name 1, 1, 1 sta 1 - 35 to 150			т. т.	,,	1			
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>	°C		'J, 'stg	, , , ,				

THERMAL RESISTANCE RATINGS										
Parameter		Symbol	Typical	Maximum	Unit					
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	R <sub>thJA</sub>	28	36	°C/W					
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	5.3	6.5	0///					

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (<a href="https://www.vishay.com/ppq273257">www.vishay.com/ppq273257</a>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
   e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

Document Number: 63535 S11-2242-Rev. A, 14-Nov-11 www.vishay.com

## SiA436DJ

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<b>SPECIFICATIONS</b> ( $T_J = 25  ^{\circ}C$ , Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	Symbol	rest conditions	IVIIII.	тур.	IVIAX.	Onic
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, } I_D = 250 \mu\text{A}$	8			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	VGS = 0 V, 1D = 200 μ V		11		, v
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 2.5		mV/°
Gate-Source Threshold Voltage		$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	0.35	- 2.5	0.8	V
Gate-Source Leakage	V <sub>GS(th)</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$	0.55		± 100	-
Gale-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 8 \text{ V}, V_{GS} = 2 \text{ V}$ $V_{DS} = 8 \text{ V}, V_{GS} = 0 \text{ V}$				nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 8 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 8 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			1	μΑ
					10	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			Α
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15.7 A		0.0078	0.0094	
	_	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 14.9 A		0.0087	0.0105	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 13.6 A		0.0104	0.0125	Ω
		$V_{GS} = 1.5 \text{ V}, I_D = 2.5 \text{ A}$		0.0120	0.0180	
		$V_{GS} = 1.2 \text{ V}, I_D = 1.5 \text{ A}$		0.0180	0.0360	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 4 \text{ V}, I_{D} = 15.7 \text{ A}$		70		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			1508		
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		535		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			321		
Tatal Cata Chausa	Q <sub>g</sub>	V <sub>DS</sub> = 4 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 15.7 A		16.8	25.2	nC
Total Gate Charge				15	23	
Gate-Source Charge		$V_{DS} = 4 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 15.7 \text{ A}$		1.7		
Gate-Drain Charge	Q <sub>gd</sub>			0.9		
Gate Resistance	$R_{g}$	f = 1 MHz	0.5	2.5	5	Ω
Turn-on Delay Time	t <sub>d(on)</sub>			11	20	
Rise Time	t <sub>r</sub>	1 , , , , , , , , , , , , , , , , , , ,		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{DD} = 4 \text{ V}, R_L = 0.4 \Omega$ $I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$		30	45	
Fall Time	t <sub>f</sub>	$I_D = 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, N_g = 1.52$		8	16	
Turn-on Delay Time	t <sub>d(on)</sub>			10	20	ns
Rise Time	t <sub>r</sub>	1 <u>-</u>		10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{DD} = 4 \text{ V}, R_L = 0.4 \Omega$		30	45	
Fall Time	t <sub>f</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 5 \text{ V}, R_g = 1 \Omega$		8	16	
Drain-Source Body Diode Characteristic						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			12	
Pulse Diode Forward Current	I <sub>SM</sub>	-			50	1 A
ody Diode Voltage V <sub>SD</sub>		I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		0.73	1.2	V
Body Diode Reverse Recovery Time t <sub>rr</sub>				10	20	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	1		1	4	nC
Reverse Recovery Fall Time	t <sub>a</sub>	$I_F = 10 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		4		
Reverse Recovery Rise Time	t <sub>b</sub>	1		6		ns

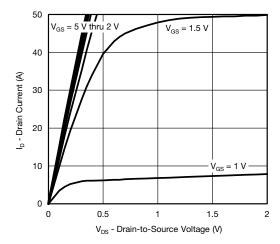
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 % b. Guaranteed by design, not subject to production testing.

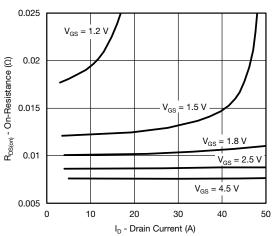


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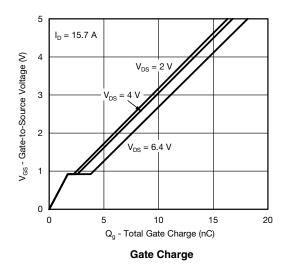
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

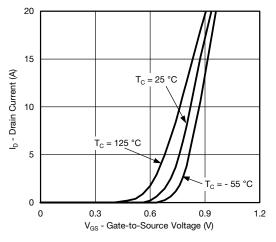


#### **Output Characteristics**

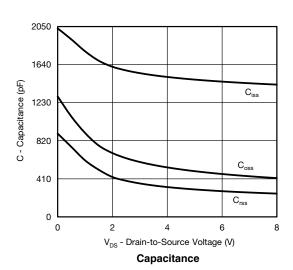


On-Resistance vs. Drain Current and Gate Voltage





**Transfer Characteristics** 



 $V_{GS} = 4.5 \text{ V}$ I<sub>D</sub> = 15.7 A R<sub>DS(on)</sub> - On-Resistance (Normalized) 1.3  $V_{GS} = 2.5 \text{ V}$ 1.1 0.9 0.7 - 50 - 25 0 25 75 100 125 50

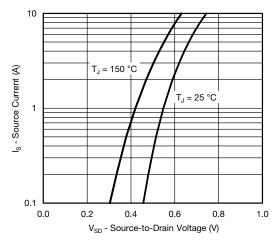
T<sub>J</sub> - Junction Temperature (°C) On-Resistance vs. Junction Temperature

1.5

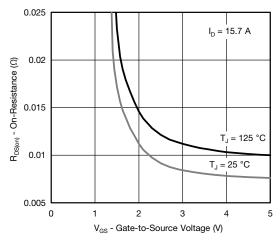
# SiA436DJ

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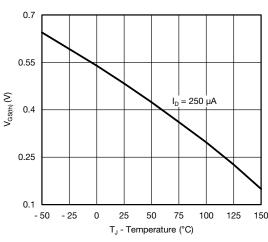
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



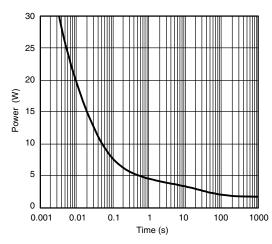
Source-Drain Diode Forward Voltage



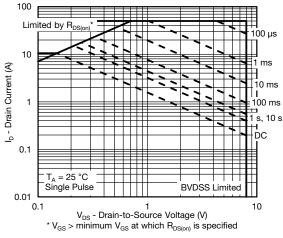
On-Resistance vs. Gate-to-Source Voltage



**Threshold Voltage** 



Single Pulse Power (Junction-to-Ambient)

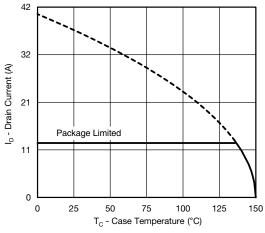


Safe Operating Area, Junction-to-Ambient

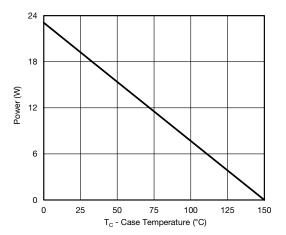


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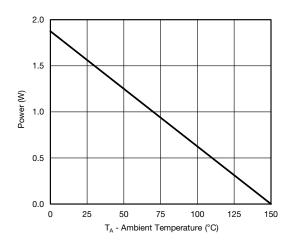
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\*** 



Power Derating, Junction-to-Case



Power Derating, Junction-to-Ambient

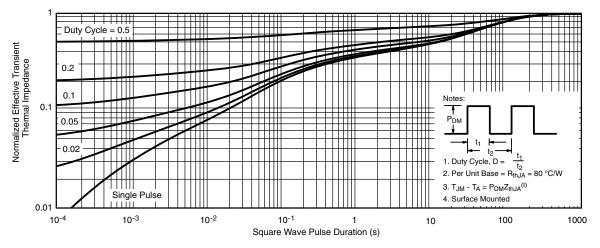
Document Number: 63535 S11-2242-Rev. A, 14-Nov-11

 $<sup>^*</sup>$  The power dissipation  $P_D$  is based on  $T_{J(max.)}$  = 150  $^{\circ}$ C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

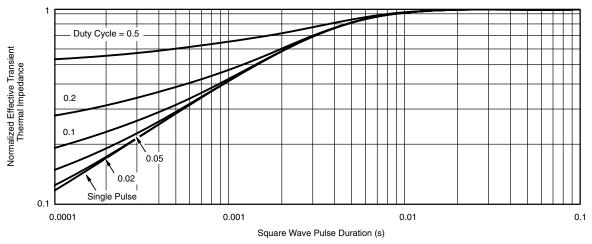
## SiA436DJ

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### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

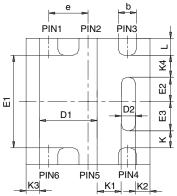
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63535





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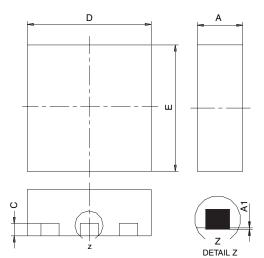
## PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
   Package outline exclusive of mold flash and metal burr
   Package outline inclusive of plating

		SINGLE PAD						DUAL PAD					
DIM	M	ILLIMETER	RS		INCHES		MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC		0.026 BSC			0.65 BSC			0.026 BSC			
K		0.275 TYP	1		0.011 TYP	1	0.275 TYP			0.011 TYP			
K1		0.400 TYP	1		0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP	1	0.009 TYP			0.252 TYP			0.010 TYP			
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP		0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
FCN: C-07431 - Rev. C. 06-Aug-07													

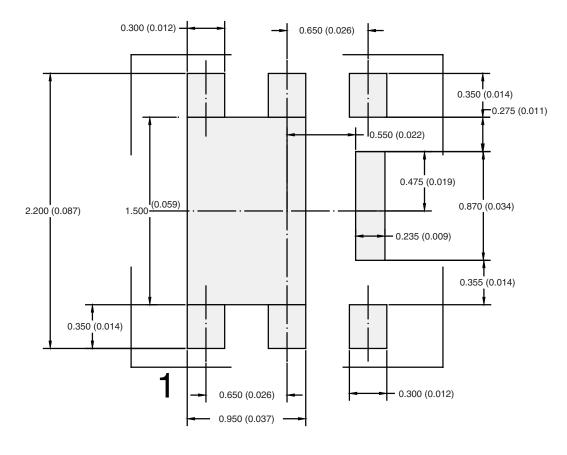
DWG: 5934

Document Number: 73001 06-Aug-07

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## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOTE



## **Legal Disclaimer Notice**

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Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.