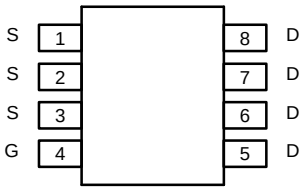
N-Channel Reduced Q_g, Fast Switching MOSFET

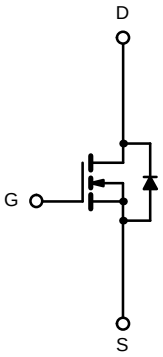
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
200	0.420 @ V_{GS} = 10 V	±1.7

High-Efficiency PWM Optimized

SO-8



Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150°C)[a, b]	T_A = 25°C	I_D	±1.7	A
	T_A = 70°C		±1.3	
Pulsed Drain Current		I_{DM}	±12	
Avalanche Current	L = 0.1 mH	I_{AS}	±12.5	
Single Avalanche Energy		E_{AS}	8	mJ
Continuous Source Current (Diode Conduction)[a, b]		I_S	2.1	A
Maximum Power Dissipation[a, b]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}		50	°C/W
	Steady State		80		

Notes
a. Surface Mounted on FR4 Board.
b. t ≤ 10 sec.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

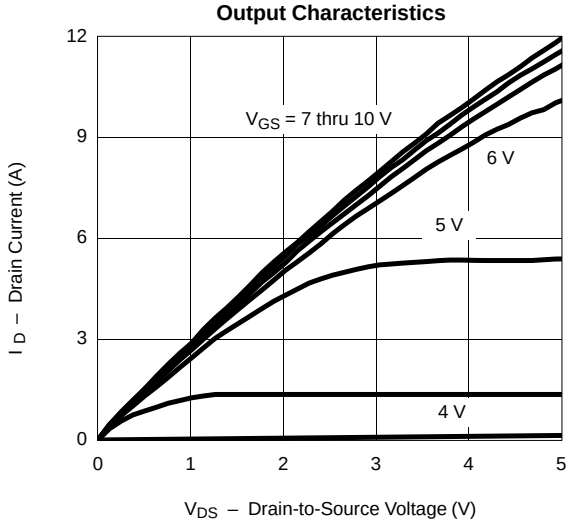
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160 V, V_{GS} = 0 V			1	μA
		V_{DS} = 160 V, V_{GS} = 0 V, T_J = 55°C			25	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	5			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 1.7 A		0.340	0.420	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 1.7 A		3.5		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.1 A, V_{GS} = 0 V		0.95	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 1.7 A		13	25	nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			4.5		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 100 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			20	40	
Fall Time	t_f			25	50	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1 A, di/dt = 100 A/μs		115	150	

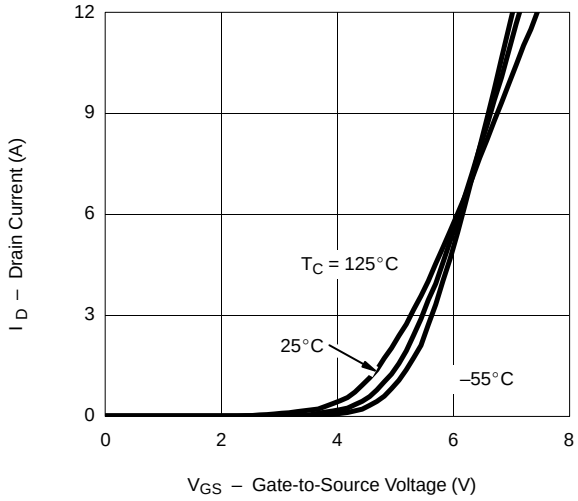
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

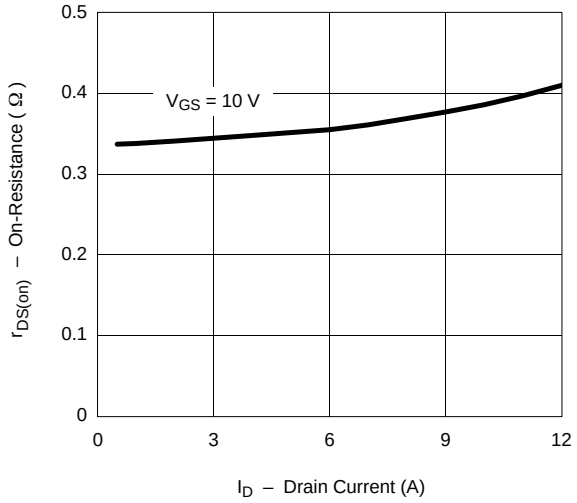
Output Characteristics



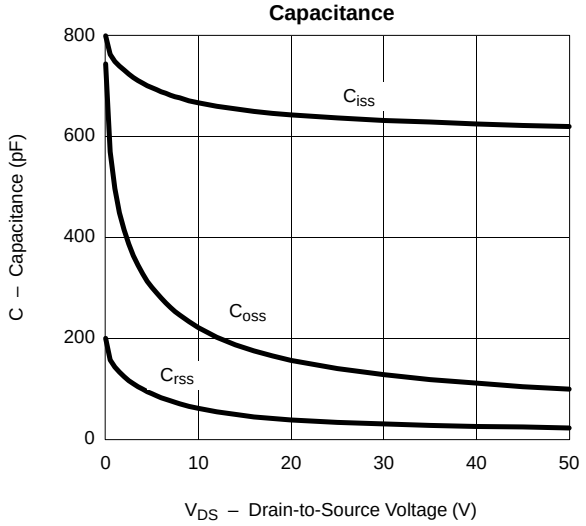
Transfer Characteristics



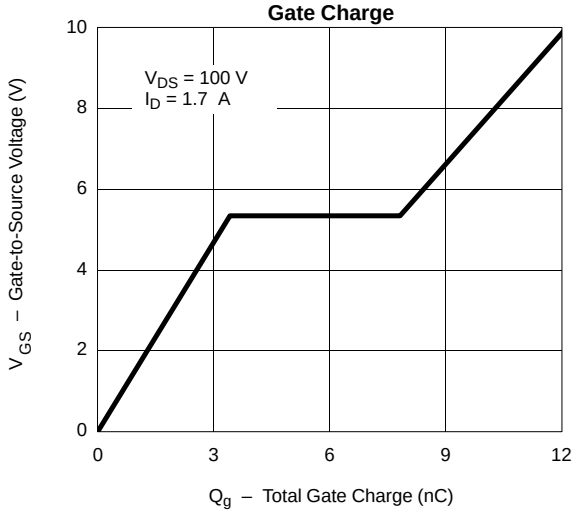
On-Resistance vs. Drain Current



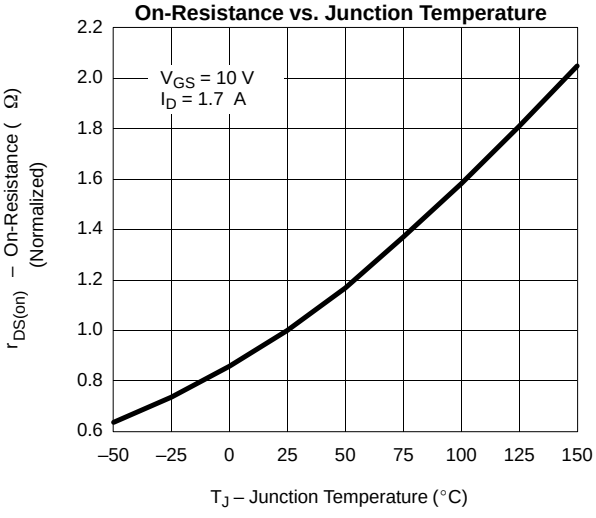
Capacitance



Gate Charge

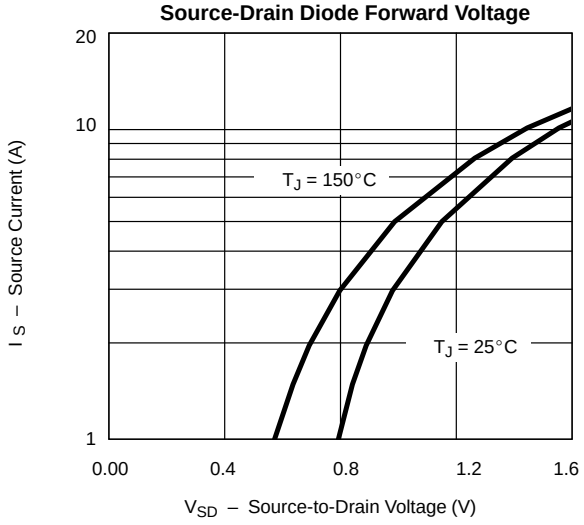


On-Resistance vs. Junction Temperature

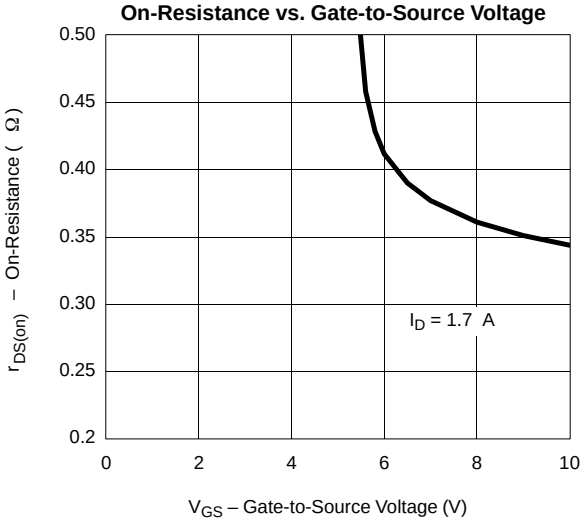


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

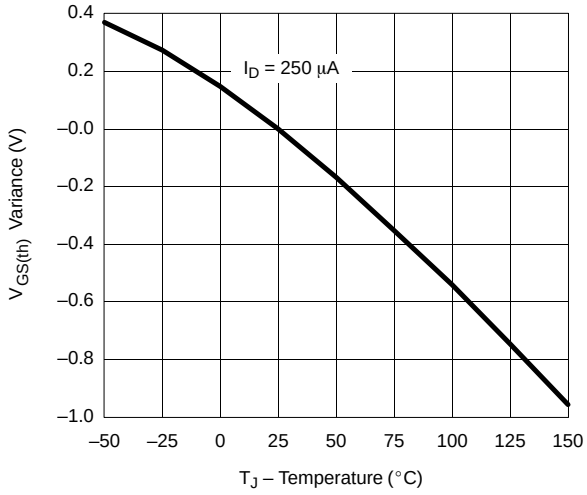
Source-Drain Diode Forward Voltage



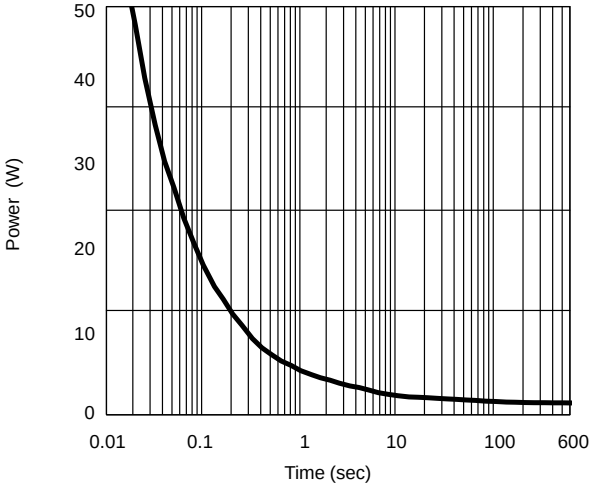
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient