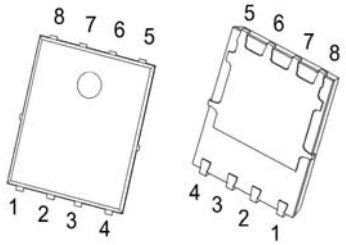
N-Channel MOSFET

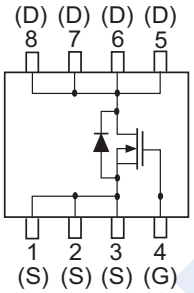
SI7738DP (KI7738DP)

DFN5x6-8(PDFNWB5x6-8L)



■ Features

- $V_{DS\ (V)}$ = 150V
- I_D = 30 A
- $R_{DS(ON)} \leqslant$ 38mΩ (V_{GS} = 10V)



■ Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J=150℃)	T_C=25℃	I_D	30 [a]	A
	T_C=70℃		26	
	T_A=25℃		7.7 [b,c]	
	T_A=70℃		6.2 [b,c]	
Pulsed Drain Current		I_{DM}	60	
Continuous Source-Drain Diode Current	T_C=25℃	I_S	30 [a]	
	T_A=25℃		4.5 [b,c]	
Single Pulse Avalanche Current	L=0.1mH	IAS	30	
Single Pulse Avalanche Energy		EAS	45	mJ
Maximum Power Dissipation	T_C=25℃	P_D	96	W
	T_C=70℃		62	
	T_A=25℃		5.4 [b,c]	
	T_A=70℃		3.5 [b,c]	
Thermal Resistance.Junction- to-Ambient [b,f]	t≤10s	R_{thJA}	23	℃/W
Thermal Resistance.Junction- to-Case (Drain)	Steady state	R_{thJC}	1.3	
Soldering Recommendations (Peak Temperature) [d,e]			260	℃
Junction Temperature		T_J	150	
Storage Temperature Range		T_{stg}	-55 to 150	

Notes: a.Package limited. b.Surface Mounted on 1" x 1" FR4 board. c.t = 10 s.

d.The DFN5X6-8 is a leadless package. The end of the lead terminal is exposed copper(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guararequired to ensure adequate bottom side solder interconnection.

e.Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f.Maximum under Steady State conditions is 65 °C/W.

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■ Electrical Characteristics (T_J = 25℃ unless othewise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=250μA, V_{GS}=0V	150			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=250μA		200		mV/℃
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-10		
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=150V, V_{GS}=0V			1	μA
		V_{DS}=150V, V_{GS}=0V, T_C=55℃			10	
Gate-Body Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=250μA	2		4	V
On-State Drain Current [a]	$I_{D(on)}$	V_{DS}≥5V, V_{GS}=10V	30			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=7.7A			38	mΩ
Forward Transconductance	g_{FS}	V_{DS}=15V, I_D=7.7A		22		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=75V, f=1MHz		2100		pF
Output Capacitance	C_{oss}			160		
Reverse Transfer Capacitance	C_{rss}			45		
Turn-On DelayTime	$t_{d(on)}$	V_{DD}=75V, R_L=12Ω, I_D=6.2A, V_{GEN}=10V, R_g=1Ω		15	25	ns
Turn-On Rise Time	t_r			10	15	
Turn-Off DelayTime	$t_{d(off)}$			25	40	
Turn-Off Fall Time	t_f			10	15	
Total Gate Charge	Q_g	V_{DS}=75V, I_D=7.7A, V_{GS}=10V		35	53	nC
Gate Source Charge	Q_{gs}			8		
Gate Drain Charge	Q_{gd}			9		
Body Diode Reverse Recovery Time	t_{rr}	I_F= 6.2A, dI/dt = 100A/μs, T_J=25℃		75	115	ns
Body Diode Reverse Recovery Charge	Q_{rr}			245	370	nC
Body Diode Reverse Recovery Fall Time	t_a			58		ns
Body Diode Reverse Recovery Rise Time	t_b			17		
Maximum Body-Diode Continuous Current	I_S	T_C=25℃			30	A
Maximum Body-Diode Current (Pulsed)	I_{SM}				30	
Diode Forward Voltage	V_{SD}	I_{SD}=6.2A,V_{GS}=0V			1.2	V

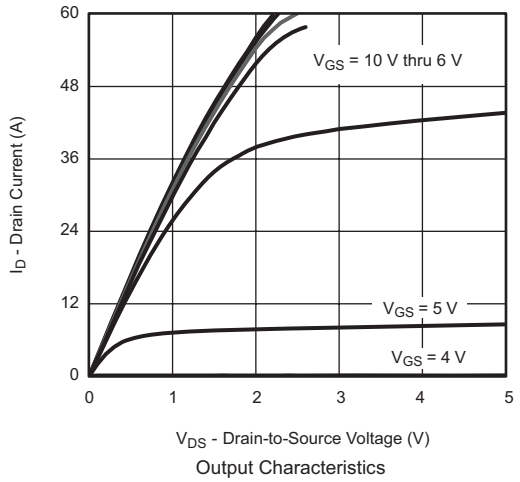
Notes: a. Pulse test; pulse width≤300 μs, duty cycle≤2%

b. Guaranteed by design, not subject to production testing.

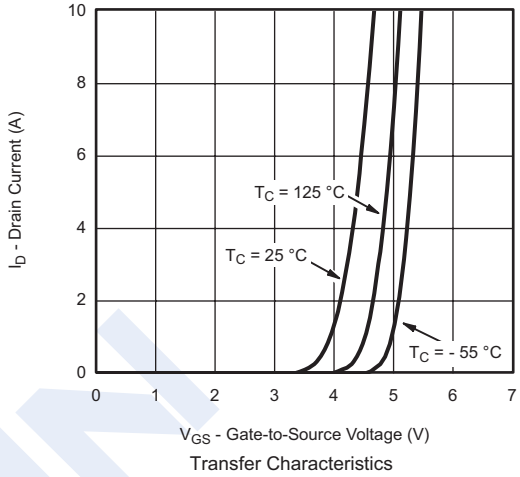
N-Channel MOSFET

SI7738DP (KI7738DP)

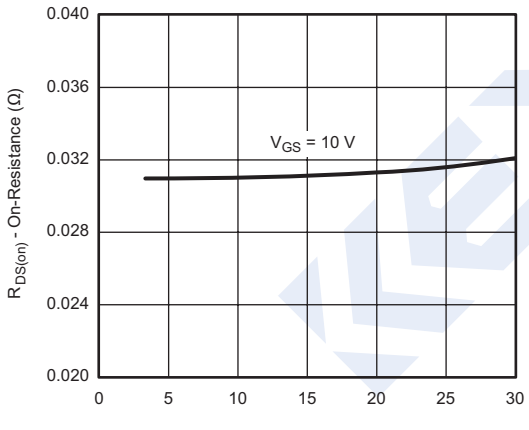
■ Typical Characterisitics 25℃ unless otherwise noted



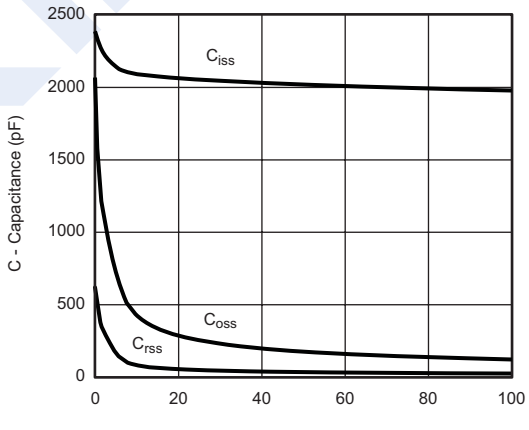
Output Characteristics



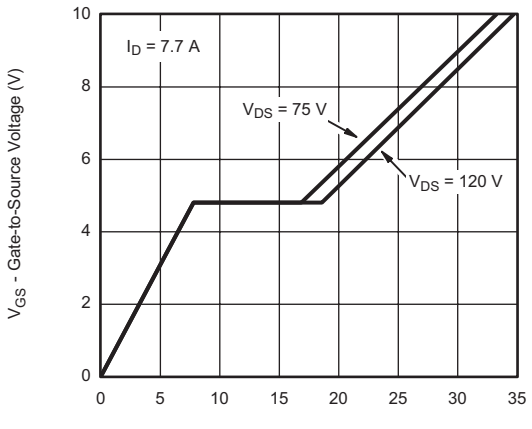
Transfer Characteristics



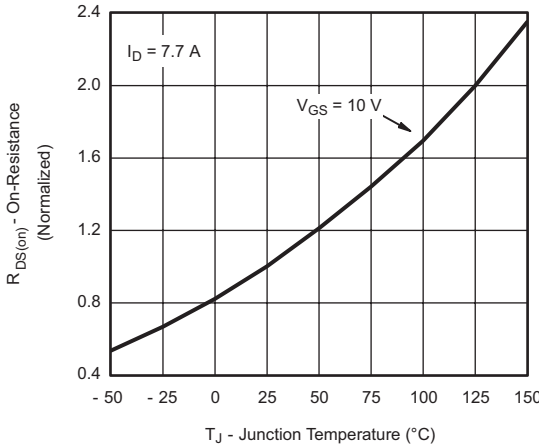
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge

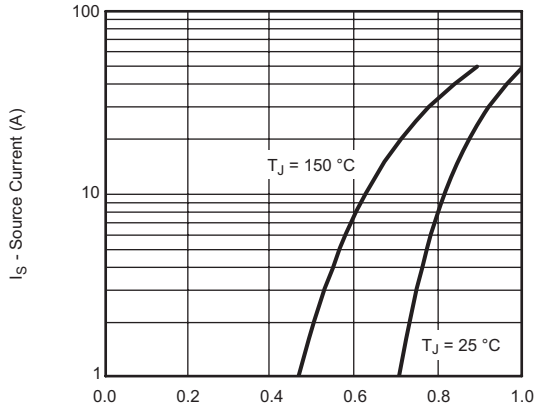


On-Resistance vs. Junction Temperature

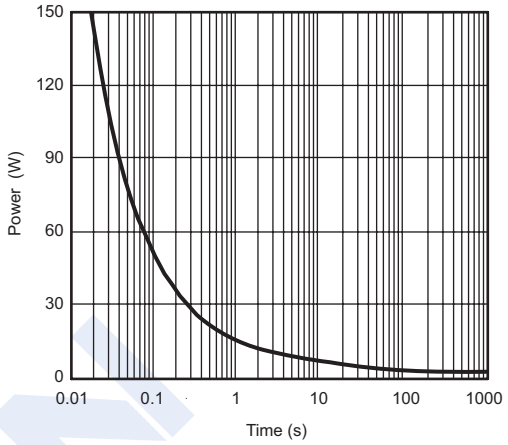
N-Channel MOSFET

SI7738DP (KI7738DP)

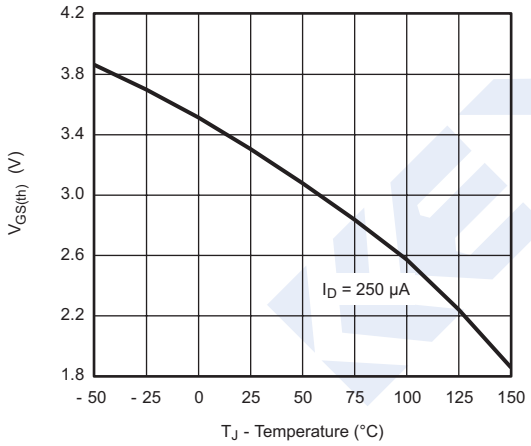
■ Typical Characterisitics 25℃ unless otherwise noted



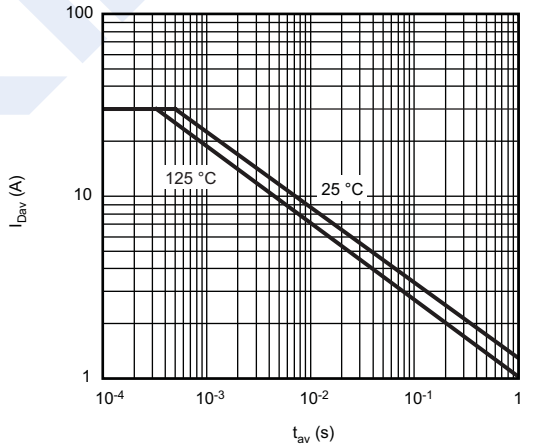
Source-Drain Diode Forward Voltage



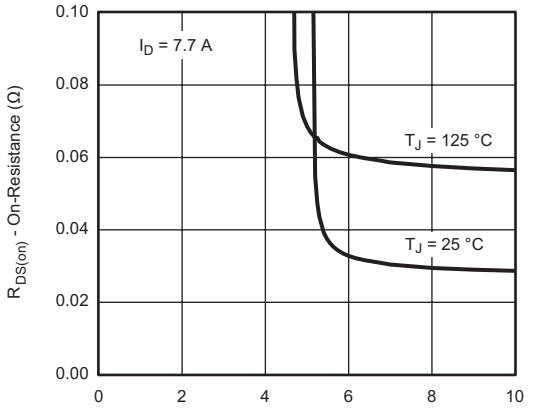
Single Pulse Power (Junction-to-Ambient)



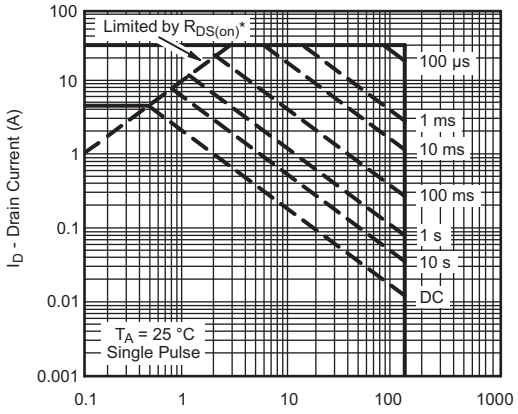
Threshold Voltage



Single Pulse Avalanche Current Capability vs. Time



On-Resistance vs. Gate-to-Source Voltage



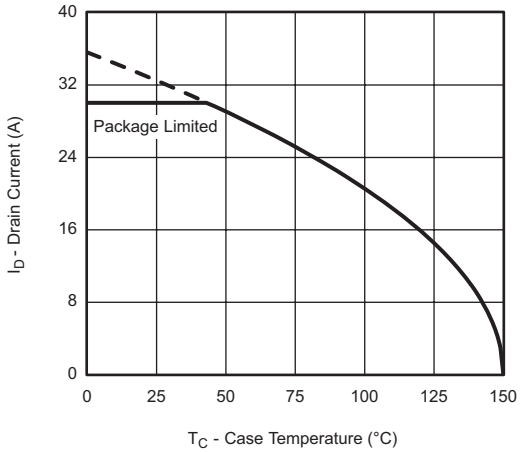
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

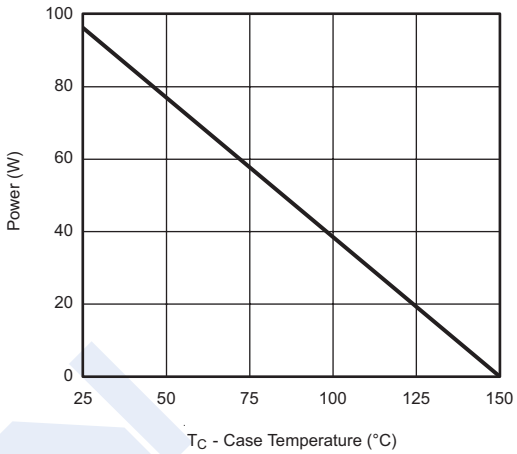
N-Channel MOSFET

SI7738DP (KI7738DP)

■ Typical Characterisitics 25℃ unless otherwise noted

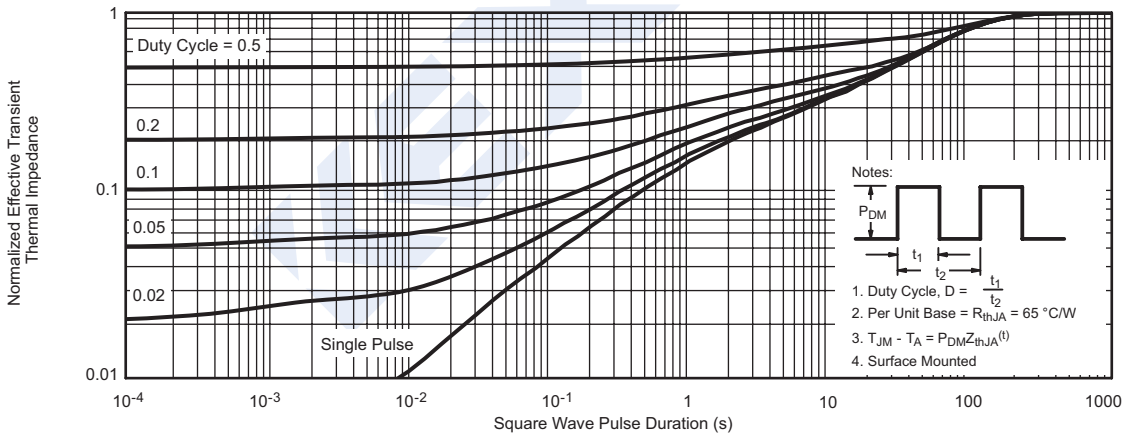


Current Derating*

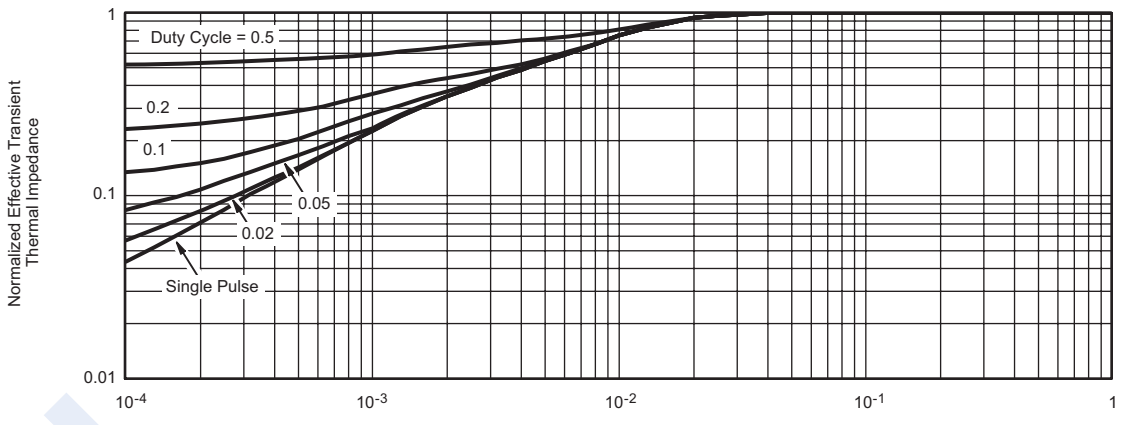


Power Derating

* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Im pedance, Junction-to-Ambient

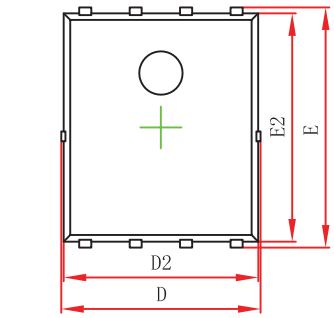


Normalized Thermal Transient Impedance, Junction-to-Case

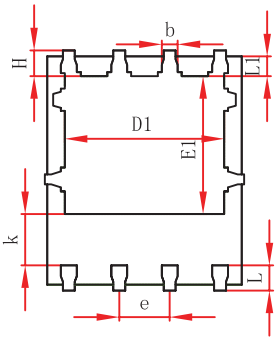
N-Channel MOSFET

SI7738DP (KI7738DP)

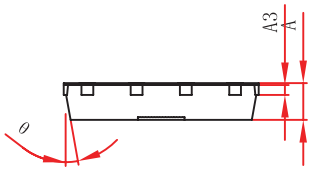
■ DFN5x6-8(PDFNWB5x6-8L) Package Outline Dimensions



Top View
[顶视图]



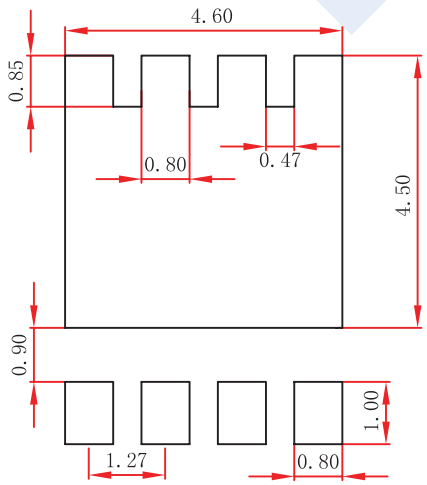
Bottom View
[背视图]



Side View
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

■ DFN5x6-8(PDFNWB5x6-8L) Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.