Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
60	0.060 @ V_{GS} = 10 V	4.8	13
	0.075 @ V_{GS} = 4.5 V	4.3	

FEATURES

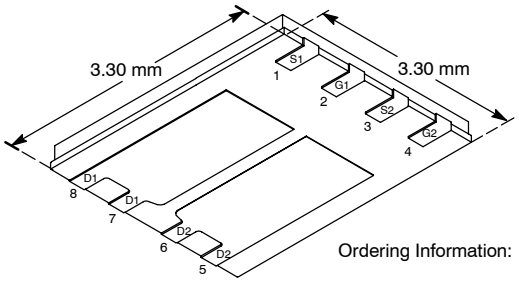
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package, $^1/_3$ the Space of An SO-8 While Thermally Comparable

Pb-free
RoHS COMPLIANT

APPLICATIONS

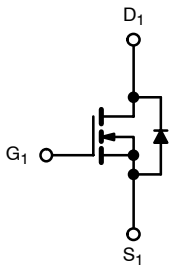
- Synchronous Rectification
- Primary Side Switch

PowerPAK 1212-8

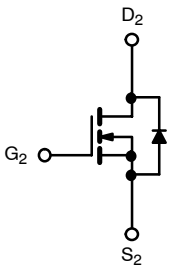


Bottom View

Ordering Information: Si7220DN-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	4.8	3.4	A
	T_A = 70°C		3.8	2.7	
Pulsed Drain Current		I_{DM}	20		
Avalanche Current	L = 0.1 mH	I_{AS}	11		
Single Avalanche Energy		E_{AS}	6.1		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	2.2	1.1	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.6	1.3	W
	T_A = 70°C		1.4	0.69	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C
Soldering Recommendations (Peak Temperature)[b,c]			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	38	48	°C/W
	Steady State		77	94	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	4.3	5.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Solder Profile (http://www.vishay.com/doc?73257). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

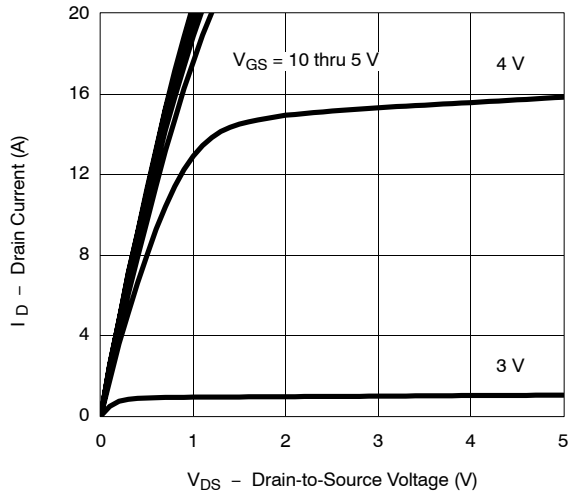
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1		3	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 85°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.8 A		0.048	0.060	Ω
		V_{GS} = 4.5 V, I_D = 4.3 A		0.061	0.075	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 4.8 A		15		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.2 A, V_{GS} = 0 V		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 4.8 A		13	20	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			2.6		
Gate Resistance	R_g	f = 1 MHz		2		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		10	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.2 A, di/dt = 100 A/μs		30	60	

Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

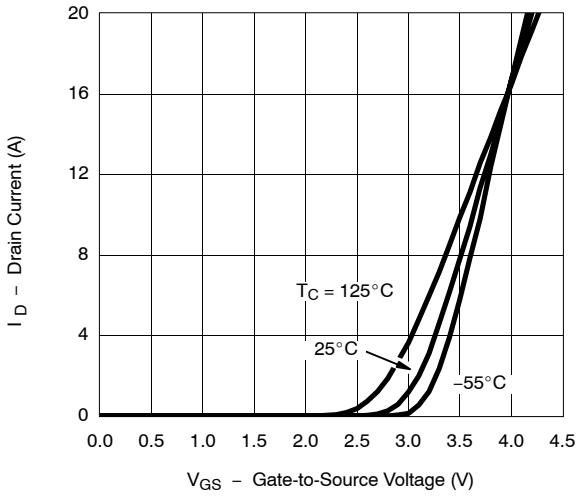
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

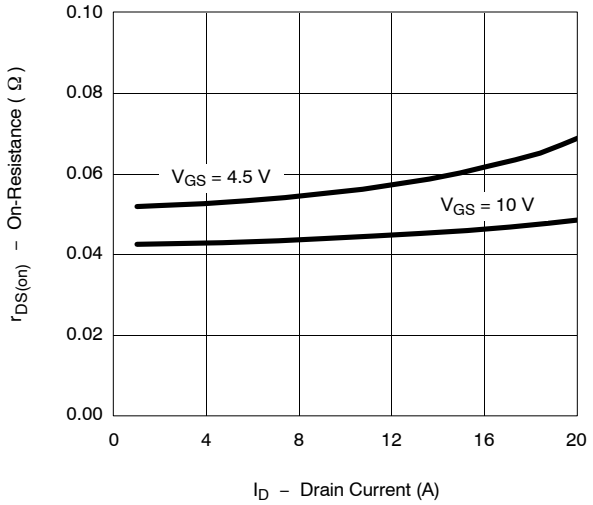


Transfer Characteristics

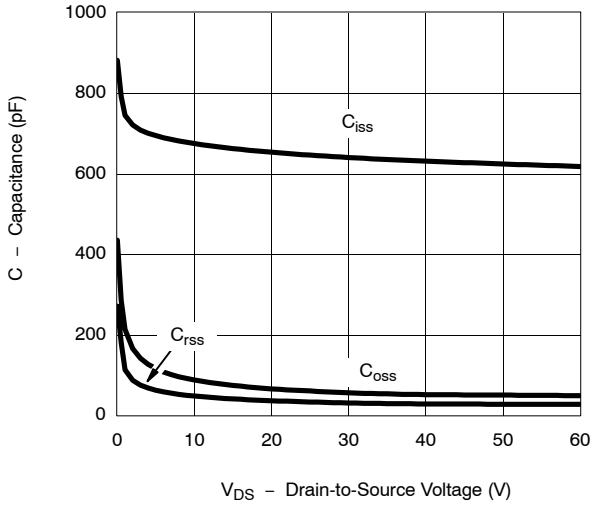


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

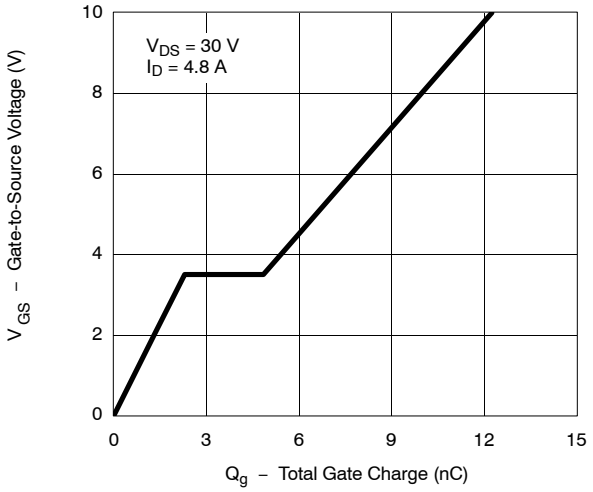
On-Resistance vs. Drain Current



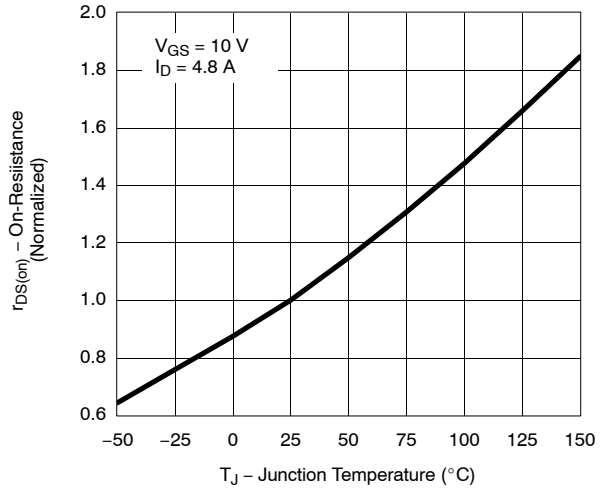
Capacitance



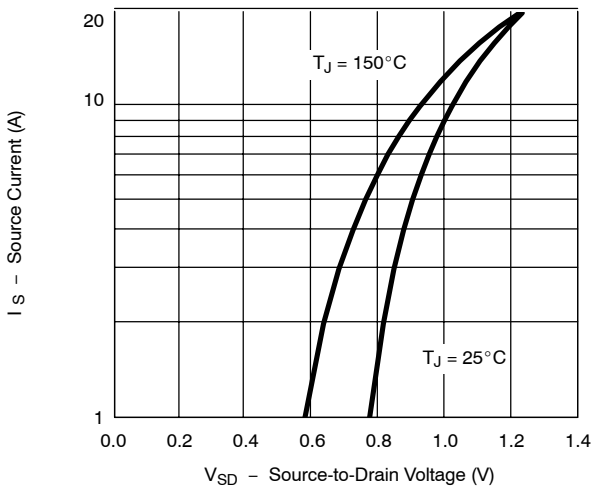
Gate Charge



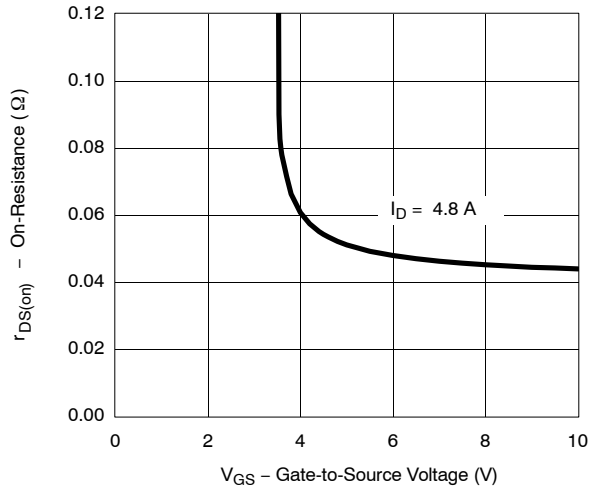
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

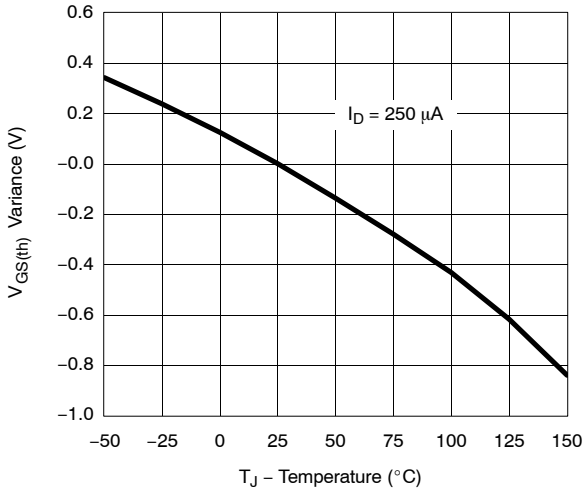


On-Resistance vs. Gate-to-Source Voltage

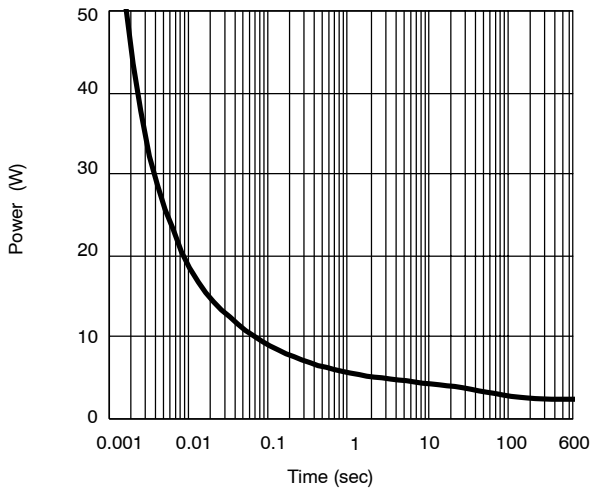


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

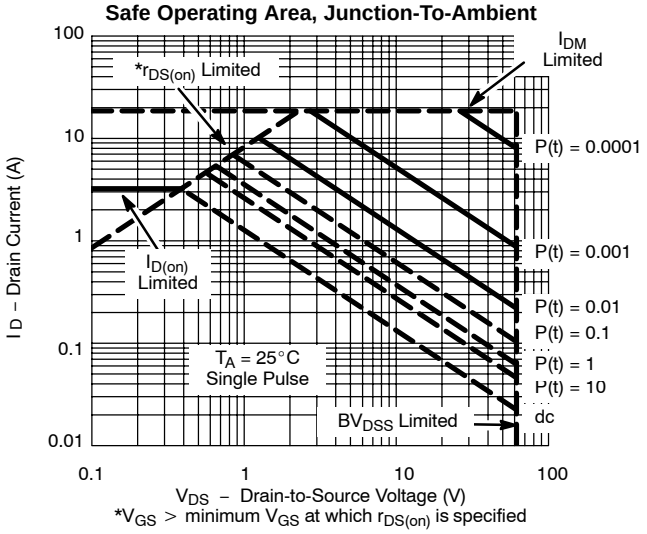
Threshold Voltage



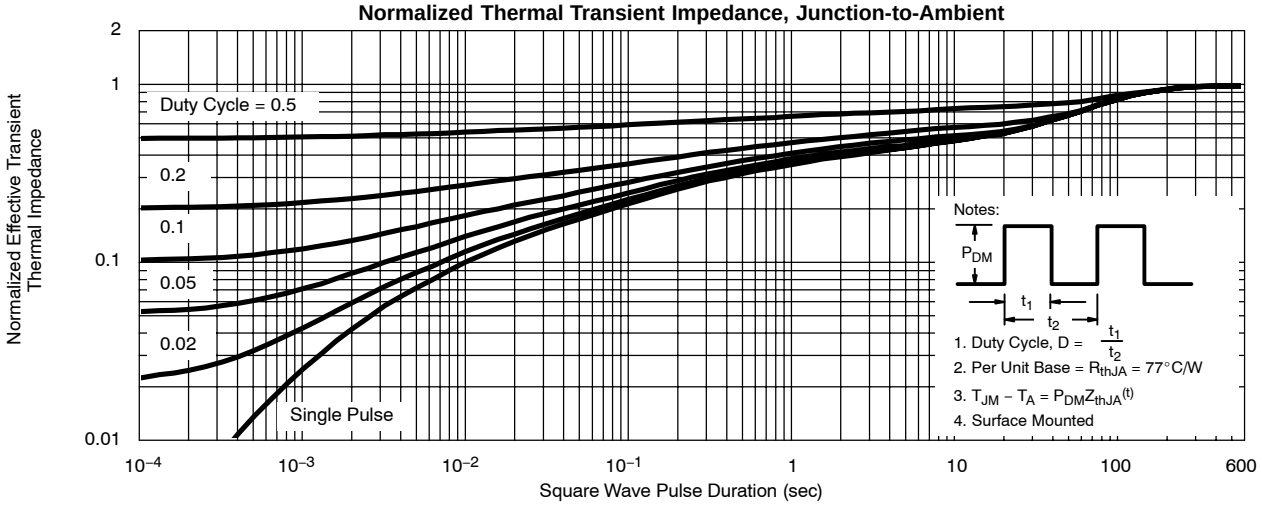
Single Pulse Power



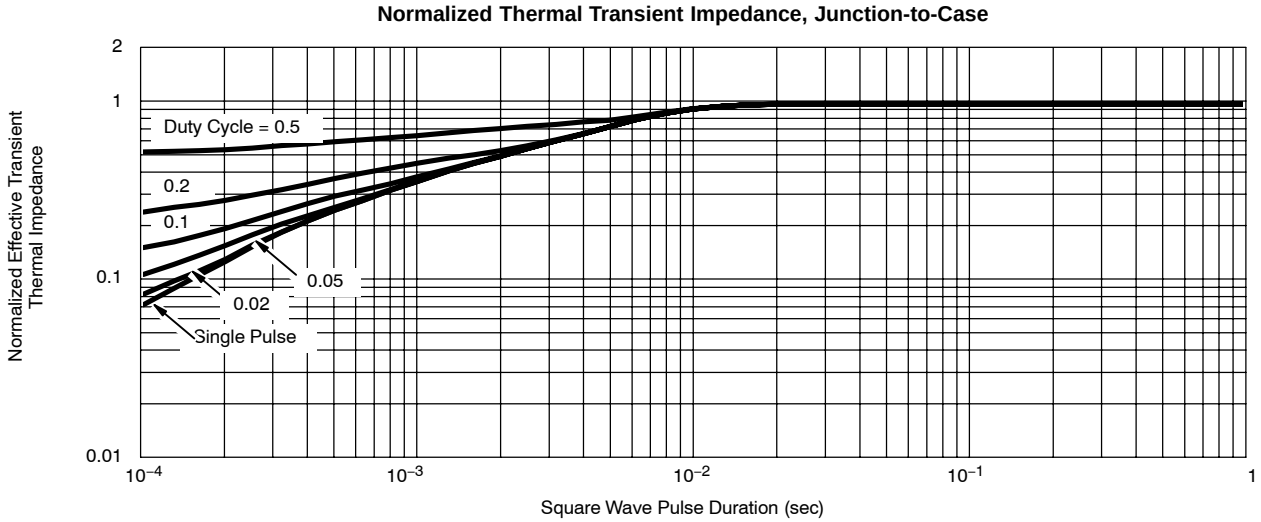
Safe Operating Area, Junction-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



NOTE:

The minimum creepage between D1 and D2 for this 100-V device is 0.2 mm. Please see PowerPAK 1212-8 outline drawing, document # 71656, for more information.

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