Dual P-Channel 12-V (D-S) MOSFET

CHARACTERISTICS

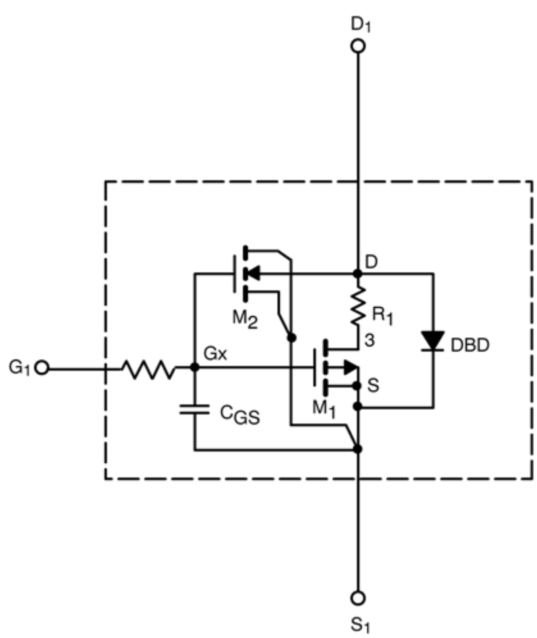
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

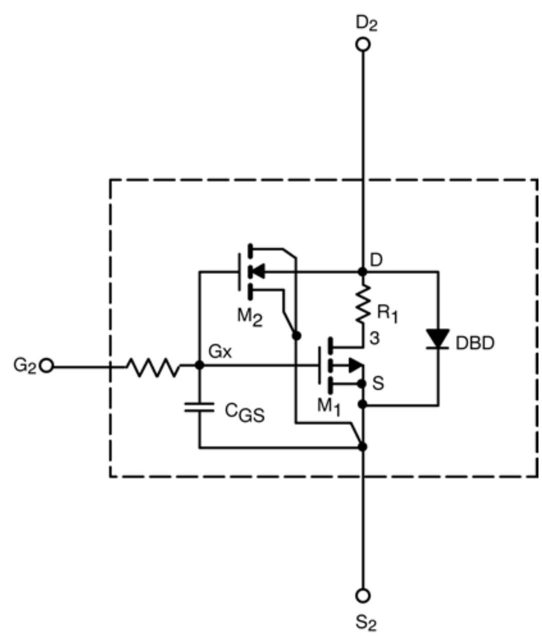
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



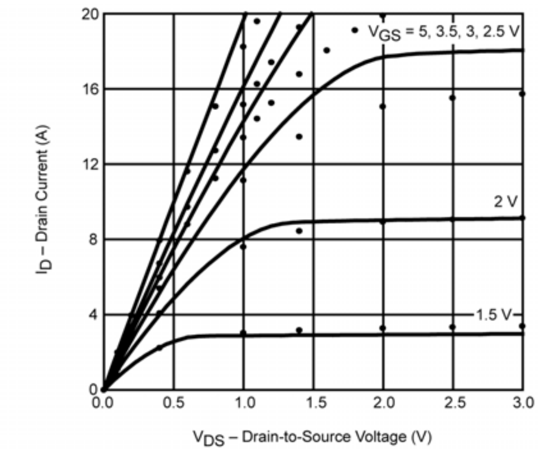


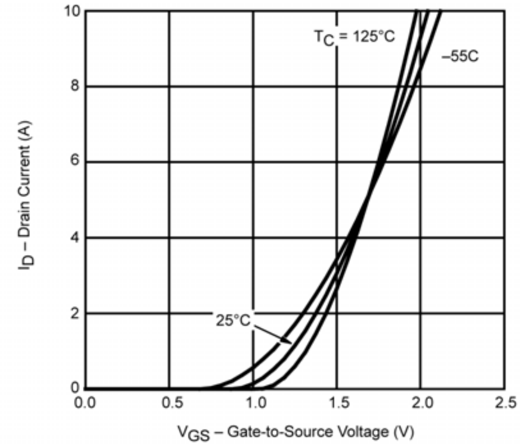
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

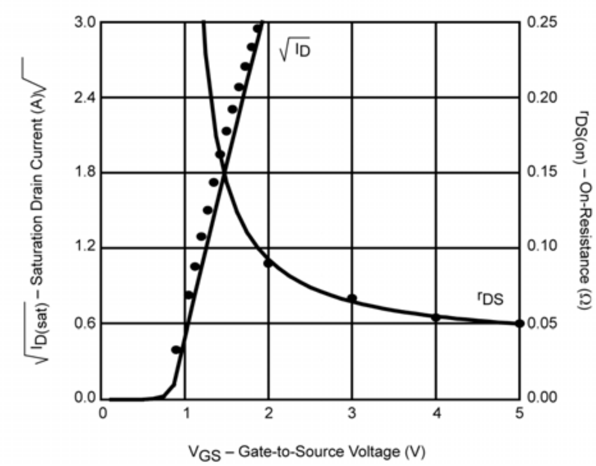
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = –250 µA	0.75		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ –5 V, V_{GS} = –4.5 V	73		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –4.5 V, I_D = –3.6 A	0.052	0.053	Ω
		V_{GS} = –2.5 V, I_D = –3.1 A	0.075	0.073	
		V_{GS} = –1.8 V, I_D = –0.83 A	0.106	0.098	
Forward Transconductance[a]	g_{fs}	V_{DS} = –6 V, I_D = –3.6 A	18	11	S
Diode Forward Voltage[a]	V_{SD}	I_S = –4 A	–0.85	–0.80	V
Dynamic[b]					
Input Capacitance	C_{iss}	V_{DS} = –6 V, V_{GS} = 0 V, f = 1 MHz	624	460	pF
Output Capacitance	C_{oss}		169	170	
Reverse Transfer Capacitance	C_{rss}		118	115	
Total Gate Charge	Q_g	V_{DS} = –6 V, V_{GS} = –8 V, I_D = –5A	8	10	nC
		V_{DS} = –6 V, V_{GS} = –4.5 V, I_D = –5 A	5	6	
Gate-Source Charge	Q_{gs}		0.90	0.90	
Gate-Drain Charge	Q_{gd}		1.65	1.65	

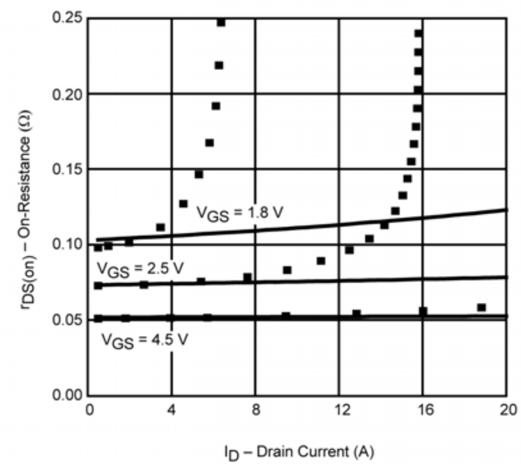
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

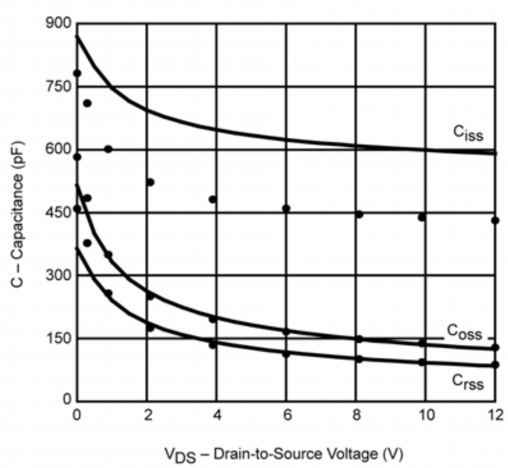
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

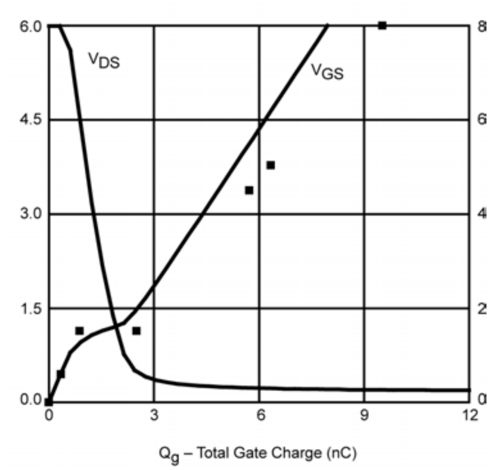












Note: Dots and squares represent measured data.