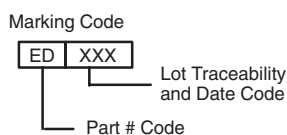
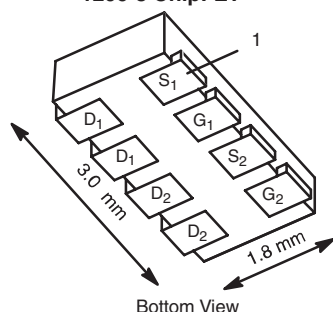


## N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
N-Channel	20	0.052 at V <sub>GS</sub> = 4.5 V	6.1 <sup>a</sup>	3.9 nC
		0.084 at V <sub>GS</sub> = 2.5 V	4.8 <sup>a</sup>	
P-Channel	- 20	0.090 at V <sub>GS</sub> = - 4.5 V	- 4.8 <sup>a</sup>	3.8 nC
		0.160 at V <sub>GS</sub> = - 2.5 V	- 3.6 <sup>a</sup>	

1206-8 ChipFET®



Ordering Information: Si5509DC-T1-E3 (Lead (Pb)-free)  
Si5509DC-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

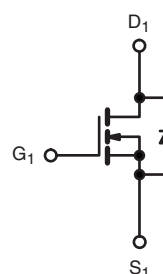
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC



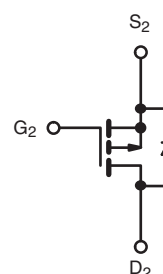
**RoHS**  
COMPLIANT  
**HALOGEN**  
**FREE**  
Available

### APPLICATIONS

- Complementary MOSFET for Portable Devices
- Ideal for Buck-Boost Circuits



N-Channel MOSFET



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS T<sub>A</sub> = 25 °C, unless otherwise noted

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V <sub>DS</sub>	20	- 20	V
Gate-Source Voltage		V <sub>GS</sub>	± 12		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	I <sub>D</sub>	6.1 <sup>a</sup>	- 4.8 <sup>a</sup>	A
	T <sub>C</sub> = 70 °C		4.9 <sup>a</sup>	- 3.8 <sup>a</sup>	
	T <sub>A</sub> = 25 °C		5.0 <sup>b, c</sup>	- 3.9 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		3.9 <sup>b, c</sup>	- 3.1 <sup>b, c</sup>	
Pulsed Drain Current		I <sub>DM</sub>	10	- 15	A
Source Drain Current Diode Current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	3.7	- 3.7	
	T <sub>A</sub> = 25 °C		1.7 <sup>b, c</sup>	- 1.7 <sup>b, c</sup>	
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	4.5	4.5	W
	T <sub>C</sub> = 70 °C		2.88	2.88	
	T <sub>A</sub> = 25 °C		2.1 <sup>b, c</sup>	2.1 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		1.33 <sup>b, c</sup>	1.33 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>			260		

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	N-Channel		P-Channel		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	50	60	50	60	°C/W
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	30	40	30	40	

Notes:

a. Based on T<sub>C</sub> = 25 °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 90 °C/W for both channels.

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

Parameter	Symbol	Test Conditions		Min.	Typ. <sup>a</sup>	Max.	Unit		
Static									
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	20			V		
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	P-Ch	- 20					
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		18.4		mV/°C		
		I <sub>D</sub> = - 250 μA	P-Ch		- 15.1				
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA	N-Ch		- 3.4				
		I <sub>D</sub> = - 250 μA	P-Ch		2.2				
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.7		2	V		
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	P-Ch	- 0.7		- 2			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 12 V	N-Ch P-Ch	 	 	100 - 100	nA		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA		
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V	P-Ch			- 1			
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	N-Ch			10			
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	P-Ch			- 10			
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	10			A		
		V <sub>DS</sub> ≤ - 5 V, V <sub>GS</sub> = - 4.5 V	P-Ch	- 15					
Drain-Source On-State Resistance <sup>b</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5.0 A	N-Ch		0.043	0.052	Ω		
		V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 3.9 A	P-Ch		0.074	0.090			
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.9 A	N-Ch		0.068	0.084			
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 2.9 A	P-Ch		0.128	0.160			
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	N-Ch		10.4		S		
		V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 3.9 A	P-Ch		8.2				
Dynamic <sup>a</sup>									
Input Capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch P-Ch	 	455 300	 	pF		
Output Capacitance	C <sub>oss</sub>		N-Ch P-Ch	 	85 95	 			
Reverse Transfer Capacitance	C <sub>rss</sub>	P-Channel V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	N-Ch P-Ch	 	50 65	 			
Total Gate Charge	Q <sub>g</sub>		V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 4.0 A	N-Ch		4.4		6.6	nC
		V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 5 V, I <sub>D</sub> = - 3.9 A	P-Ch		4.1	6.2			
		N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 4.0 A	N-Ch		3.8	5.7			
			P-Ch		3.9	5.9			
Gate-Source Charge	Q <sub>gs</sub>	P-Channel V <sub>DS</sub> = - 10 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 3.9 A	N-Ch P-Ch	 	0.9 0.7	 			
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch P-Ch	 	0.95 1.25	 			
			Gate Resistance	R <sub>g</sub>	f = 1 MHz	N-Ch P-Ch	 	1.9 8	

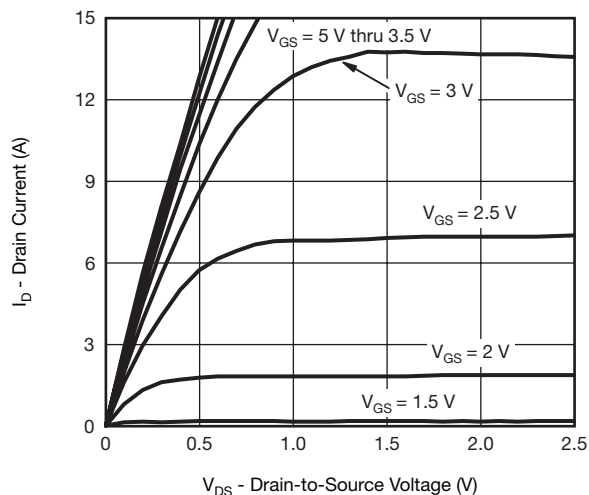
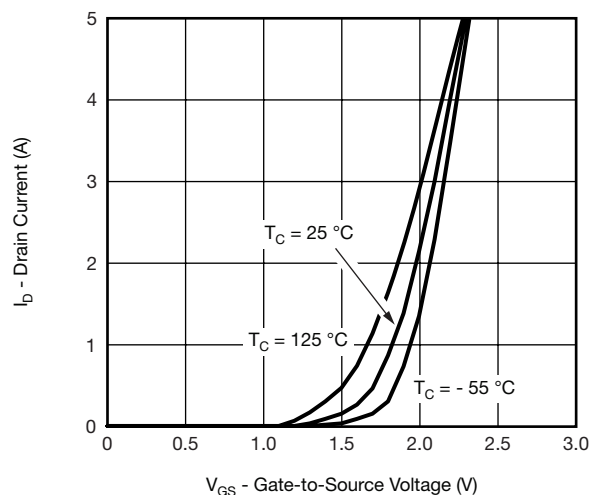
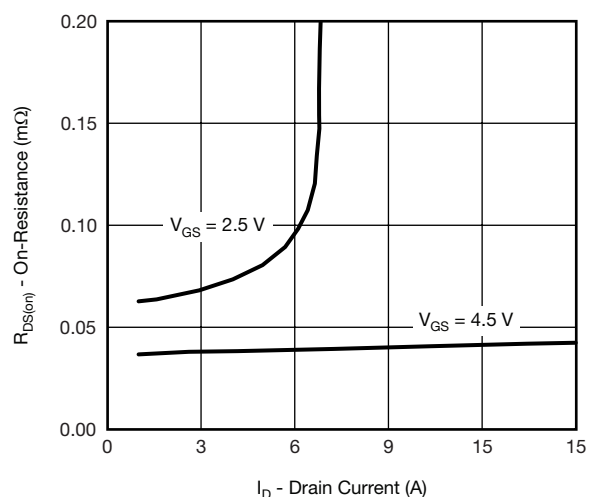
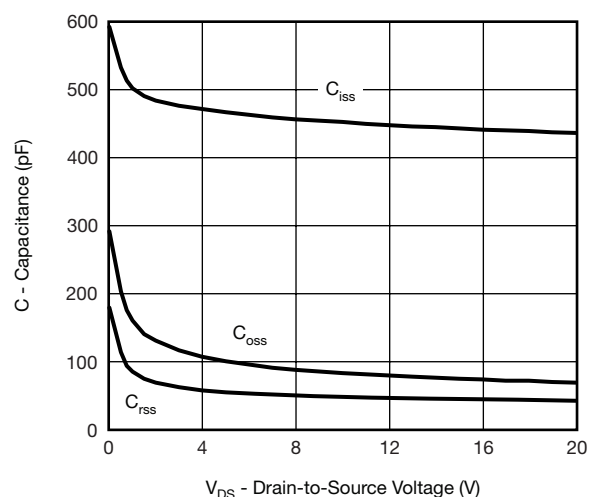
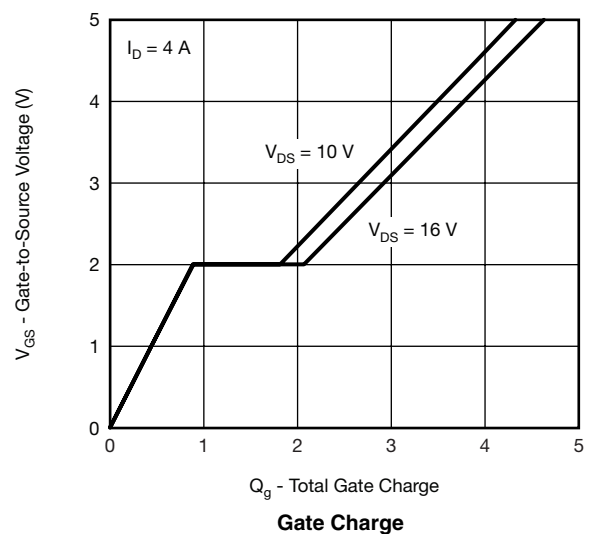
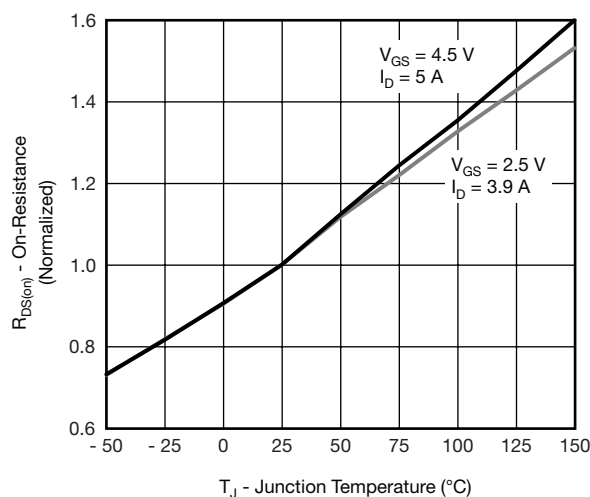
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted								
Parameter	Symbol	Test Conditions		Min.	Typ. <sup>a</sup>	Max.	Unit	
Dynamic <sup>a</sup>								
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}$ , $R_L = 2.5\text{ }\Omega$ $I_D \cong 4.0\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch		6	9	ns	
			P-Ch		8	12		
Rise Time	$t_r$		N-Ch		95	143		
			P-Ch		75	113		
Turn-Off Delay Time	$t_{d(off)}$	P-Channel $V_{DD} = -10\text{ V}$ , $R_L = 3.2\text{ }\Omega$ $I_D \cong -3.14\text{ A}$ , $V_{GEN} = -4.5\text{ V}$ , $R_g = 1\text{ }\Omega$	N-Ch		12	18		
			P-Ch		25	38		
Fall Time	$t_f$		N-Ch		6	9		
			P-Ch		60	90		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^{\circ}\text{C}$	N-Ch			3.75	A	
			P-Ch			- 3.75		
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		N-Ch			10		
			P-Ch			- 15		
Body Diode Voltage	$V_{SD}$	$I_S = 2.4\text{ A}$ , $V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V	
		$I_S = -1.5\text{ A}$ , $V_{GS} = 0\text{ V}$	P-Ch		- 0.8	- 1.2		
Body Diode Reverse Recovery Time	$t_{rr}$	N-Channel $I_F = 2.4\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		12	18	ns	
			P-Ch		18	27		
Body Diode Reverse Recovery Charge	$Q_{rr}$		P-Channel $I_F = -1.5\text{ A}$ , $dI/dt = -100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^{\circ}\text{C}$	N-Ch		5	8	nC
				P-Ch		8	12	
Reverse Recovery Fall Time	$t_a$			N-Ch		7.5		ns
				P-Ch		14		
Reverse Recovery Rise Time	$t_b$		N-Ch		4.5			
			P-Ch		4			

Notes:

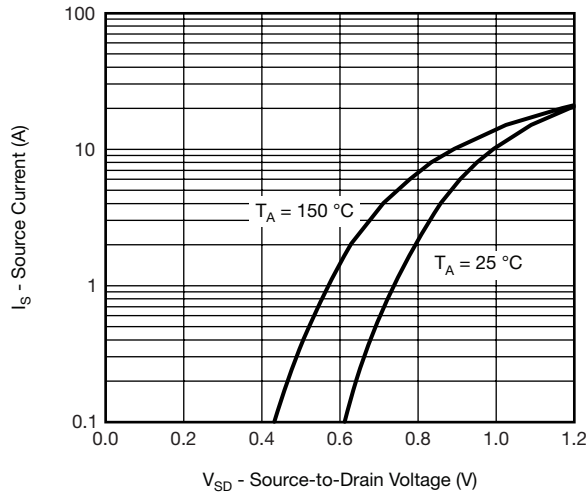
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\text{ }\%$ .

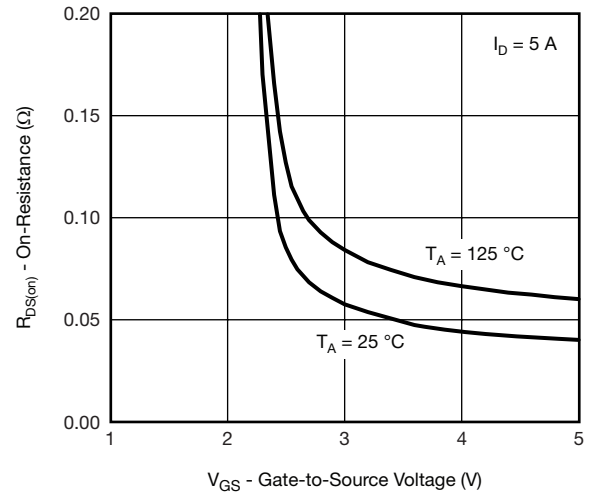
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

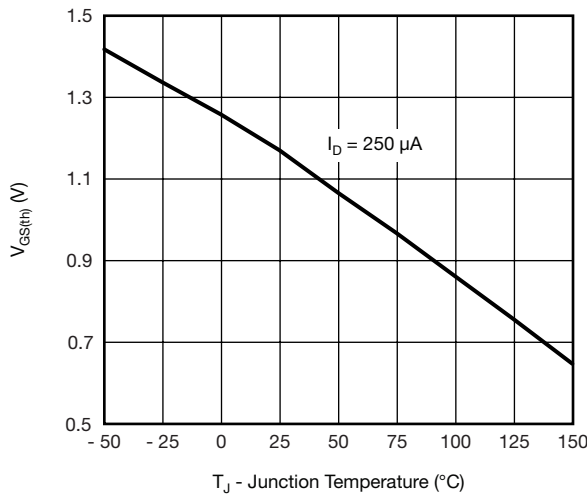
## N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



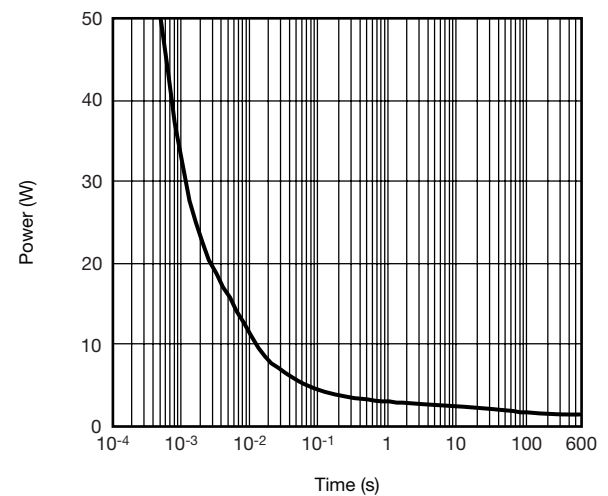
Source-Drain Diode Forward Voltage



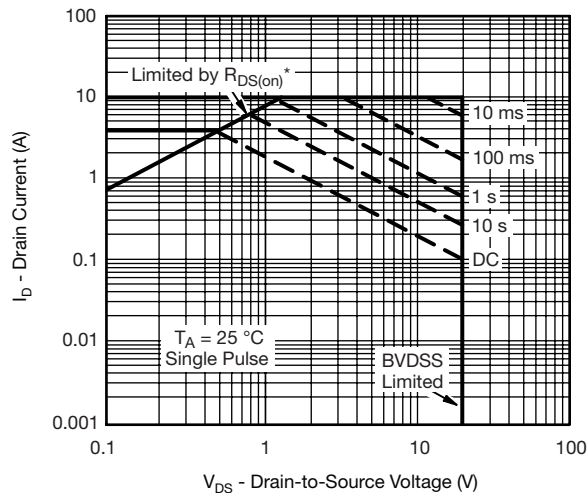
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

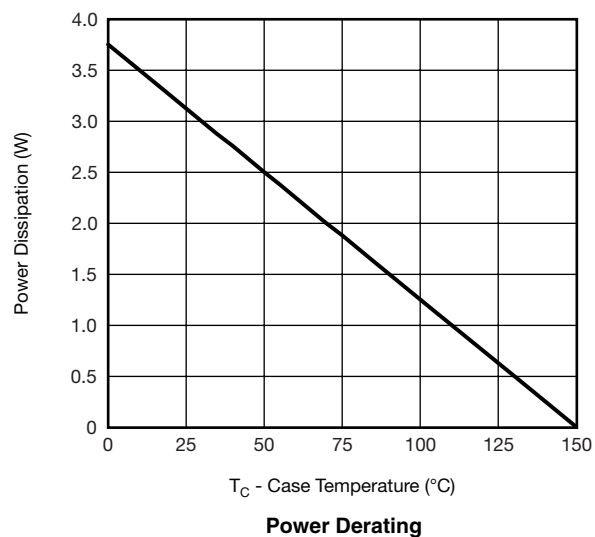
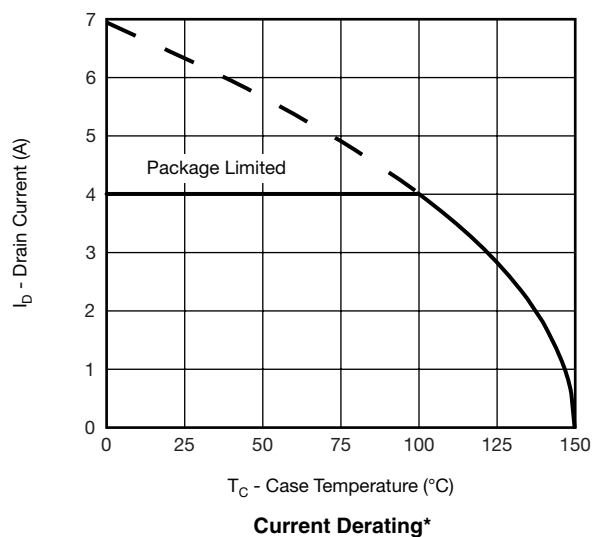


Single Pulse Power



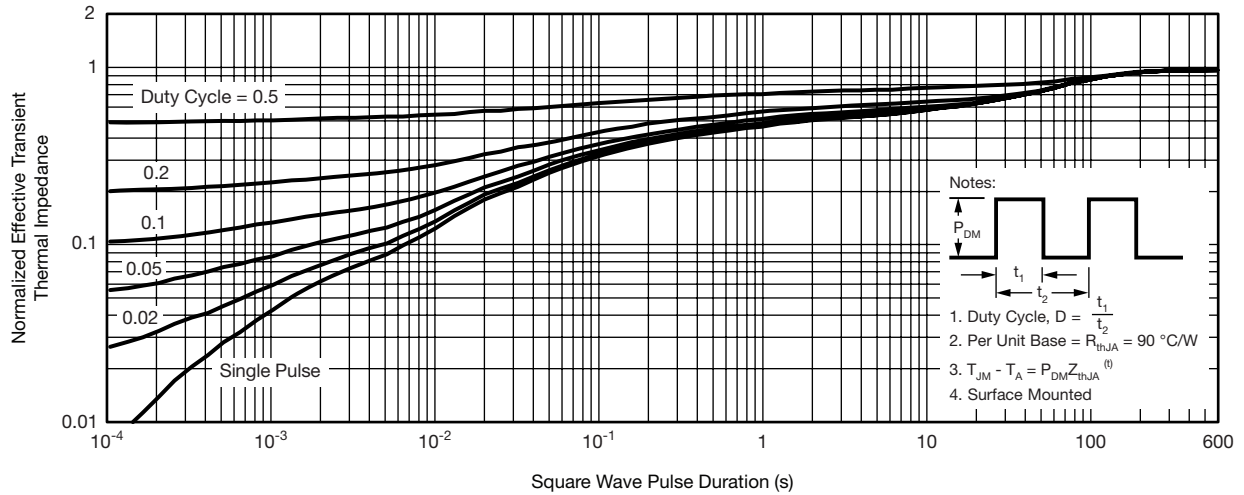
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Case

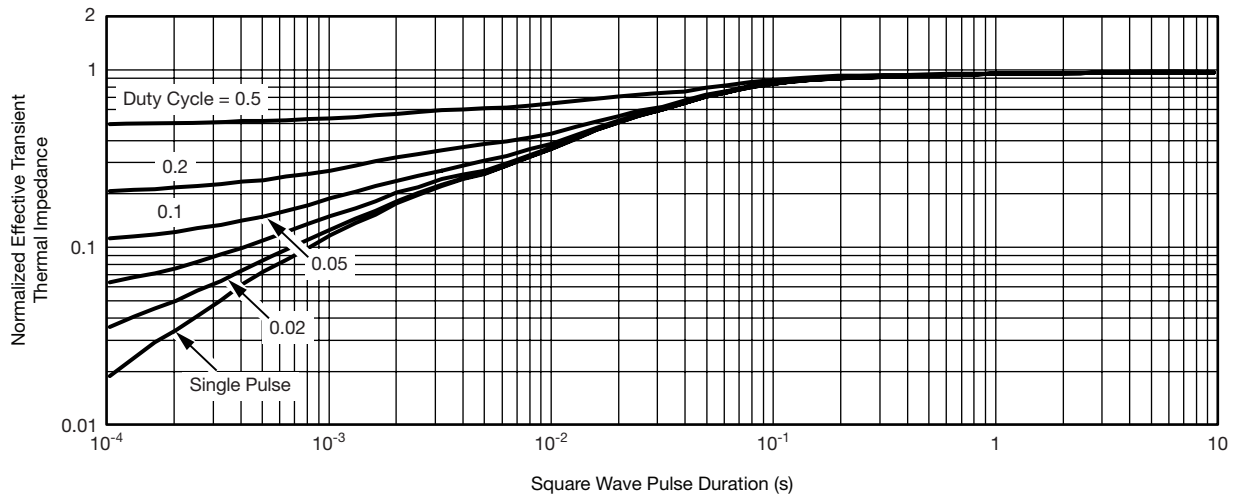
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

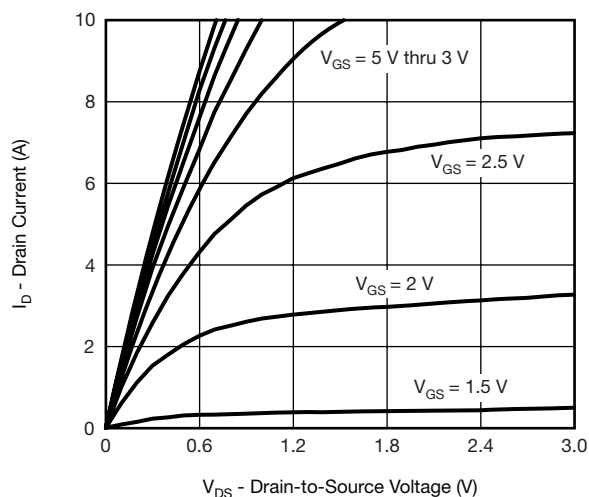
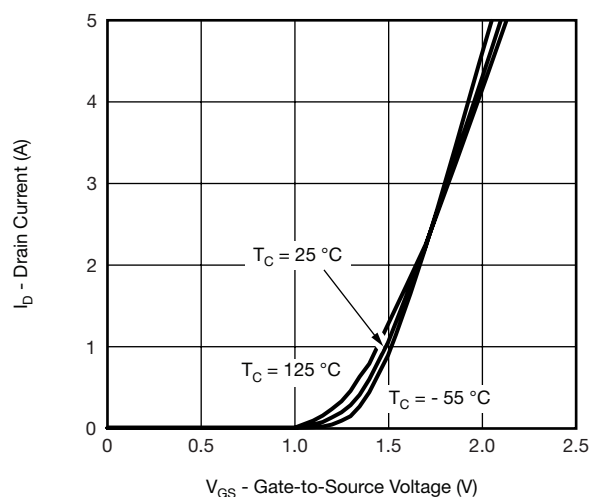
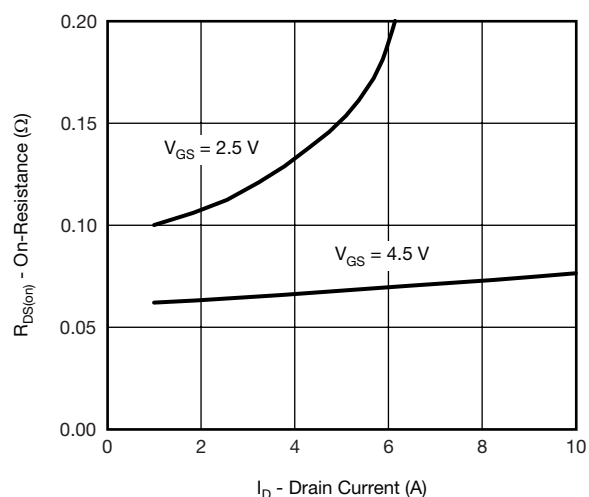
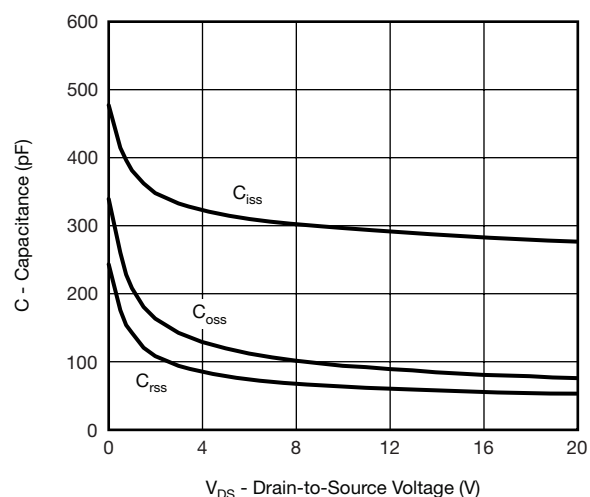
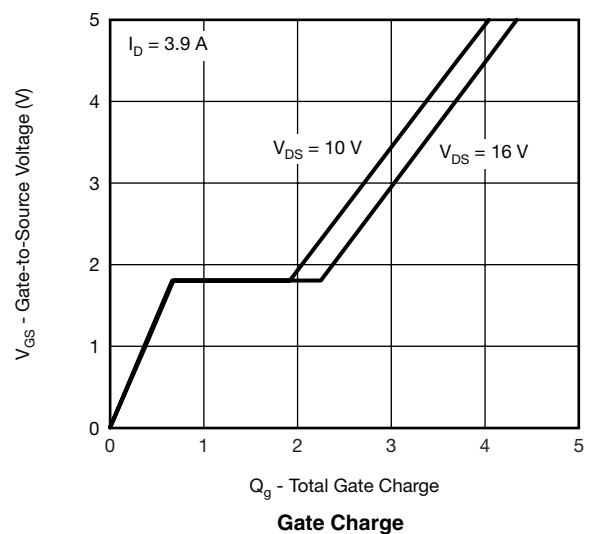
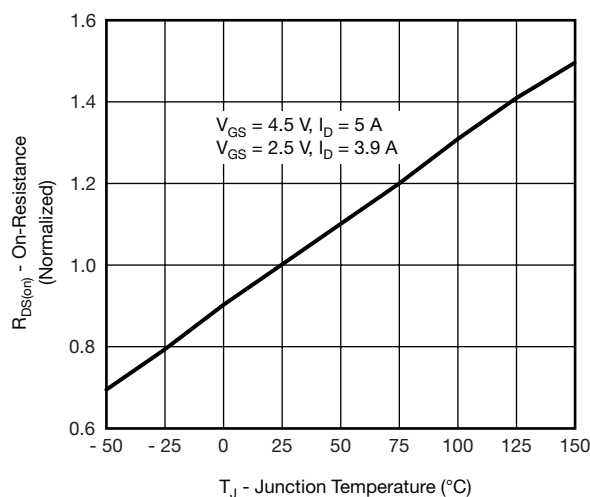
**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

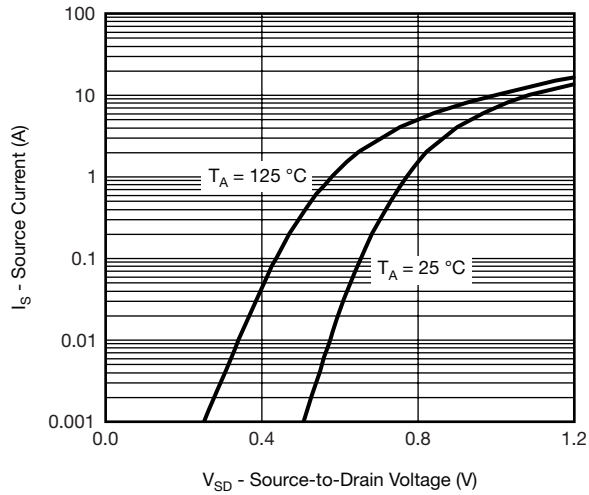


**Normalized Thermal Transient Impedance, Junction-to-Foot**

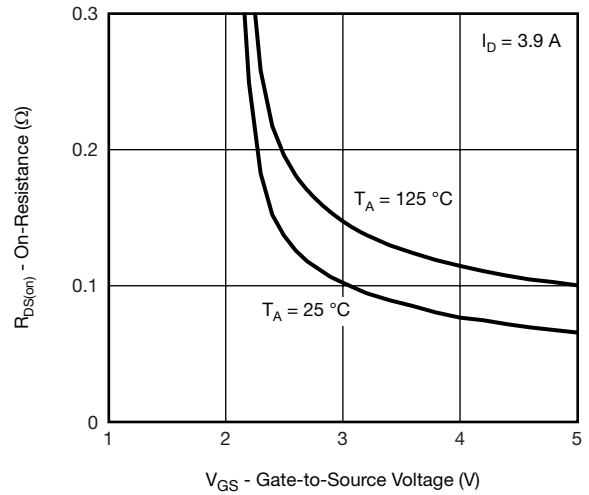
**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**



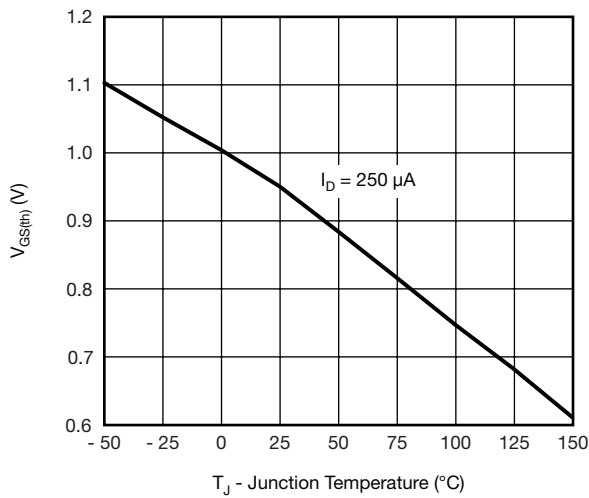
## P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



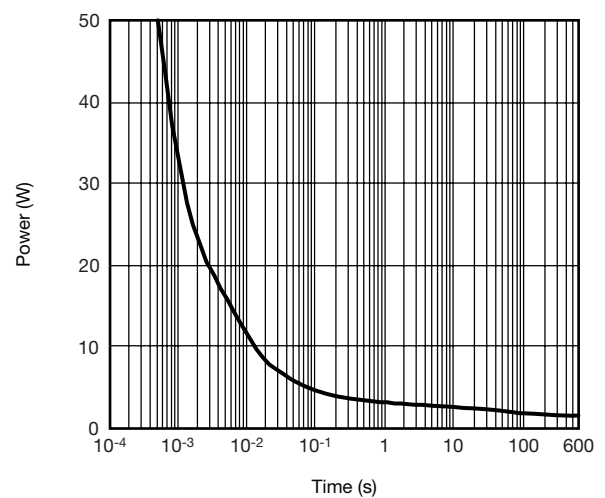
Source-Drain Diode Forward Voltage



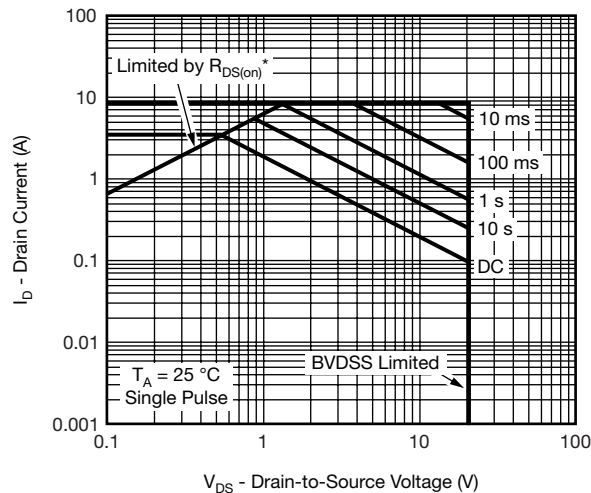
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

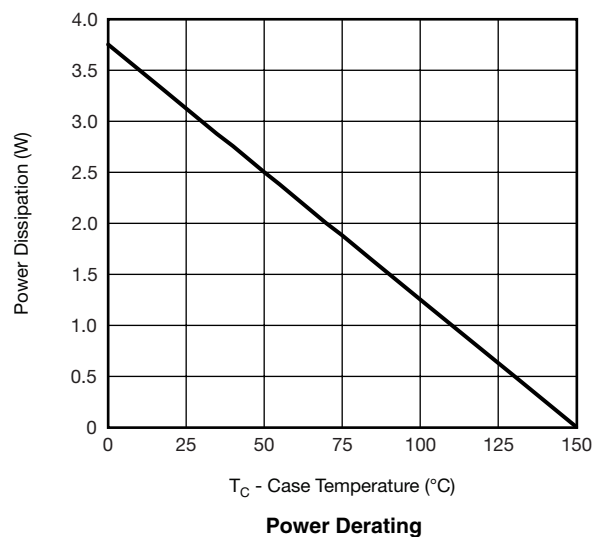
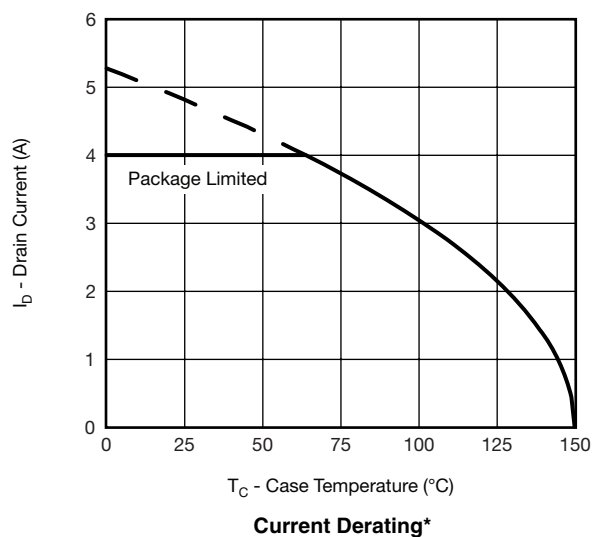


Single Pulse Power



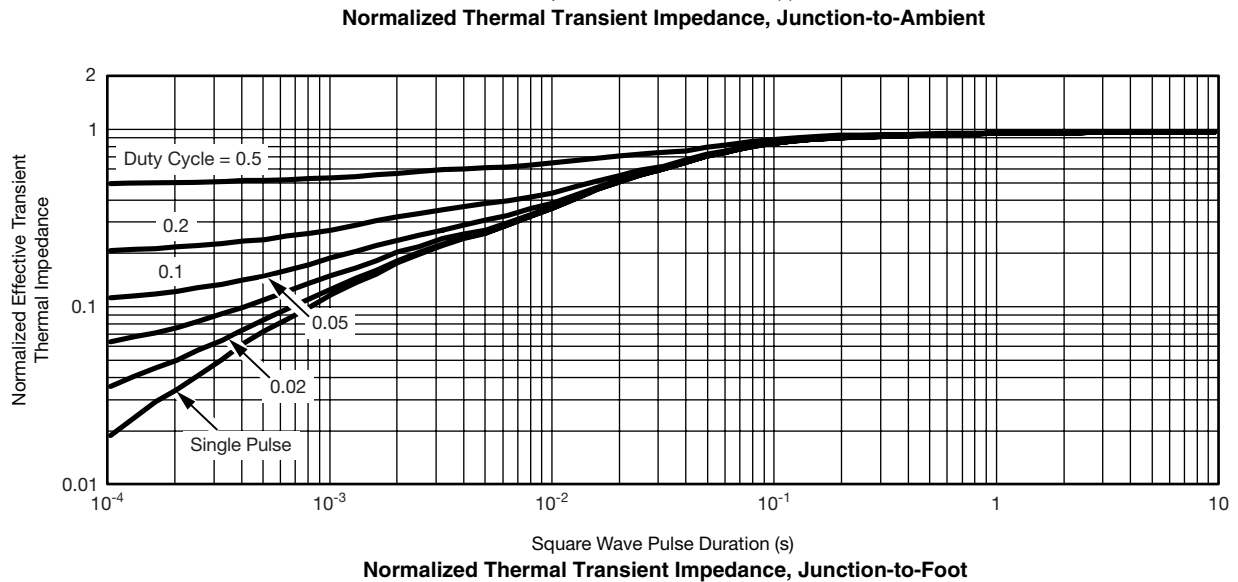
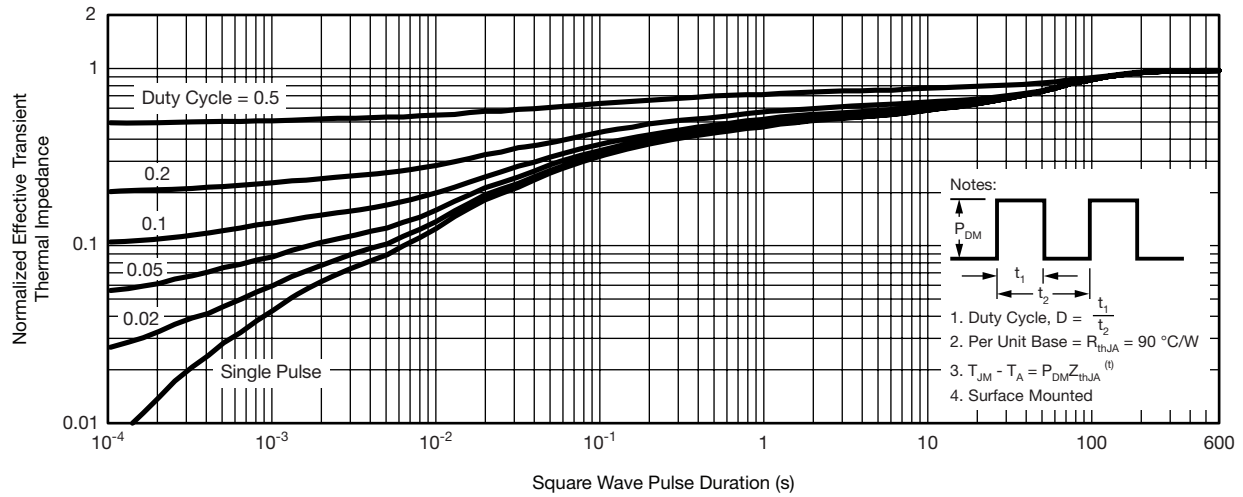
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Case

**N-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**P-CHANNEL TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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