

## P-Channel 12-V (D-S) MOSFET

### PRODUCT SUMMARY

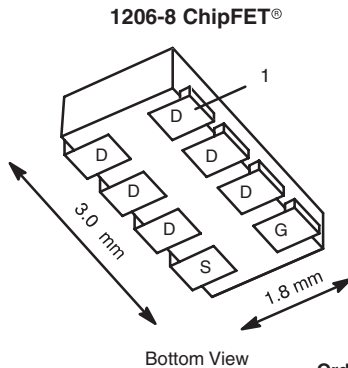
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
- 12	0.028 at $V_{GS} = - 4.5$ V	- 6	15.5 nC
	0.039 at $V_{GS} = - 2.5$ V	- 6	
	0.054 at $V_{GS} = - 1.8$ V	- 6	

### FEATURES

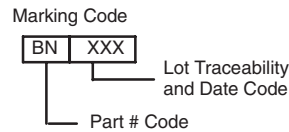
- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET<sup>®</sup> Power MOSFET: 1.8 V Rated



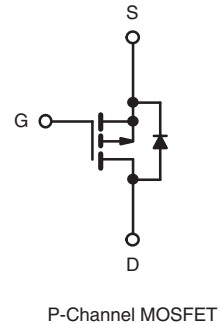
**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available



Bottom View



**Ordering Information:** Si5475BDC-T1-E3 (Lead (Pb)-free)  
Si5475BDC-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

### ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	- 12	V
Gate-Source Voltage	$V_{GS}$	$\pm 8$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	$I_{DM}$	- 20	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b, f</sup>	$R_{thJA}$	40	50	°C/W
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	15	20	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$  s.
- See Solder Profile ([www.vishay.com/ppg?73257](http://www.vishay.com/ppg?73257)). The 1206 ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 95 °C/W.

SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = - 250 μA	- 12			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = - 250 μA		- 7		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			2.5		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = - 250 μA	- 0.45		- 1.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 12 V, V <sub>GS</sub> = 0 V			- 1	μA
		V <sub>DS</sub> = - 12 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			- 5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = - 4.5 V	- 20			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 5.6 A		0.023	0.028	Ω
		V <sub>GS</sub> = - 2.5 V, I <sub>D</sub> = - 4.7 A		0.032	0.039	
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 1.9 A		0.044	0.054	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = - 6 V, I <sub>D</sub> = - 6.9 A		22		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = - 6 V, V <sub>GS</sub> = 0 V, f = 1 MHz		1400		pF
Output Capacitance	C <sub>oss</sub>			370		
Reverse Transfer Capacitance	C <sub>rss</sub>			260		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = - 6 V, V <sub>GS</sub> = - 8 V, I <sub>D</sub> = - 6 A		26	40	nC
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = - 6 V, V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 6 A		15.5	24	
Gate-Drain Charge	Q <sub>gd</sub>			2.1		
				4.0		
Gate Resistance	R <sub>g</sub>	f = 1 MHz		9		Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 6 V, R <sub>L</sub> = 0.97 Ω I <sub>D</sub> ≅ - 6.2 A, V <sub>GEN</sub> = - 4.5 V, R <sub>g</sub> = 1 Ω		10	15	ns
Rise Time	t <sub>r</sub>			38	60	
Turn-Off DelayTime	t <sub>d(off)</sub>			62	95	
Fall Time	t <sub>f</sub>			70	105	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = - 6 V, R <sub>L</sub> = 0.97 Ω I <sub>D</sub> ≅ - 6.2 A, V <sub>GEN</sub> = - 8 V, R <sub>g</sub> = 1 Ω		5	10	
Rise Time	t <sub>r</sub>			15	25	
Turn-Off DelayTime	t <sub>d(off)</sub>			65	100	
Fall Time	t <sub>f</sub>			72	110	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			- 5.2	A
Pulse Diode Forward Current	I <sub>SM</sub>				- 20	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 6.2 A, V <sub>GS</sub> = 0 V		- 0.9	- 1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 6.2 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		45	70	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			27	42	nC
Reverse Recovery Fall Time	t <sub>a</sub>			15		ns
Reverse Recovery Rise Time	t <sub>b</sub>			30		

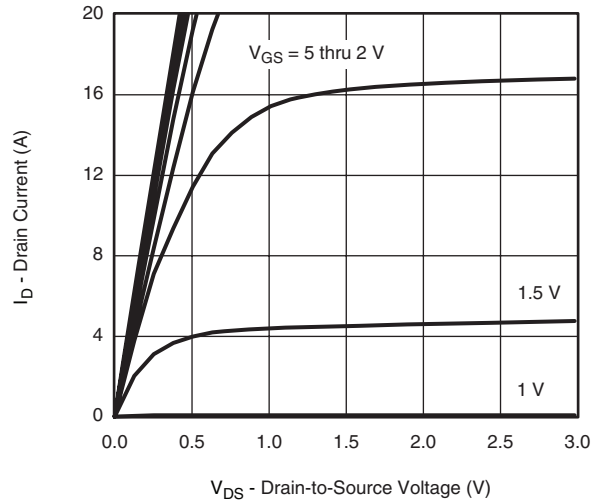
Notes:

a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

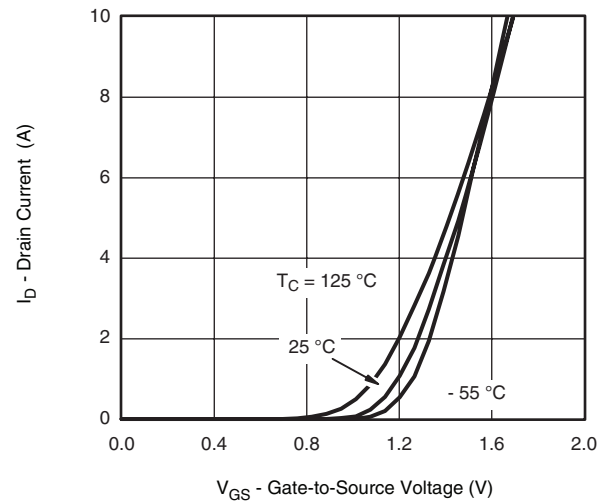
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

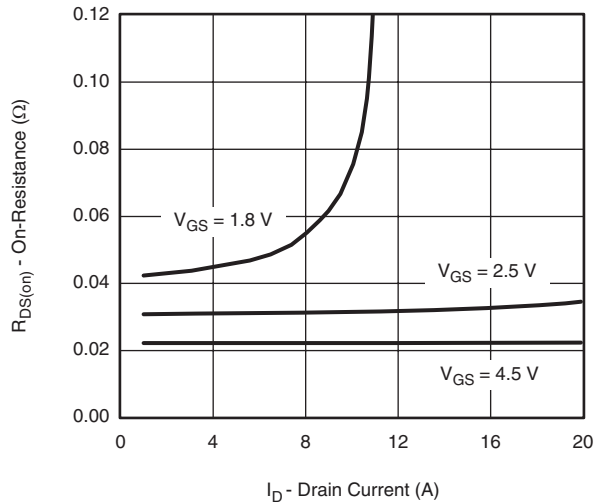
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



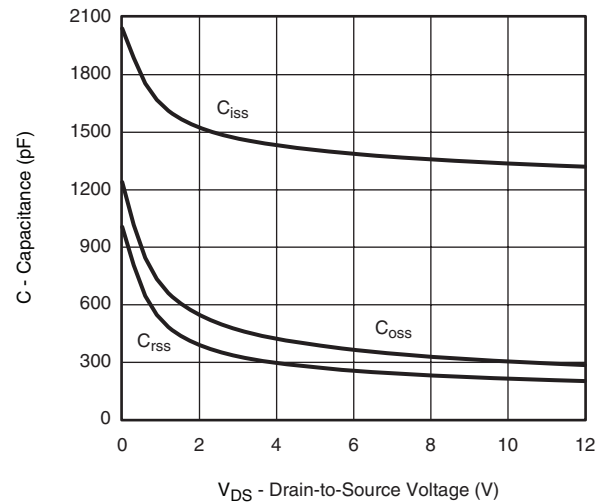
Output Characteristics



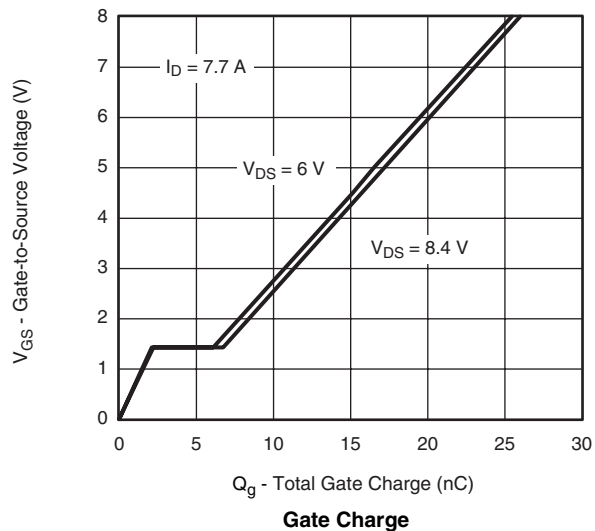
Transfer Characteristics



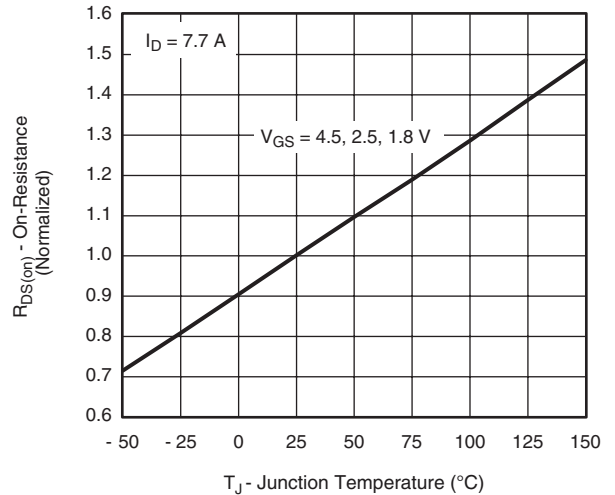
On-Resistance vs. Drain Current and Gate Voltage



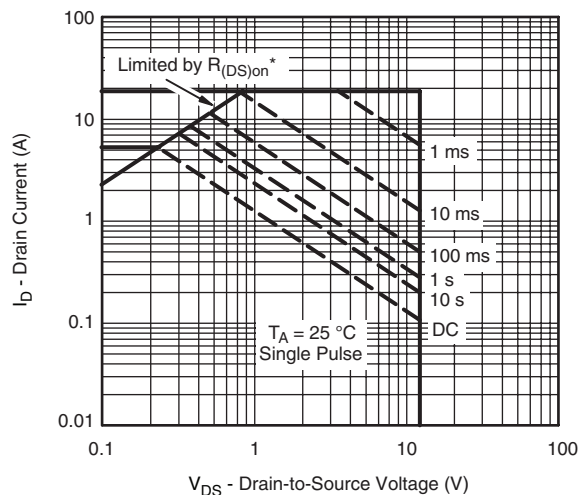
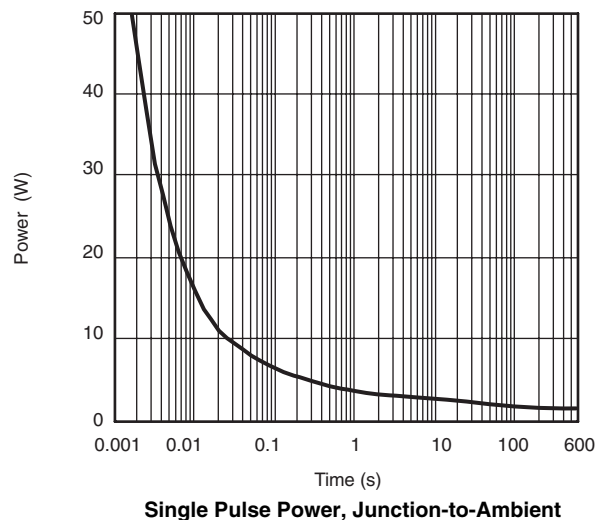
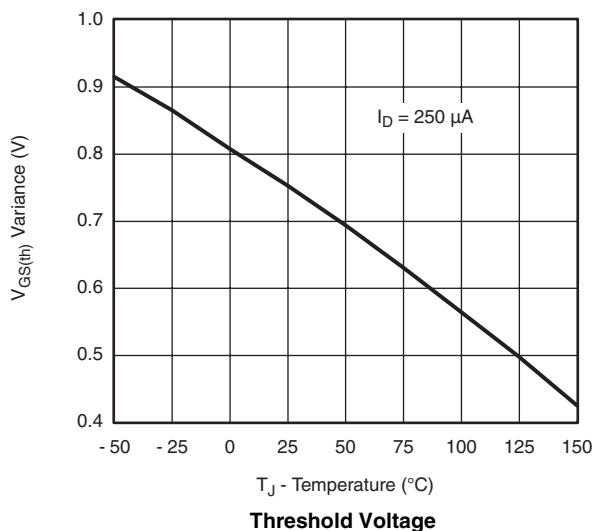
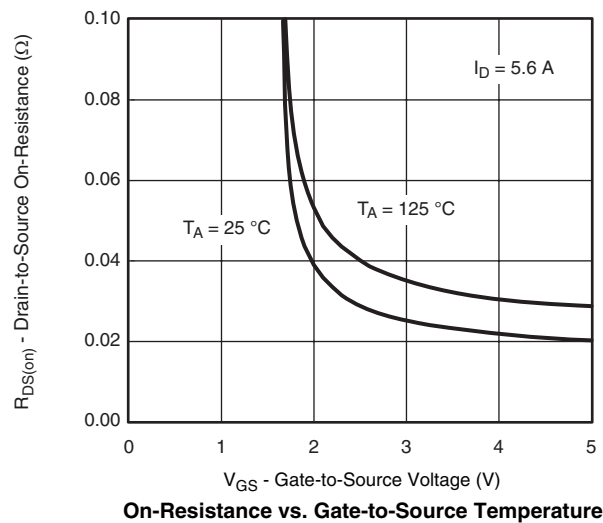
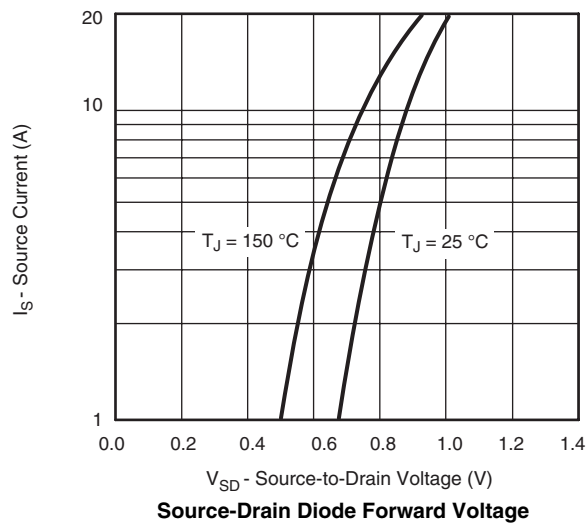
Capacitance



Gate Charge



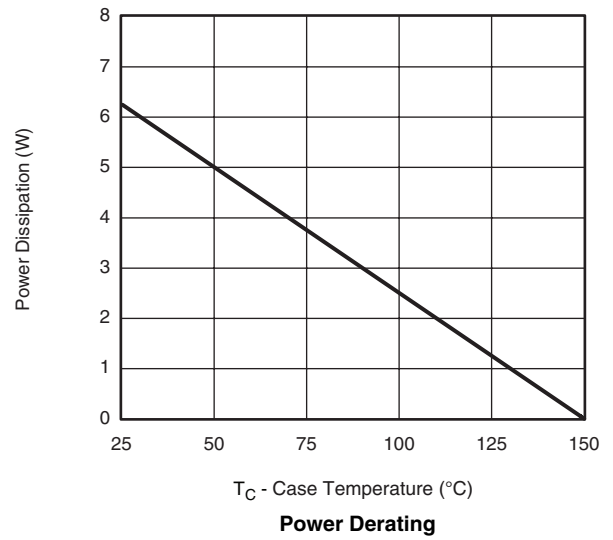
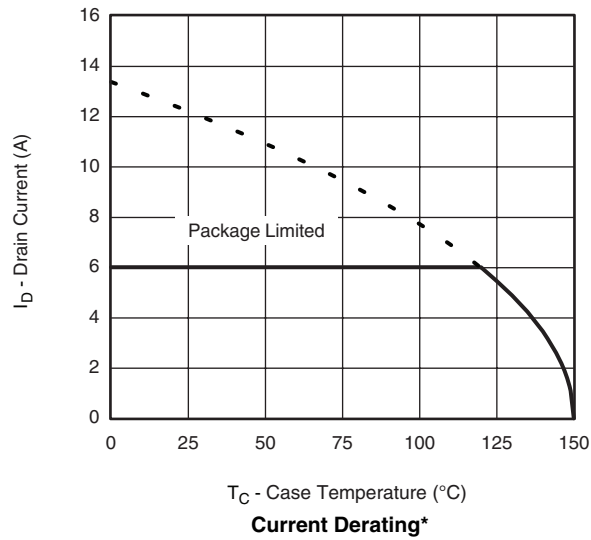
On-Resistance vs. Junction Temperature

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

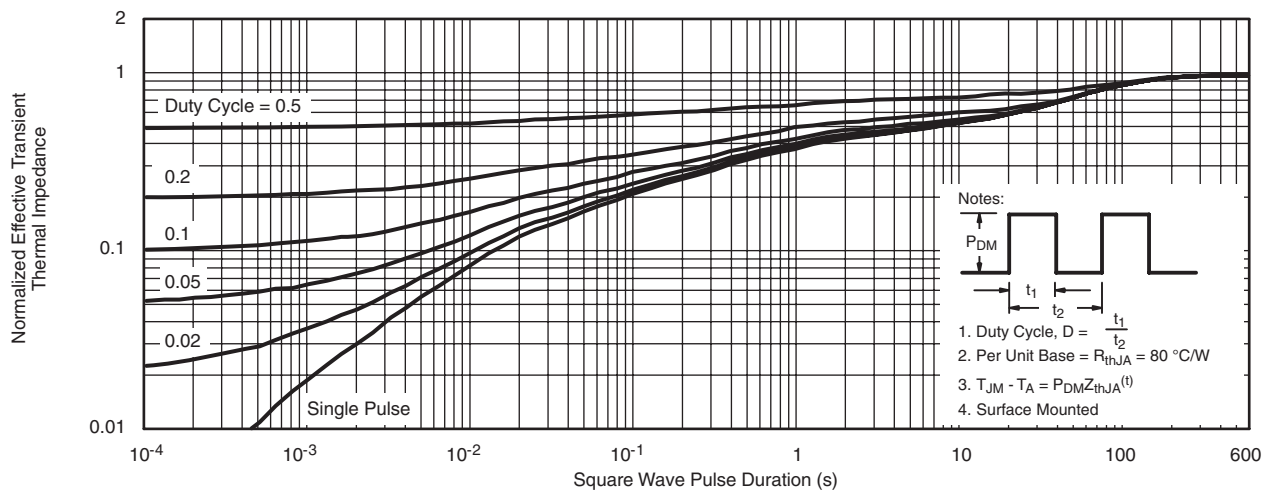
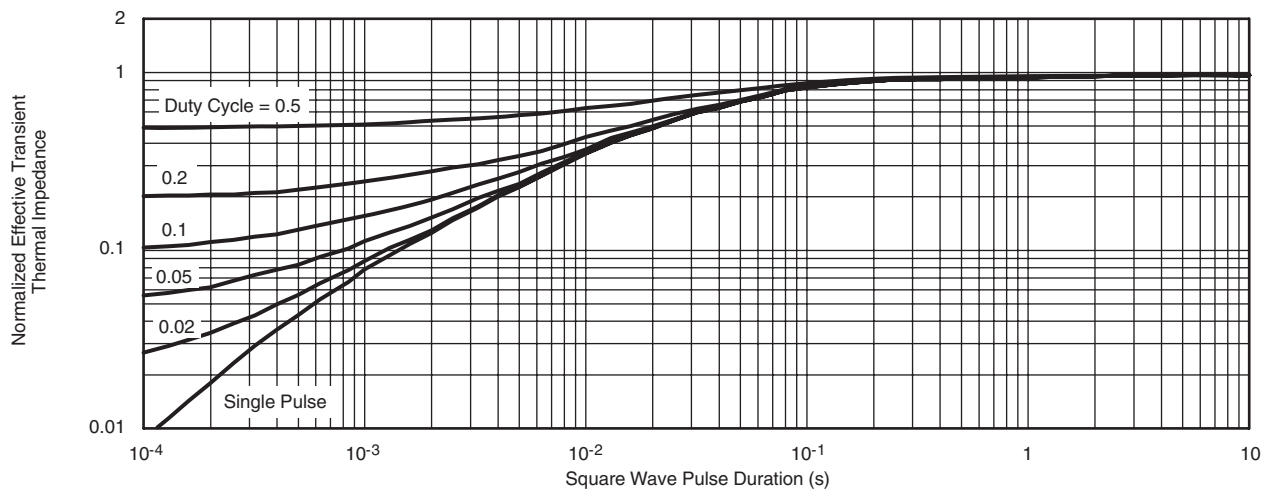
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



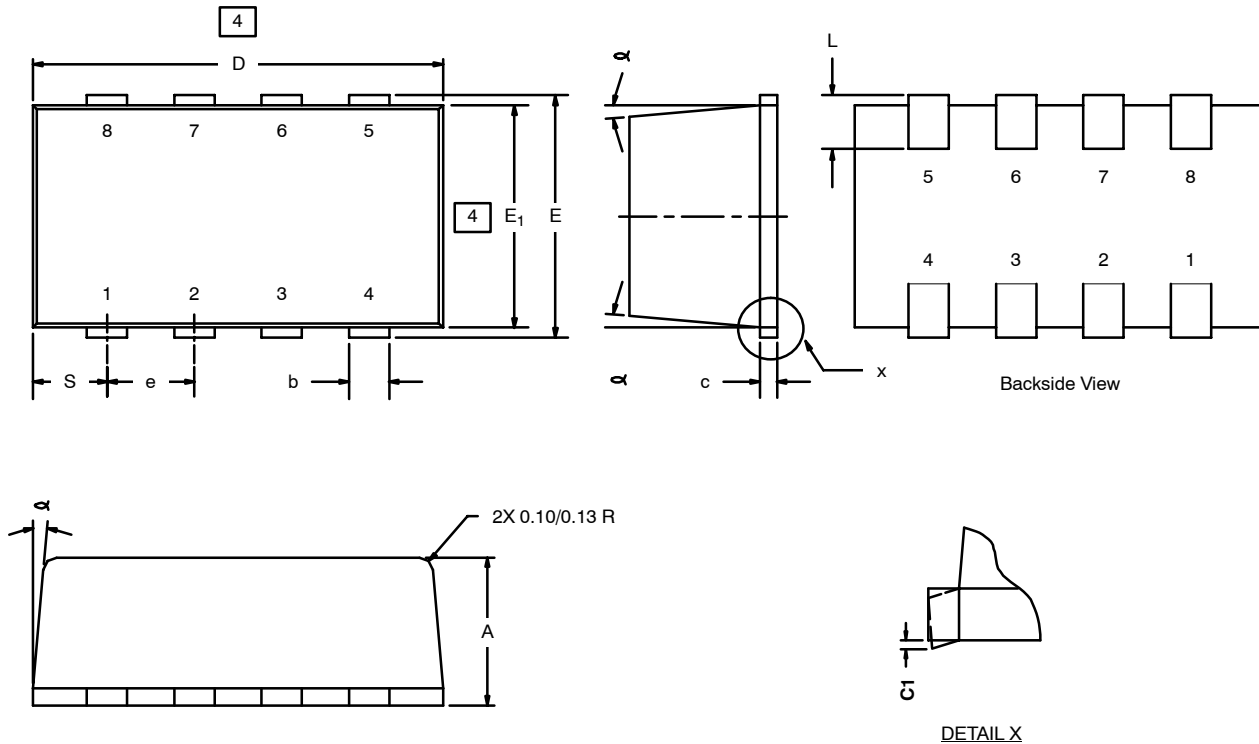
\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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### 1206-8 ChipFET®



#### NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E <sub>1</sub>	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04						
DWG: 5547						

# Single-Channel 1206-8 ChipFET® Power MOSFET Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

New Vishay Siliconix ChipFETs in the leadless 1206-8 package feature the same outline as popular 1206-8 resistors and capacitors but provide all the performance of true power semiconductor devices. The 1206-8 ChipFET has the same footprint as the body of the LITTLE FOOT® TSOP-6, and can be thought of as a leadless TSOP-6 for purposes of visualizing board area, but its thermal performance bears comparison with the much larger SO-8.

This technical note discusses the single-channel ChipFET 1206-8 pin-out, package outline, pad patterns, evaluation board layout, and thermal performance.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the single-channel 1206-8 ChipFET device. The pin-out is similar to the TSOP-6 configuration, with two additional drain pins to enhance power dissipation and thermal performance. The legs of the device are very short, again helping to reduce the thermal path to the external heatsink/pcb and allowing a larger die to be fitted in the device if necessary.

Single 1206-8 ChipFET



Bottom View

FIGURE 1.

For package dimensions see the 1206-8 ChipFET package outline drawing (<http://www.vishay.com/doc?71151>).

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (<http://www.vishay.com/doc?72286>). This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

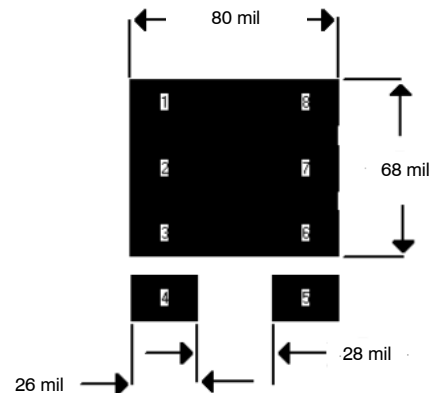


FIGURE 2. Footprint With Copper Spreading

The pad pattern with copper spreading shown in Figure 2 improves the thermal area of the drain connections (pins 1,2,3,6,7,8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further. An example of this method is implemented on the Vishay Siliconix Evaluation Board described in the next section (Figure 3).

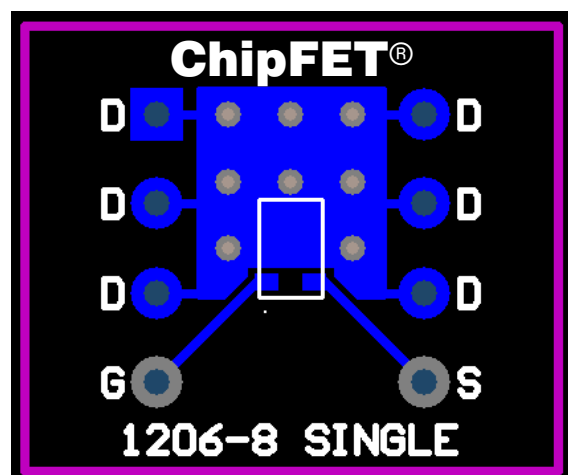
## THE VISHAY SILICONIX EVALUATION BOARD FOR THE SINGLE 1206-8

The ChipFET 1206-08 evaluation board measures 0.6 in by 0.5 in. Its copper pad pattern consists of an increased pad area around the six drain leads on the top-side—approximately 0.0482 sq. in. 31.1 sq. mm—and vias added through to the underside of the board, again with a maximized copper pad area of approximately the board-size dimensions. The outer package outline is for the 8-pin DIP, which will allow test sockets to be used to assist in testing.

The thermal performance of the 1206-8 on this board has been measured with the results following on the next page. The testing included comparison with the minimum recommended footprint on the evaluation board-size pcb and the industry standard one-inch square FR4 pcb with copper on both sides of the board.



Front of Board



Back of Board

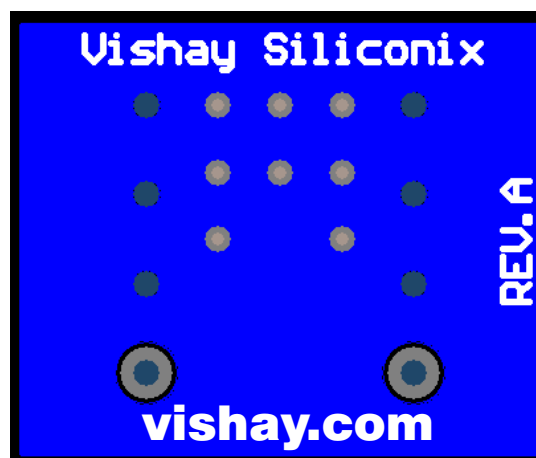


FIGURE 3.

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the 1206-8 ChipFET measured as junction-to-foot thermal resistance is  $15^{\circ}\text{C/W}$  typical,  $20^{\circ}\text{C/W}$  maximum for the single device. The “foot” is the drain lead of the device as it connects with the body. This is identical to the SO-8 package  $R_{\theta_{jf}}$  performance, a feat made possible by shortening the leads to the point where they become only a small part of the total footprint area.

### Junction-to-Ambient Thermal Resistance (dependent on pcb size)

The typical  $R_{\theta_{ja}}$  for the single-channel 1206-8 ChipFET is  $80^{\circ}\text{C/W}$  steady state, compared with  $68^{\circ}\text{C/W}$  for the SO-8. Maximum ratings are  $95^{\circ}\text{C/W}$  for the 1206-8 versus  $80^{\circ}\text{C/W}$  for the SO-8.

### Testing

To aid comparison further, Figure 4 illustrates ChipFET 1206-8 thermal performance on two different board sizes and three different pad patterns. The results display the thermal performance out to steady state and produce a graphic account of how an increased copper pad area for the drain connections can enhance thermal performance. The measured steady state values of  $R_{\theta_{ja}}$  for the single 1206-8 ChipFET are :

1) Minimum recommended pad pattern (see Figure 2) on the evaluation board size of 0.5 in x 0.6 in.	$156^{\circ}\text{C/W}$
2) The evaluation board with the pad pattern described on Figure 3.	$111^{\circ}\text{C/W}$
3) Industry standard 1" square pcb with maximum copper both sides.	$78^{\circ}\text{C/W}$

The results show that a major reduction can be made in the thermal resistance by increasing the copper drain area. In this example, a  $45^{\circ}\text{C/W}$  reduction was achieved without having to increase the size of the board. If increasing board size is an option, a further  $33^{\circ}\text{C/W}$  reduction was obtained by maximizing the copper from the drain on the larger 1" square pcb.

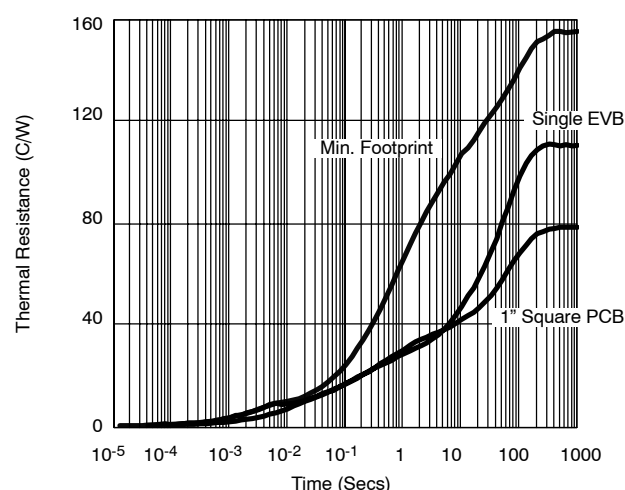


FIGURE 4. Single 1206-8 ChipFET

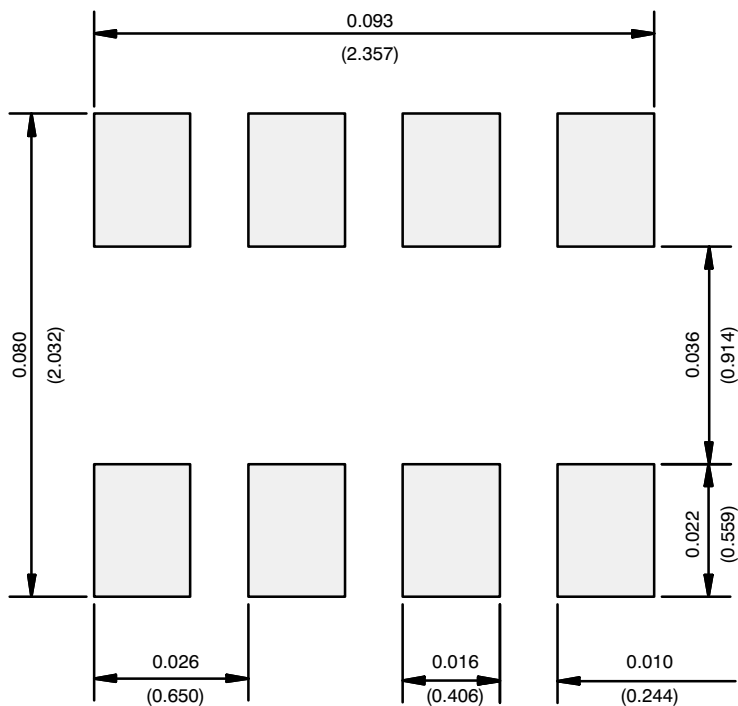
## SUMMARY

The thermal results for the single-channel 1206-8 ChipFET package display similar power dissipation performance to the SO-8 with a footprint reduction of 80%. Careful design of the package has allowed for this performance to be achieved. The short leads allow the die size to be maximized and thermal resistance to be reduced within the confines of the TSOP-6 body size.

## ASSOCIATED DOCUMENT

1206-8 ChipFET Dual Thermal performance, AN812 (<http://www.vishay.com/doc?71127>).

## RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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