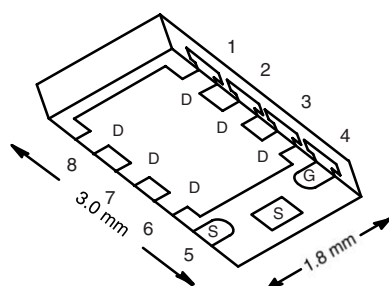


N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
20	0.010 at $V_{GS} = 10$ V	12	9.8 nC
	0.0135 at $V_{GS} = 4.5$ V	12	

PowerPAK ChipFET Single



Bottom View

Marking Code

AC	XXX
----	-----

Lot Traceability
and Date Code

Part # Code

FEATURES

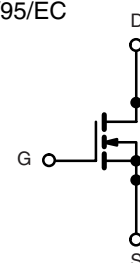
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Gen III Power MOSFET
- New Thermally Enhanced PowerPAK® ChipFET® Package
 - Small Footprint Area
 - Low On-Resistance
 - Thin 0.8 mm Profile
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch
- DC/DC



Ordering Information: Si5456DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	50	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	34	40	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	3	4	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See Solder Profile (www.vishay.com/ppg?73257). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 90 °C/W.

SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

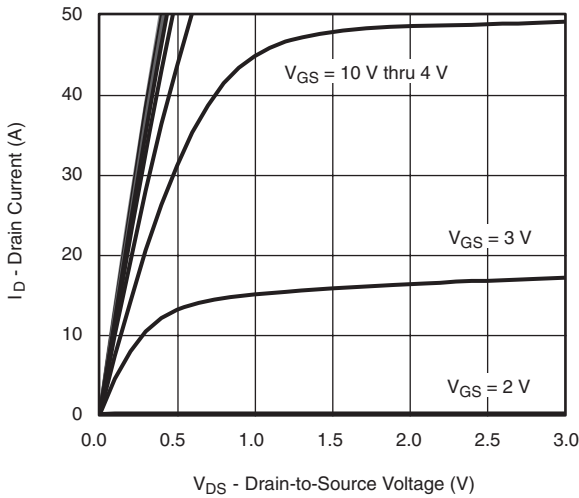
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		21		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 4.8		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	ns
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 9.3 A		0.008	0.010	Ω
		V _{GS} = 4.5 V, I _D = 8 A		0.011	0.0135	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 9.3 A		25		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		1200		pF
Output Capacitance	C _{oss}			350		
Reverse Transfer Capacitance	C _{rss}			220		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 14 A		20	30	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 14 A		9.8	15	
Gate-Source Charge	Q _{gs}			3.2		
Gate-Drain Charge	Q _{gd}			3.2		
Gate Resistance	R _g	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.1 Ω I _D ≅ 9.6 A, V _{GEN} = 4.5 V, R _g = 1 Ω		20	30	ns
Rise Time	t _r			15	25	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			10	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1.1 Ω I _D ≅ 9.6 A, V _{GEN} = 10 V, R _g = 1 Ω		10	15	
Rise Time	t _r			10	15	
Turn-Off Delay Time	t _{d(off)}			20	30	
Fall Time	t _f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			12	A
Pulse Diode Forward Current	I _{SM}				30	
Body Diode Voltage	V _{SD}	I _S = 9.6 A, V _{GS} = 0 V		0.85	1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 9.6 A, dI/dt = 100 A/μs, T _J = 25 °C		15	30	ns
Body Diode Reverse Recovery Charge	Q _{rr}			10	20	nC
Reverse Recovery Fall Time	t _a			8		ns
Reverse Recovery Rise Time	t _b			7		

Notes:

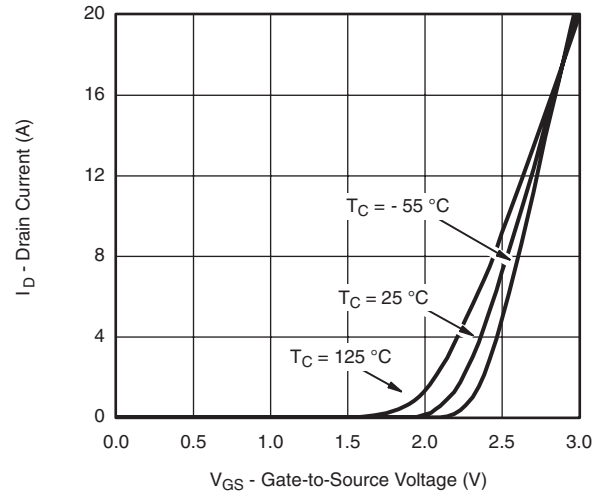
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

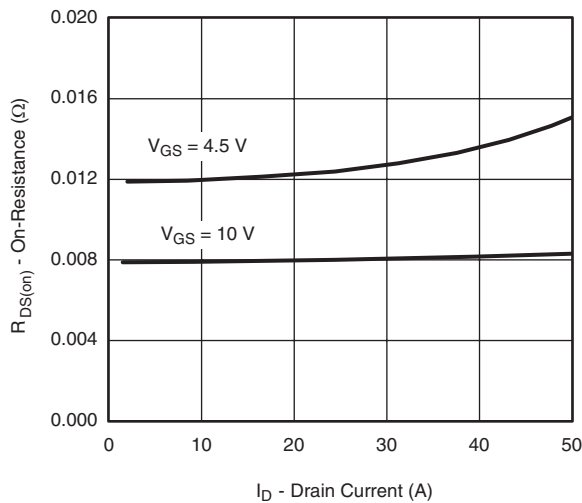
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



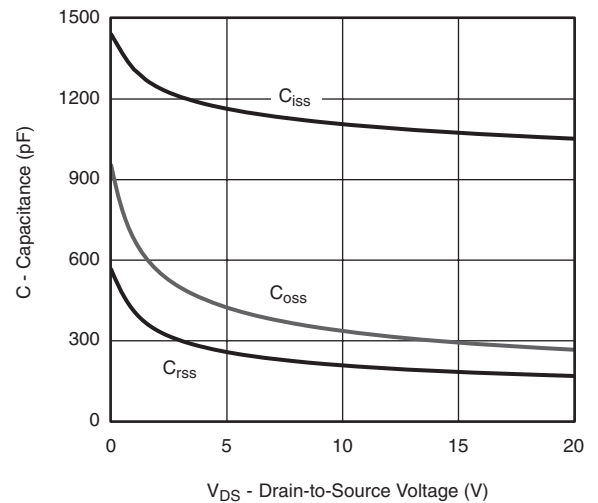
Output Characteristics



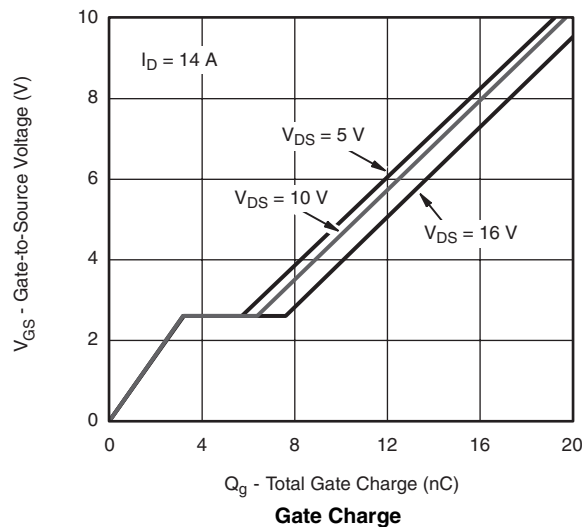
Transfer Characteristics



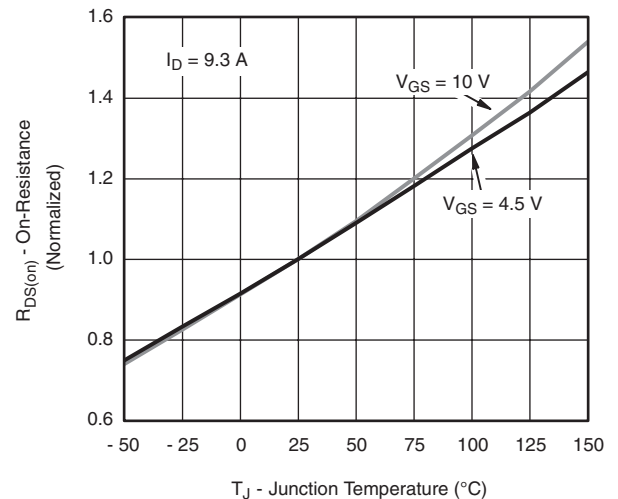
On-Resistance vs. Drain Current and Gate Voltage



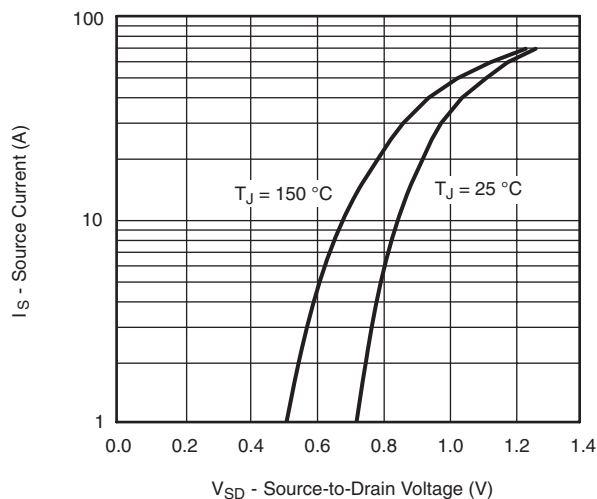
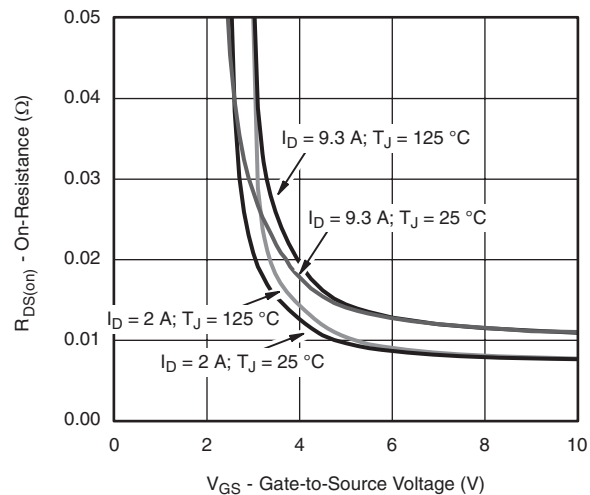
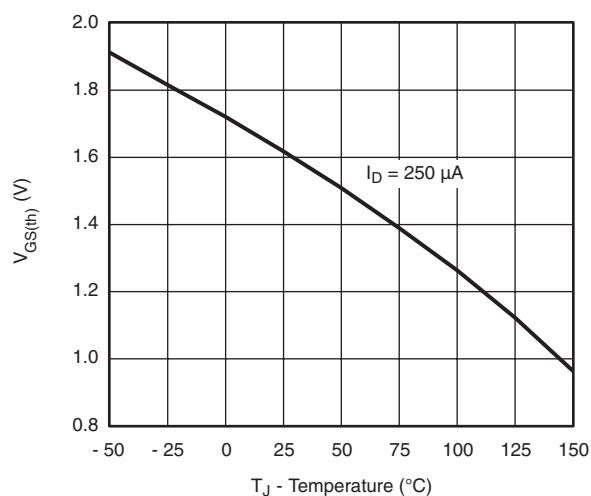
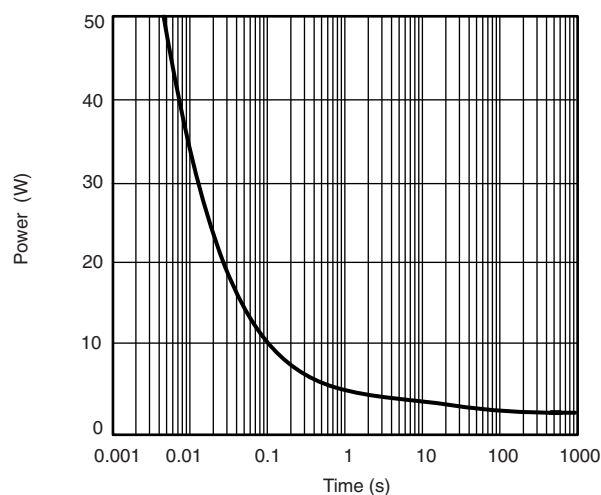
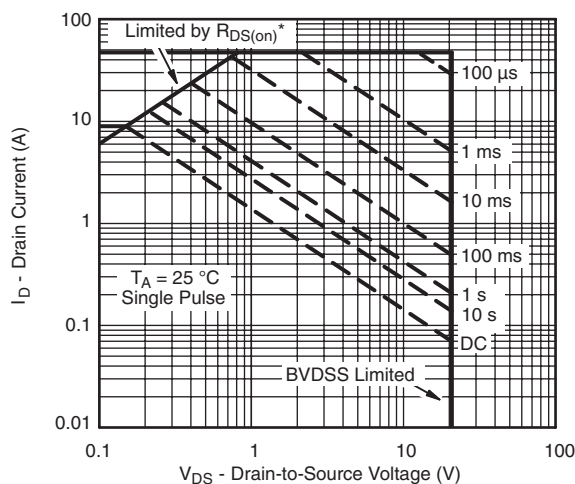
Capacitance



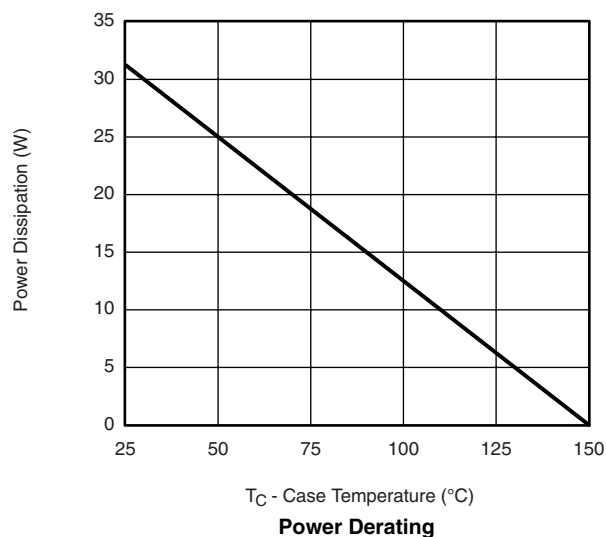
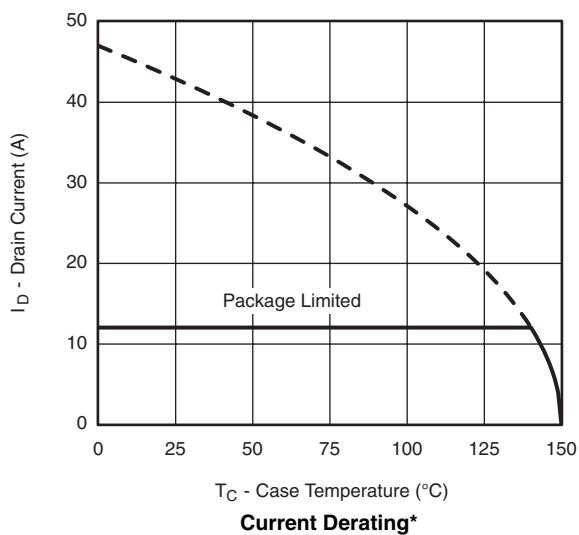
Gate Charge



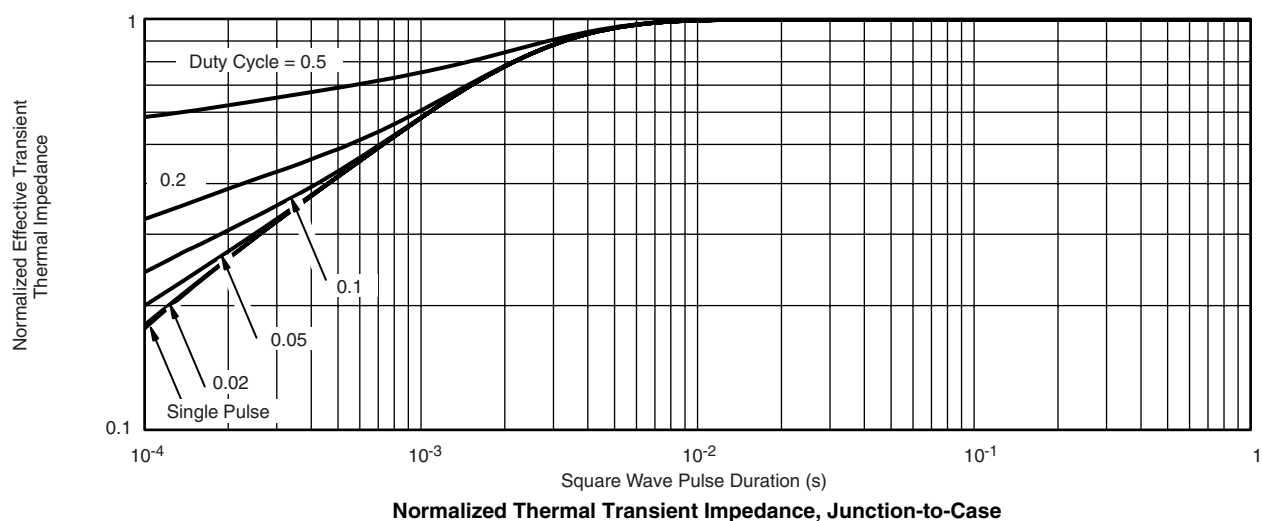
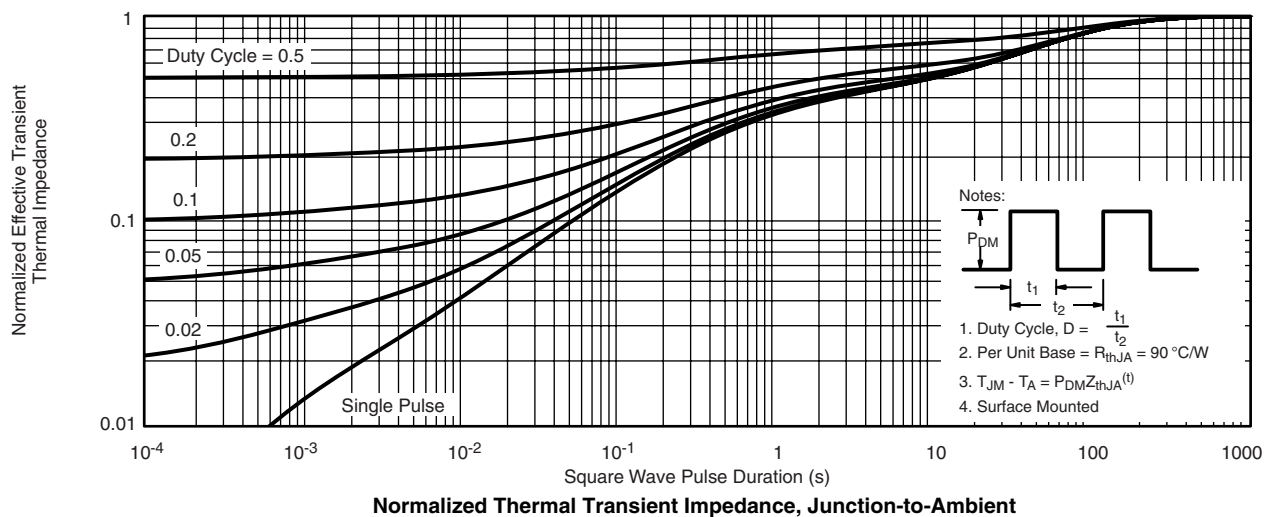
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

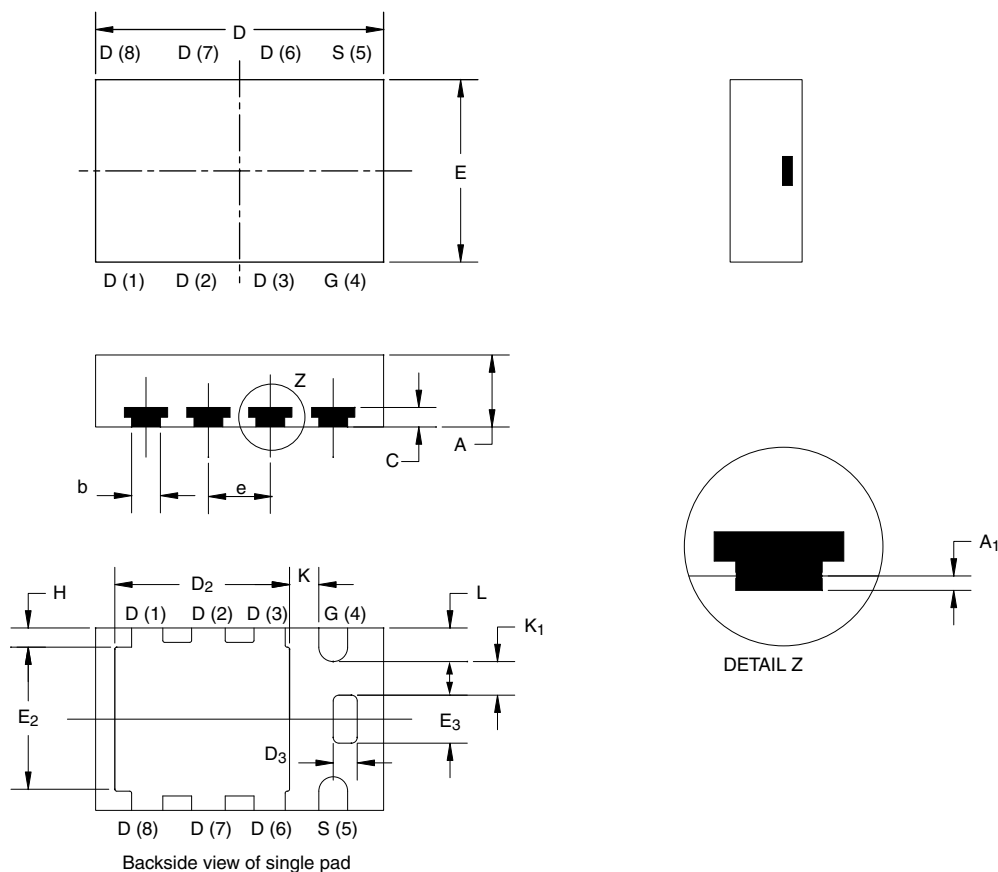


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

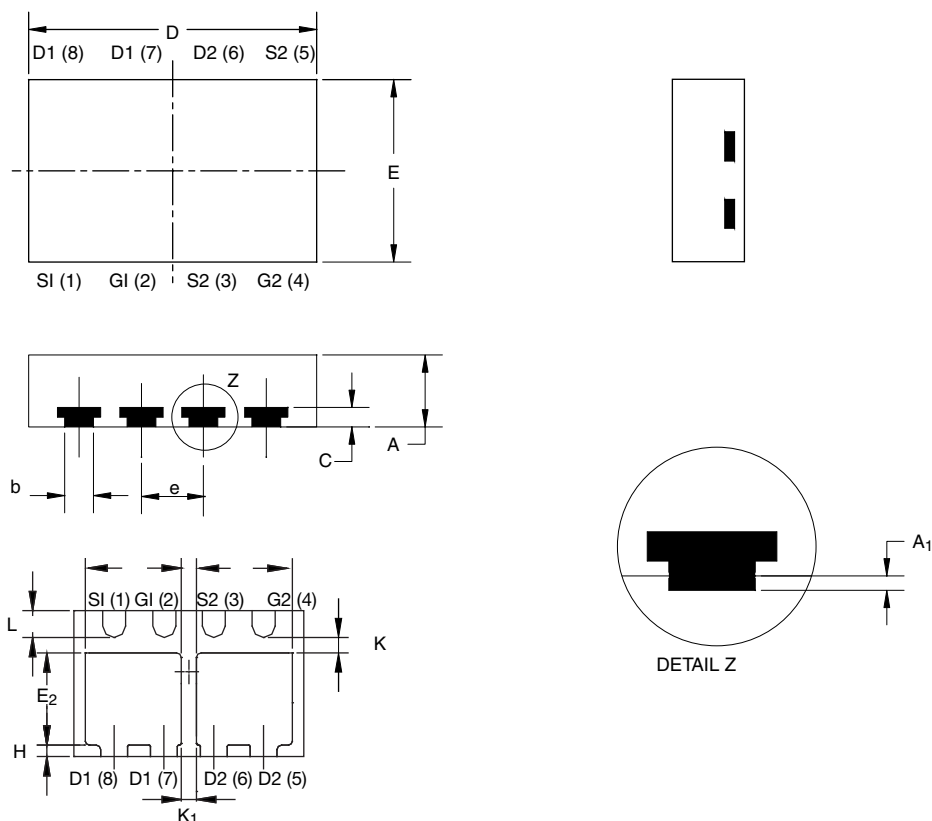
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PowerPAK® ChipFET® SINGLE PAD



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.75	1.87	2.00	0.069	0.074	0.079
D ₃	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	1.38	1.50	1.63	0.054	0.059	0.064
E ₃	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K ₁	0.30	-	-	0.012	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

PowerPAK® ChipFET® DUAL PAD



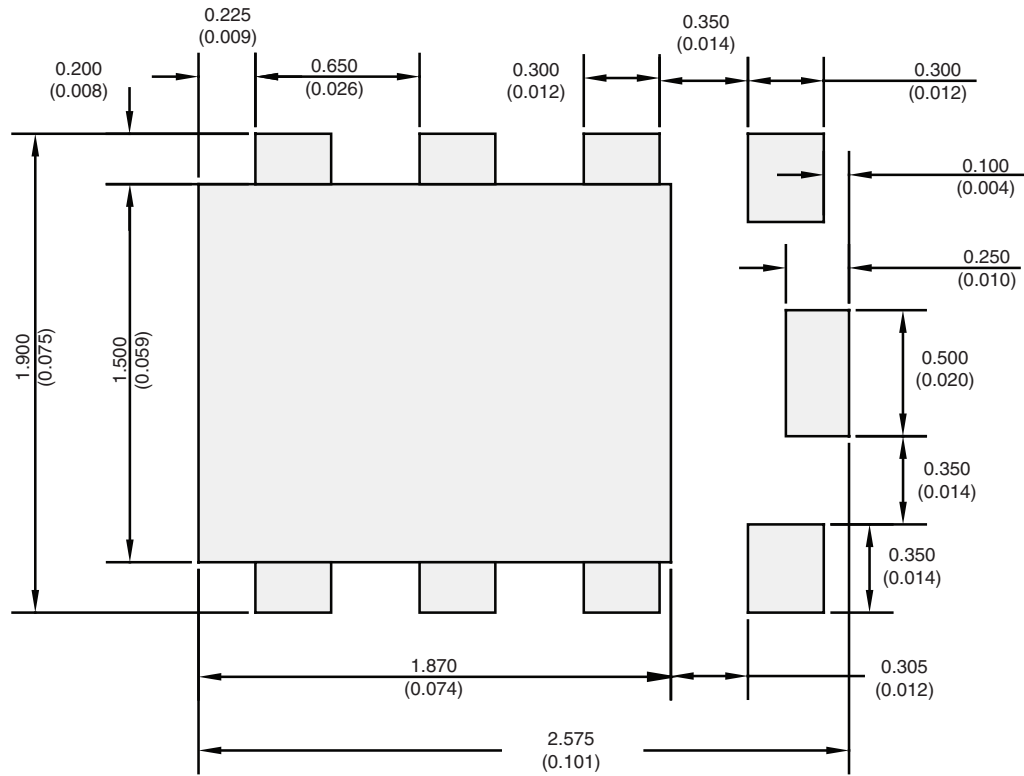
Backside view of dual pad

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A ₁	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D ₂	1.07	1.20	1.32	0.042	0.047	0.052
E	1.82	1.90	1.98	0.072	0.075	0.078
E ₂	0.92	1.05	1.17	0.036	0.041	0.046
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.20	-	-	0.008	-	-
K ₁	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016

ECN: C10-0618-Rev. C, 19-Jul-09

DWG: 5940

RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads
Dimensions in mm/(Inches)

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