

4-PLL ANY-FREQUENCY PRECISION CLOCK **MULTIPLIER/JITTER ATTENUATOR**

Features

- Highly integrated, 4–PLL clock multiplier/jitter attenuator
- Four independent DSPLLs support any-frequency synthesis
 Simultaneous free-run and and jitter attenuation
- Four inputs/four outputs
- Each DSPLL can generate any frequency from 2 kHz to 808 MHz from a 2 kHz to 710 MHz input
- Ultra-low jitter clock outputs: 350 fs rms (12 kHz- 20 MHz) and 410 fs rms (50 kHz-80 MHz) typical
- Meets ITU-T G.8251 and Telcordia GR-253-CORE OC-192 jitter specifications

Applications

- High density any-port, anyprotocol, any-frequency line cards
- ITU-T G.709 OTN custom FEC
- 10/40/100G
- OC-48/192, STM-16/64

- Integrated loop filter with programmable bandwidth as low as 60 Hz
- synchronous operation
- Automatic/manual hitless input clock switching
- Selectable output clock signal format (LVPECL, LVDS, CML, CMOS)
- LOL and interrupt alarm outputs
- I²C programmable
- Single 1.8 V ±5% or 2.5 V ±10% operation with high PSRR onchip voltage regulator
- 10x10 mm PBGA



- 1/2/4/8/10G Fibre Channel
- **GbE/10GbE Synchronous Ethernet**
- Carrier Ethernet, multi-service switches and routers
- MSPP, ROADM, P-OTS, muxponders

Description

The Si5375 is a highly-integrated, 4-PLL, jitter-attenuating precision clock multiplier for applications requiring sub 1 ps jitter performance. Each of the DSPLL[®] clock multiplier engines accepts an input clock ranging from 2 kHz to 710 MHz and generates an output clock ranging from 2 kHz to 808 MHz. The device provides virtually any frequency translation combination across this operating range. For asynchronous, free-running clock generation applications, the Si5375's reference oscillator can be used as a clock source for any of the four DSPLLs. The Si5375 input clock frequency and clock multiplication ratio are programmable through an I²C interface. The Si5375 is based on Silicon Laboratories' third-generation DSPLL® technology, which provides any-frequency synthesis and jitter attenuation in a highly-integrated PLL solution that eliminates the need for external VCXO and loop filter components. Each DSPLL loop bandwidth is digitally-programmable, providing jitter performance optimization at the application level. The device operates from a single 1.8 or 2.5 V supply with on-chip voltage regulators with excellent PSRR. The Si5375 is ideal for providing clock multiplication and jitter attenuation in high port count optical line cards requiring independent timing domains.

Functional Block Diagram





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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit	
Ambient Temperature	T _A		-40	25	85	°C	
Supply Voltage during	V	2.5 V Nominal	2.25	2.5	2.75	V	
Normal Operation	V DD	1.8 V Nominal	1.71	1.8	1.89	V	
Note: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.							



Figure 1. Differential Voltage Characteristics



Figure 2. Rise/Fall Time Characteristics



Table 2. DC Characteristics

 $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, T_A = -40 \text{ to } 85 \text{ °C})$

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
		LVPECL Format 622.08 MHz Out All CKOUTs Enabled		870	980	mA
Supply Current ¹	I _{DD}	CMOS Format 19.44 MHz Out All CKOUTs Enabled	_	780	880	mA
		Disable Mode		660		mA
CKINn Input Pins ²						
Input Common Mode	V	1.8 V ± 5%	0.9		1.4	V
Voltage (Input Thresn- old Voltage)	VICM	2.5 V ± 10%	1		1.7	V
Input Resistance	CKN _{RIN}	Single-ended	20	40	60	kΩ
Single-Ended Input	V	f _{CKIN} < 212.5 MHz See Figure 1.	0.2			V _{PP}
Voltage Swing (See Absolute Specs)	VISE	f _{CKIN} > 212.5 MHz See Figure 1.	0.25			V _{PP}
Differential Input	V _{ID}	f _{CKIN} < 212.5 MHz See Figure 1.	0.2			V _{PP}
(See Absolute Specs)		f _{CKIN} > 212.5 MHz See Figure 1.	0.25	_		V _{PP}
Output Clocks (CKOU	Tn) ^{3,4}					
Common Mode	CKO _{VCM}	LVPECL 100 Ω load line-to-line	V _{DD} – 1.42	_	V _{DD} -1.25	V
Differential Output Swing	СКО _{VD}	LVPECL 100 Ω load line-to-line	1.1		1.9	V _{PP}
Single Ended Output Swing	CKO _{VSE}	LVPECL 100 Ω load line-to-line	0.5		0.93	V _{PP}
Differential Output Voltage	СКО _{VD}	CML 100 Ω load line-to-line	350	425	500	mV _{PP}
Common Mode Output Voltage	CKO _{VCM}	CML 100 Ω load line-to-line		V _{DD} -0.36	—	V
Notes: 1. Current draw is ind 2. No under- or oversi 3. LVPECL outputs re	ependent of sup hoot is allowed.	pply voltage.				

LVPECL outputs require nominal V_{DD} = 2.5 V.
 LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.



Table 2. DC Characteristics (Continued)

 $(V_{DD} = 1.8 \pm 5\%, 2.5 \pm 10\%, T_A = -40$ to 85 °C)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Differential Output		LVDS 100 Ω load line-to-line	500	700	900	mV _{PP}
Voltage	UNUVD	Low Swing LVDS 100 Ω load line-to-line	350	425	500	mV _{PP}
Common Mode Output Voltage	CKO _{VCM}	LVDS 100 Ω load line-to-line	1.125	1.2	1.275	V
Differential Output Resistance	CKO _{RD}	CML, LVPECL, LVDS — 200 — CMOS — — 0.		_	Ω	
Output Voltage Low	CKO _{VOLLH}	CMOS	CMOS — — 0.		0.4	V
Output Voltage High	CKO _{VOHLH}	V _{DD} = 1.71 V CMOS	0.8 x V _{DD}		_	V
		ICMOS[1:0] = 11 V _{DD} = 1.8 V	_	7.5	_	mA
		ICMOS[1:0] = 10 V _{DD} = 1.8 V		5.5	_	mA
Output Drive Current		ICMOS[1:0] = 01 V _{DD} = 1.8 V		3.5	_	mA
(CMOS driving into CKO _{VOL} for output low	CKO -	ICMOS[1:0] = 00 V _{DD} = 1.8 V		1.75	_	mA
or CKO _{VOH} for output high. CKOUT+ and CKOUT– shorted	Cruio	ICMOS[1:0] = 11 V _{DD} = 2.5 V		20	_	mA
externally)		ICMOS[1:0] = 10 V _{DD} = 2.5 V		15	_	mA
		ICMOS[1:0] = 01 V _{DD} = 2.5 V	_	10	_	mA
		ICMOS[1:0] = 00 V _{DD} = 2.5 V	_	5	_	mA
Notes: 1. Current draw is ind	lependent of sur	oply voltage.				<u> </u>

2. No under- or overshoot is allowed.

3. LVPECL outputs require nominal V_{DD} = 2.5 V. 4. LVPECL, CML, LVDS and low-swing LVDS measured with Fo = 622.08 MHz.



Table 2. DC Characteristics (Continued) (V_{DD} = 1.8 \pm 5%, 2.5 \pm 10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit				
2-Level LVCMOS Input Pins										
		V _{DD} = 1.71 V			0.5	V				
Input Voltage Low	VIL	V _{DD} = 2.25 V			0.7	V				
		V _{DD} = 1.89 V	1.4		_	V				
Input Voltage High	VIH	V _{DD} = 2.25 V	1.8	—	—	V				
LVCMOS Output Pins	LVCMOS Output Pins									
Output Voltage Low		IO = 2 mA V _{DD} = 1.71 V	_	_	0.4	V				
Output Voltage Low	VOL	IO = 2 mA V _{DD} = 2.25 V	_		0.4	V				
Output Voltage High		IO = -2 mA V _{DD} = 1.71 V	V _{DD} - 0.4		_	V				
Output Voltage High	∨он	IO = -2 mA V _{DD} = 2.25 V	V _{DD} - 0.4		_	V				
Notes: 1. Current draw is independent of supply voltage.										

under- or overshoot is allowed.



Table 3. AC Characteristics

(V_DD = 1.8 ± 5%, 2.5 ±10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Single-Ended Referen	ce Clock Inp	ut Pin OSC_P (OSC_N with	Cap to GN) ¹		
OSC_P to OSC_N Resistance	OSC _{RIN}	RATE_REG = 0101 or 0110, ac coupled		100	_	Ω
Input Voltage Swing	OSC _{VPP}	RATE_REG = 0101 or 0110, ac coupled	0.5		1.2	V _{PP}
Differential Reference	Clock Input I	Pins (OSC_P/OSC_N) ¹				
Input Voltage Swing	OSC _{VPP}	RATE_REG = 0101 or 0110, ac coupled	0.5		2.4	V _{PP}
CKINn Input Pins	<u> </u>			<u> </u>	<u> </u>	
Input Frequency	CKN _F		0.002	—	710	MHz
Input Duty Cycle (Minimum Pulse Width)	CKN _{DC}	Whichever is smaller (i.e., the 40% / 60% limitation applies only to high frequency clocks)	40	_	60	%
			2			ns
Input Rise/Fall Time	CKN _{TRF}	20–80% See Figure 2			11	ns
CKOUTn Output Pins						
(See ordering section to	or speed grade	<pre>> vs frequency limits)</pre>			1	1
Output Frequency (Output not config- ured for CMOS or Disabled)	СКО _F		0.002	_	808	MHz
Maximum Output Frequency in CMOS Format	СКО _F				212.5	MHz
Output Rise/Fall (20–80 %) @ 622.08 MHz output	CKO _{TRF}	Output not configured for CMOS or Disabled See Figure 2		230	350	ps
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO _{TRF}	CMOS Output $V_{DD} = 1.71$ $C_{LOAD} = 5 \text{ pF}$	—	_	8	ns
Output Rise/Fall (20–80%) @ 212.5 MHz output	CKO _{TRF}	CMOS Output $V_{DD} = 2.25$ $C_{LOAD} = 5 \text{ pF}$	—	_	2	ns
Notes:						

1. A crystal may not be used in place of an oscillator.

2. Input to output skew after an ICAL is not controlled and can be any value.



Table 3. AC Characteristics (Continued) (V_{DD} = 1.8 \pm 5%, 2.5 \pm 10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
Output Duty Cycle Uncertainty @ 622.08 MHz	CKO _{DC}	100 Ω Load Line-to-Line Measured at 50% Point (differential)		_	±40	ps		
LVCMOS Input Pins								
Minimum Reset Pulse Width	t _{RSTMN}		1	_	—	μs		
Reset to Microproces- sor Access Ready	t _{READY}		— — 10		10	ms		
LVCMOS Output Pins								
Rise/Fall Times	t _{RF}	C _{LOAD} = 20pf See Figure 2	_	25	_	ns		
LOSn Trigger Window	Window LOS _{TRIG} From last CK N3 ≠		_	_	4.5 x N3	Т _{СКІN}		
Time to Clear LOL after LOS Cleared	t _{CLRLOL}	↓LOS to ↓LOL Fold = Fnew Stable OSC_P, OSC_N reference	_	10	_	ms		
Device Skew ²								
Phase Change due to Temperature Variation	t _{TEMP}	Max phase changes from -40 to +85 °C	_	300	500	ps		
 Notes: 1. A crystal may not be used in place of an oscillator. 2. Input to output skew after an ICAL is not controlled and can be any value. 								



Table 4. Microprocessor Control (V_{DD} = 1.8 \pm 5%, 2.5 \pm 10%, T_A = -40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit			
I ² C Bus Lines (SDA, SCL)									
Input Voltage Low	VIL _{I2C}		—	_	0.25 x V _{DD}	V			
Input Voltage High	VIH _{I2C}		$0.7 \mathrm{x} \mathrm{V}_\mathrm{DD}$		V _{DD}	V			
Hysteresis of Schmitt	VHYS _{I2C}	V _{DD} = 1.8V	$0.1 \mathrm{x} \mathrm{V}_{\mathrm{DD}}$			V			
trigger inputs		V _{DD} = 2.5	$0.05 \times V_{DD}$			V			
	VO	V _{DD} = 1.8 V IO = 3 mA	_		0.2 x V _{DD}	V			
Output voltage LOW	VOL _{I2C}	V _{DD} = 2.5 IO = 3 mA	_		0.4	V			



Table 5. Performance Specifications V_{DD} = 1.8 V ±5% or 2.5 V ±10%, T_A = -40 to 85 °C

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit		
PLL Performance*								
Lock Time	t _{LOCKMP}	Start of ICAL to \downarrow of LOL	—	35	1200	ms		
Output Clock Phase Change	t _{P_STEP}	After clock switch f3 \ge 128 kHz	—	200	_	ps		
Closed Loop Jitter Peaking	J _{PK}		—	0.05	0.1	dB		
Jitter Tolerance	J _{TOL}	Jitter Frequency ≥ Loop Band- width	5000/BW	_	_	ns pk-pk		
		1 kHz Offset	—	-106		dBc/Hz		
Phase Noise	CKO	10 kHz Offset	—	-114	_	dBc/Hz		
fout = 622.08 MHz	CKOPN	100 kHz Offset	—	-116		dBc/Hz		
		1 MHz Offset	—	-132		dBc/Hz		
Subharmonic Noise	SP _{SUBH}	Phase Noise @ 100 kHz Offset	—	-88	_	dBc		
Spurious Noise	SP _{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	-70		dBc		
Jitter Generation	J _{GEN}	f _{IN} = f _{OUT} = 622.08 MHz, BW = 120 Hz LVPECL output 12 kHz–20 MHz	_	350	410	fs rms		
		50 kHz–80 MHz	—	410	_	fs rms		
*Note: fin = fout = 622.08 MHz; B	N = 120 Hz; I	LVDS.	II			1		



Table 6. Thermal Characteristics^{1,2}

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Maximum Junction Temperature			_	125	_	°C
Thermal Resistance Junction to Ambient	ΑLΨ	Still Air Air Flow 1 m/s Air Flow 2 m/s Air Flow 3 m/s	 	16 14 13 12	 	°C/W
Thermal Resistance Junction to Case	φJC	Still Air	_	3.4	_	°C/W

Notes:

1. In most circumstances the Si5375 does not require special thermal management. A system level thermal analysis is strongly recommend. Contact Silicon Labs applications for further details if required.

2. Thermal characteristic for the 80-pin Si5375 on an 8-layer PCB.

Table 7. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V _{DD}	-0.5 to 2.8	V
LVCMOS Input Voltage	V _{DIG}	–0.3 to (V _{DD} + 0.3)	V
CLKIN1P/N_q	CKN _{VIN}	0 to V _{DD}	V
OSC_P, OSC_N Voltage Limits	OSC _{VIN}	0 to 1.2	V
Operating Junction Temperature	T _{JCT}	-55 to 150	°C
Storage Temperature Range	T _{STG}	-55 to 150	°C
ESD HBM Tolerance (100 pF, 1.5 k); All pins except CKINnP/N-q		2	kV
ESD MM Tolerance; All pins except CKINnP/N_q		200	V
ESD HBM Tolerance (100 pF, 1.5 k); CKINnP/N_q		700	V
ESD MM Tolerance; CKINnP/N_q		125	V
Latch-Up Tolerance		JESD78 Compliant	
Note: Permanent device damage may occur if the a	absolute maximum rati	ings are exceeded. Functional operation	should be

restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.







Figure 3. Typical Application Schematic



3. Typical Phase Noise Plot

- 622.08 MHz input
- 641.52 MHz output
- 321 fs RMS jitter (12 kHz to 20 MHz)



Figure 4. Si5375 Phase Noise Plot



4. Functional Description



Figure 5. Functional Block Diagram

The Si5375 is a highly integrated jitter-attenuating clock multiplier that integrates four fully independent DSPLLs and provides ultra-low jitter generation with less than 410 fs RMS. The device accepts clock inputs ranging from 2 kHz to 710 MHz and generates independent, synchronous clock outputs ranging from 2 kHz to 808 MHz for each DSPLL. Virtually any frequency translation (M/N) combination across its operating range is supported. The Si5375 supports a digitally programmable loop bandwidth that can range from 60 Hz to 8.4 kHz requiring no external loop filter components. An external single-ended or differential reference clock or XO is required for the device to enable ultra-low jitter generation and jitter attenuation. The Si5375 uses this external reference clock as both a jitter and holdover reference. The reference clock can be either single-ended or differential and should be connected to the OSC_P pin (and the OSC_N pin for differential signaling). Because there is very little jitter attenuation from the OSC_P and OSC_N pins to the output clocks, a low-jitter reference clock. For more details, see the description of RATE_REG (register 2 on page 12) and the Any-Frequency Precision Clocks Family Reference Manual, which can be downloaded from http://www.silabs.com/timing. The reference oscillator can be internally routed into CKIN2_q, so free-running clock generation is supported for each DSPLL offering simultaneous synchronous and asynchronous operation. Configuration and control of the Si5375 is primarily handled through the I²C interface.

The device monitors each input clock for Loss-of-Signal (LOS) and provides a LOS alarm when missing pulses on any of the input clocks are detected. The device monitors the lock status of each DSPLL and provides a Loss-of-Lock (LOL) alarm when the DSPLL is unlocked. The lock detect algorithm continuously monitors the phase of the selected input clock in relation to the phase of the feedback clock. The Si5375 provides a VCO freeze capability that allows the device to continue generation of a stable output clock when the input reference is lost.

The output drivers are configurable to support common signal formats, such as LVPECL, LVDS, CML, and CMOS loads. If the CMOS signal format is selected, each differential output buffer generates two in-phase CMOS clocks at the same frequency. For system-level debugging, a bypass mode drives the clock output directly from the selected input clock, bypassing the internal DSPLL.

Silicon Laboratories offers a PC-based software utility, Si537xDSPLL*sim* that can be used to determine valid frequency plans and loop bandwidth settings to simplify device setup. Si537xDSPLL*sim* provides the optimum input, output, and feedback divider values for a given input frequency and clock multiplication ratio that minimizes phase noise. This utility can be downloaded from http://www.silabs.com/timing. For further assistance, refer to the Si53xx Any-Frequency Precision Clocks Family Reference Manual.



5. Si5375 Application Examples and Suggestions

5.1. Schematic and PCB Layout

For a typical application schematic and PCB layout, see the Si537x-EVB Evaluation Board User's Guide, which can be downloaded from www.silabs.com/timing.

In order to preserve the ultra low jitter of the Si5375 in applications where the four different DSPLL's are each operating at different frequency, special care and attention must be paid to the PCB layout. The following is a list of rules that should be observed:

- 1. The four V_{DD} supplies should be isolated from one another with four ferrite beads. They should be separately bypassed with capacitors that are located very close to the Si5375 device.
- 2. Use a solid and undisturbed ground plane for the Si5375 and all of the clock input and output return paths.
- 3. For applications that wish to logically connect the four RESET signals, do not tie them together underneath the BGA package. Instead connect them outside of the BGA footprint.
- 4. As much as is possible, do not route clock input and output signals underneath the BGA package. The clock output signals should go directly outwards from the BGA footprint.
- 5. Avoid placing the OSC_P and OSC_N signals on the same layer as the clock outputs. Add grounded guard traces surrounding the OSC_P and OSC_N signals.
- 6. Where possible, place the CKOUT and CKIN signals on separate PCB layers with a ground layer between them. The use of ground guard traces between all clock inputs and outputs is recommended.

For more information, see the Si537x-EVB Evaluation Board User's Guide and Appendix I of the Si53xx Reference Manual, Rev 0.5 or higher.

5.2. Thermal Considerations

The Si5375 dissipates a significant amount of heat and it is important to take this into consideration when designing the Si5375 operating environment. Among other issues, high die temperatures can result in increased jitter and decreased long term reliability. It is therefore recommended that one or more of the following occur:

- 1. Use a heat sink: A heat sink example is Aavid part number 375324B00035G.
- 2. Use a V_{DD} voltage of 1.8 V.
- 3. Limit the ambient temperature to significantly less that 85 °C.
- 4. Implement very good air flow.

5.3. SCL Leakage

When selecting pull up resistors for the two I^2C signals, note that there is an internal pull down resistor of 18 k Ω from the SCL pin to ground. This comment does not apply to the SDA pin.

5.4. RSTL_x Pins

It is recommended that the four RSTL_x pins (RSTL_A, RSTL_B, RSTL_C and RSTL_D) be logically connected together such that all four DSPLLs are either in or out of reset mode. When a DSPLL is in reset mode, its VCO will not be locked to any signal and may drift across its operating range. If a drifting VCO has a frequency similar to that of an operating VCO, there could be some crosstalk between the two VCOs. To avoid this from occurring during device initialization, DSPLLsim loads each DSPLL with default Free Run frequency plans with VCO values apart from one another. If the four RSTL_x pins are directly connected to one another, the connections should not be made directly underneath the BGA package. Instead, the connections should be made outside the package footprint.



5.5. Reference Oscillator Selection

Care should be taken during the selection of the external oscillator that is connected to the OSC_P and OSC_N pins. There is no jitter attenuation from the OSC reference inputs to the output; so, to achieve low output jitter, a low-jitter reference OSC must be used. Also, the output drift during holdover will be the same as the drift of the OSC reference. For example, a Stratum 3 application will require an OSC reference source that has Stratum 3 stability (though Stratum 3 accuracy is not required).

The OSC frequency can be any value from 109 to 125.5 MHz. See the RATE_REG (reg 2) description. Alternately, for applications with less demanding jitter requirements, the OSC frequency can be in the range from 37 to 41 MHz. For applications that use Free Run mode, the freedom to use any OSC frequency within these bands can be used to select an OSC frequency that has an integer relationship to the desired output frequency, which will make it easier to find a high-performance frequency plan.

If Free Run is not being used, an OSC frequency that is not integer-related to the output frequency is preferred. A recommended choice for an external oscillator is the Silicon Labs 530HB121M109DG, which is a 2.5 V, CML device with a temperature stability of 20 ppm. It was used to take the typical phase noise plot on page 14. For more details and a more complete discussion of these topics, see the Si53xx Reference Manual.

5.6. Alarms

To assist in the programming of the IRQ_n pins, refer to the below diagram of the Si5375 alarm structure.



Figure 6. Si5375 Alarm Structure



5.7. OSC_P and OSC_N Connection

Figures 7, 8, and 9 show examples of connecting various OSC reference sources to the OSC_P and OSC_N pins. A crystal may not be used in place of an external oscillator.



Figure 7. Differential OSC Reference Input Example for Si5375



Figure 8. Single-Ended OSC Reference Input Example for Si5375



Figure 9. Single-Ended, 2.5 V, CMOS XO Connection



6. Register Map

The Si5375 has four identical register maps for each DSPLL having a unique I²C address. The I²C address is 11010 [A1] [A0] for the entire device. Each corresponding DSPLL [A1] [A0] address is fixed as below.

[A1] [A0] DSPLLA: 0 0 DSPLLB: 0 1 DSPLLC: 1 0 DSPLLD: 1 1

Note: The Si5375 register map is similar to the Si5319, although not identical.

All register bits that are not defined in this map should always be written with the specified Reset Values. Writing values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Register Address	D7	D6	D5	D4	D3	D2	D1	D0
0		FREE_RUN	CKOUT_ ALWAYS_ ON				BYPASS_ REG	
2		BWSEL_	REG[3:0]			RATE_R	EG [3:0]	
3			VCO_ FREEZE	SQ_ICAL				
5	ICMO	S[1:0]						
6						SI	OUT_REG[2	:0]
8			HLOO	G[1:0]				
10						DSBL_REG		
11								PD_CK
16				CLAT	[7:0]			
17	FLAT_VALID				FLAT[14:8]		
18				FLAT	[7:0]			
19				VALTIME[1:0]			LOCK[T2:0]	
20						Write to 0	LOL_PIN	IRQ_PIN
21	Write to 0	Write to 0						
22							LOL_POL	INT_POL
23							LOS_MSK	LOSX_MSK
24								LOL_MSK



Register Address	D7	D6	D5	D4	D3	D2	D1	D0		
25		N1_HS[2:0]	L							
31						NC1_L	S[19:16]	l		
32		L.	L	NC1_L	S[15:8]	G[15:8]				
33				NC1_L	.S[7:0]					
40		N2_HS[2:0]			N2_LS[19:16]					
41				N2_LS	5[15:8]					
42				N2_L	S[7:0]					
43							N31[18:16]			
44				N31[[*]	15:8]					
45		N31[7:0]								
46					N32[18:16]					
47				N32[⁻	15:8]					
48				N32	[7:0]					
128							OSC_ACTV _REG	CKACTV_ REG		
129							LOS_INT	LOSX_INT		
130								LOL_INT		
131							LOS_FLG	LOSX_FLG		
132							LOL_FLG			
134				PARTNUM	_RO[11:4]					
135	PARTNUM_RO[3:0] REVID_RO[3:0]									
136	RST_REG	ICAL								
138								LOS_EN [1:1]		
139				LOS_EN [0:0]						



7. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FREE_RUN	CKOUT_ALWAYS_ON				BYPASS_REG	
Туре	R	R/W	R/W	R	R	R	R/W	R

Bit	Name	Function
7	Reserved	
6	FREE_RUN	Free Run.
		This bit configures free run operation. The OSC_P/N in internally routed to the DSPLL. This allows the device to lock to its OSC reference. 0: Disable 1: Enable
5	CKOUT_ALWAYS_ON	CKOUT Always On.
		 This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Notes: The frequency may be significantly off until the part is calibrated. Must be 1 to control output to output skew.
4:2	Reserved	
1	BYPASS_REG	Bypass Register.
		 This bit enables or disables the PLL bypass mode. Use only when the device is in digital hold or before the first ICAL. BYPASS mode is not supported with CMOS clock outputs. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL.
0	Reserved	



Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		BWSEL_I	REG [3:0]		RATE_REG [3:0]			
Туре		R/	W			R/	W	

Bit	Name			Function		
7:4	BWSEL_REG [3:0]	BWSEL_REG. Selects nominal f3dB bandwidth for PLL. See the Si537xDSPLLsim software for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.				
3:0	RATE_REG [3:0]	RATE Setting for Oscillator. Set these for the frequency of the oscillator connected to OSC_P/OSC_N pins. An external oscillator or other clock source must be used. It is not possible to use just a crystal.				
		SettingMinimumRecommendedMaximum010137 MHz40 MHz41 MHz0110109 MHz114.285 MHz125.5 MHzAll others reservedreserved114.285 MHz125.5 MHz				



Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			VCO_FREEZE	SQ_ICAL				
Туре	R	R	R/W	R/W	R	R	R	R

Reset value = 0000 0101

Bit	Name	Function
7:6	Reserved	
5	VCO_FREEZE	 VCO_FREEZE. Forces the part into VCO Freeze. This bit overrides all other manual and automatic clock selection controls. 0: Normal operation. 1: Force VCO Freeze mode. Overrides all other settings and ignores the quality of all of the input clocks.
4	SQ_ICAL	SQ_ICAL. This bit determines if the output clock will remain enabled or be squelched (disabled) during an internal calibration. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMO	S [1:0]						
Туре	R/	/W	R	R	R	R	R	R

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	ICMOS [1:0]. When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. These values assume CKOUT+ is tied to CKOUT 00: 8 mA 01: 16 mA 10: 24 mA 11: 32 mA
5:0	Reserved	



Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						SFOUT_REG [2:0]		
Туре	R	R	R	R	R		R/W	

Reset value = 0010 1101

Bit	Name	Function
7:3	Reserved	
2:0	SFOUT_REG [2:0]	SFOUT_REG [2:0].
		Controls output signal format and disable for CKOUT1 output buffer.
		000: Reserved
		001: Disable
		010: CMOS
		011: Low swing LVDS
		100: Reserved
		101: LVPECL, only available when $V_{DD} = 2.5 V$
		110: CML
		111: LVDS

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			HLOG	_1[1:0]				
Туре	R	R	R/	W	R	R	R	R

Bit	Name	Function
7:6	Reserved	
5:4	HLOG_1 [1:0]	 HLOG_1 [1:0]. 00: Normal operation 01: Holds CKOUT_n output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT_n output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
3:0	Reserved	



Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						DSBL_REG		
Туре	R	R	R	R	R	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2	DSBL_REG	DSBL_REG. This bit controls the powerdown of the CKOUT output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT enabled 1: CKOUT disabled
1:0	Reserved	

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								PD_CK
Туре	R	R	R	R	R	R	R	R/W

Bit	Name	Function
7:1	Reserved	
0	PD_CK	PD_CK. This bit controls the powerdown of the CKIN input buffer. 0: Enabled 1: Disabled



Register 16.

Bit	D7	D6	D5	D4	D3	D2	D1	D0		
Name	CLAT [7:0]									
Туре				R/	W					

Reset value = 0000 0000

Bit	Name	Function
7:0	CLAT [7:0]	CLAT [7:0].
		With INCDEC_PIN = 0, this register sets the phase delay for CKOUT in units of 1/Fosc. This can take as long as 20 seconds. 01111111 = 127/Fosc (2s compliment) 00000000 = 0 10000000 = -128/Fosc (2s compliment)

Register 17.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name	FLAT_VALID		FLAT [14:8]								
Туре	R/W				R/W						

Bit	Name	Function
7	FLAT_VALID	FLAT_VALID.
		 Before writing a new FLAT[14:0] value, this bit must be set to zero, which causes the existing FLAT[14:0] value to be held internally for use while the new value is being written. Once the new FLAT[14:0] value is completely written, set FLAT_VALID = 1 to enable its use. 0: Memorize existing FLAT[14:0] value and ignore intermediate register values during write of new FLAT[14:0] value. 1: Use FLAT[14:0] value directly from registers.
6:0	FLAT [14:8]	FLAT [14:8].
		Fine resolution control for overall device latency from input clocks to output clocks. Positive values increase the skew. See DSPLLsim for details.



Register 18.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name		FLAT [7:0]									
Туре				R/	W						

Reset value = 0000 0000

Bit	Name	Function
7:0	FLAT [7:0]	FLAT [7:0]. Fine resolution control for overall device latency from input clocks to output clocks. Positive values increase the skew. See DSPLLsim for details.

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				VALTIME [1:0]			LOCKT [2:0]	
Туре	R	R	R	R/	/W		R/W	

Bit	Name	Function
7:5	Reserved	
4:3	VALTIME [1:0]	VALTIME [1:0]. Sets amount of time for input clock to be valid before the associated alarm is removed.
		01: 100 ms 10: 200 ms 11: 13 seconds
2:0	LOCKT [2:0]	LOCKT [2:0]. Sets retrigger interval for one shot monitoring phase detector output. One shot is triggered by phase slip in DSPLL. 000: 106 ms 001: 53 ms 010: 26.5 ms 011: 13.3 ms 100: 6.6 ms 101: 3.3 ms 110: 1.66 ms 111: .833 ms



Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOL_PIN	IRQ_PIN
Туре	R	R	R	R	R	W	R/W	R/W

Reset value = 0011 1110

Bit	Name	Function
7:2	Reserved	Must write to 0 for normal operation.
1	LOL_PIN	LOL_PIN.
		The LOL_INT status bit can be reflected on the LOL output pin. 0: LOL output pin tri-stated
		1: LOL_INT status reflected to output pin
0	IRQ_PIN	IRQ_PIN. Reflects the interrupt status on the IRQ output pin. 0: IRQ output pin is tri-stated. 1: Interrupt state reflected to output pin.

Register 21.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Туре	W	W	R	R	R	R	R	R

Reset value = 1111 1111

Bit	Name	Function
7:6	Reserved	Must write to 0 for normal operation.
5:0	Reserved	



Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOL_POL	IRQ_POL
Туре	R	R	R	R	R	R	R/W	R/W

Reset value = 1101 1111

Bit	Name	Function
7:3	Reserved	
1	LOL_POL	LOL_POL. Sets the active polarity for the LOL status when reflected on the LOL_q output pin. 0: Active low 1: Active high
0	IRQ_POL	INT_POL. Sets the active polarity for the interrupt status when reflected on the IRQ. output pin. 0: Active low 1: Active high



Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOS_MSK	LOSX_MSK
Туре	R	R	R	R	R	R	R/W	R/W

Reset value = 0001 1111

Bit	Name	Function
7:2	Reserved	
1	LOS_MSK	LOS_MSK.
		Determines if a LOS on CKIN_q (LOS_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS_FLG register. 0: LOS1 alarm triggers active interrupt on IRQ_q output (if INT_PIN=1). 1: LOS_FLG ignored in generating interrupt output.
0	LOSX_MSK	LOSX_MSK.
		Determines if a LOS on OSC is used in the generation of an interrupt. Writes to this register do not change the value held in the LOSX_FLG register. 0: LOSX alarm triggers active interrupt on IRQ_q output (if INT_PIN=1). 1: LOSX_FLG ignored in generating interrupt output.

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								LOL_MSK
Туре	R	R	R	R	R	R	R	R/W

Reset value = 0011 1111

Bit	Name	Function
7:1	Reserved	
0	LOL_MSK	LOL_MSK. Determines if the LOL_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the LOL_FLG register. 0: LOL alarm triggers active interrupt on IRQ output (if IRQ_PIN=1). 1: LOL_FLG ignored in generating interrupt output.



Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]							
Туре	R/W			R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	N1_HS [2:0].
		Sets value for N1 high speed divider which drives NC1_LS (n = 1 to 2) low-speed divider. 000: N1 = 4 Note: Changing the coarse skew via the INC pin is disabled for this value. 001: N1 = 5 010: N1 = 6 011: N1 = 7 100: N1 = 8 101: N1 = 9 110: N1 = 10 111: N1 = 11
4:0	Reserved	

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Name					NC1_LS [19:16]				
Туре	R	R	R	R	R/W				

Bit	Name	Function
7:4	Reserved	
3:0	NC1_LS [19:16]	NC1_LS [19:16].
		Sets value for NC1 low-speed divider, which drives CKOUTn_q output. Must be 0 or odd.
		000000000000000000000000000000000000
		000000000000000000000000000000000000
		00000000000000011 = 4
		000000000000000101 = 6
		 1111111111111111111=2 ²⁰ Valid divider values=[1, 2, 4, 6,, 2 ²⁰]



Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name	NC1_LS [15:8]										
Туре				R/	W						

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	NC1_LS [15:8].
		Sets value for NC1 low-speed divider, which drives CKOUTn_q output. Must be 0 or odd. 000000000000000000000000000000000000
		Valid divider values = $[1, 2, 4, 6,, 2^{20}]$

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name	NC1_LS [7:0]										
Туре				R/	W						

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [7:0]	NC1_LS [7:0].
		Sets value for NC1 low-speed divider, which drives CKOUTn_q output. Must be 0 or odd. 0000000000000000000000000000000000
		 1111111111111111111111 = 2^{20} Valid divider values = [1, 2, 4, 6,, 2^{20}]



Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0	
Name	N2_HS [2:0]				N2_LS [19:16]				
Туре	R/W			R	R/W				

Reset value = 1100 0000

Bit	Name	Function
7:5	N2_HS [2:0]	N2_HS [2:0]. Sets value for N2 high speed divider which drives N2_LS low-speed divider. 000: 4 001: 5 010: 6 011: 7 100: 8 101: 9 110: 10 111: 11
4	Reserved	
3:0	N2_LS [19:16]	N2_LS [19:16]. Sets value for N2 low-speed divider, which drives phase detector. 000000000000000000000000000000000000



Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name	N2_LS [15:8]										
Туре				R/	W						

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	N2_LS [15:8].
		Sets value for N2 low-speed divider, which drives phase detector.
		000000000000000000000000000000000000
		00000000000000011 = 4
		00000000000000101 = 6
		 111111111111111111 = 2^{20} Valid divider values = [2, 4, 6,, 2^{20}]

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name	N2_LS [7:0]										
Туре				R/	W						

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	N2_LS [7:0].
		Sets value for N2 low-speed divider, which drives phase detector. 000000000000000000000000000000000000



Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N31 [18:16]		
Туре	R	R	R	R	R	R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2:0	N31 [18:16]	N31 [18:16].
		Sets value for input divider for CKINn_q.
		000000000000000000000000000000000000
		000000000000000000000000000000000000
		 111111111111111111 = 2 ¹⁹ Valid divider values = [1, 2, 3,, 2 ¹⁹]

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0		
Name	N31[15:8]									
Туре				R/	W					

Bit	Name	Function						
7:0	N31[15:8]	N31[15:8].						
		s value for input divider for CKIN1.						
		000000000000000000000000000000000000						
		0000000000001 = 2						
		0000000000000010 = 3						
		$111111111111111111 = 2^{19}$						
		Valid divider values = $[1, 2, 3,, 2^{19}]$						



Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0		
Name	N31[7:0]									
Туре				R/	W					

Reset value = 0000 1001

Bit	Name	Function
7:0	N31[7:0]	N31[7:0]. Sets value for input divider for CKIN1. 000000000000000000000000000000000000

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						N32[18:16]		
Туре	R	R	R	R	R	R/W		

Bit	Name	Function
7:3	Reserved	
2:0	N32[18:16]	N32[18:16].
		Sets value for input divider for OSC clock input operation. 000000000000000000 = 1 000000000000000000 = 2 000000000000000000 = 3
		1111111111111111 = 2^{19} Valid divider values=[1, 2, 3,, 2^{19}]



Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0		
Name	N32[15:8]									
Туре				R/	W					

Reset value = 0000 0000

Bit Name Function	n
7:0 N32[15:8] N32[15:8]. Sets value for input divider for OSC clock input of 00000000000000000000000000000000000	operation.

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0		
Name	N32[7:0]									
Туре				R/	W					

Bit	Name	Function
7:0	N32[7:0]	N32[7:0]. Sets value for input divider for OSC clock input operation. 000000000000000000000000000000000000



Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							OSC_ACTV_REG	CK_ACTV_REG
Туре	R	R	R	R	R	R	R	R

Reset value = 0010 0000

Bit	Name	Function
7:2	Reserved	
1	OSC_ACTV_REG	OSC_ACTV_REG.
		Indicates if OSC is currently the active clock for PLL input.
0	CK_ACTV_REG	CK_ACTV_REG.
		Indicates if CKIN_q is currently the active clock for the PLL input. 0: CKIN_q is not the active input clock. Either it is not selected or LOS_INT is 1. 1: CKIN_q is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOS_INT	LOSX_INT
Туре	R	R	R	R	R	R	R	R

Bit	Name	Function
7:2	Reserved	
1	LOS_INT	LOS_INT. Indicates the LOS status on CKINn_q.
		0: Normal operation. 1: Internal loss-of-signal alarm on CKINn_q input.
0	LOSX_INT	LOSX_INT. Indicates the LOS status of the external reference on the OSC_P/N pins. 0: Normal operation. 1: Internal loss-of-signal alarm on OSC_P/N reference clock input.



Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLATPROGRESS							LOL_INT
Туре	R	R	R	R	R	R	R	R

Reset value = 0000 0001

Bit	Name	Function
7	CLATPROGRESS	CLAT Progress.
		Indicates if the last change in the CLAT register has been processed.
		0: Coarse skew adjustment not in progress.
		1: Coarse skew adjustment in progress.
6:1	Reserved	
0	LOL_INT	PLL Loss of Lock Status.
		0: PLL locked.
		T. PLL UNIOCKED.

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOS_FLG	LOSX_FLG
Туре	R	R	R	R	R	R	R/W	R/W

Bit	Name	Function
7:2	Reserved	
1	LOS_FLG	CKINn_q Loss-of-Signal Flag. 0: Normal operation 1: Held version of LOS_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS_MSK bit. Flag cleared by writing 0 to this bit.
0	LOSX_FLG	External Reference (Signal on Pins OSC_P/N) Loss-of-Signal Flag. 0: Normal operation 1: Held version of LOSX_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOSX_MSK bit. Flag cleared by writing 0 to this bit.



Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							LOL_FLG	
Туре	R	R	R	R	R	R	R/W	R

Reset value = 0000 0010

Bit	Name	Function
7:2, 0	Reserved	
1	LOL_FLG	PLL Loss of Lock Flag.
		0: PLL locked 1: Held version of LOL_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOL_MSK bit. Flag cleared by writing 0 to this bit.

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0			
Name		PARTNUM_RO [11:4]									
Туре				F	२						

Bit	Name	Function		
7:0	PARTNUM_RO [11:0]	Device ID (1 of 2). 0000 0100 1011: Si5375		



Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		PARTNUM	/_RO [3:0]		REVID_RO [3:0]			
Туре		F	२			F	२	

Reset value = 1011 0010

Bit	Name	Function
7:4	PARTNUM_RO [11:0]	Device ID (2 of 2). 0000 0100 1011: Si5375
3:0	REVID_RO [3:0]	Device Revision Level. 0010: Revision C Others: Reserved.

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL						
Туре	R/W	R/W	R	R	R	R	R	R

Bit	Name	Function
7	RST_REG	Internal Reset (Same as Pin Reset).
		Note: The I ² C port may not be accessed until 10 ms after RST_REG is asserted. 0: Normal operation.
		1: Reset of all internal logic. Outputs disabled or tristated during reset.
6	ICAL	Start an Internal Calibration Sequence.
		For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. Note: Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-cali- bration, LOL will go low.
5:0	Reserved	



Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								LOS_EN [1:1]
Туре	R	R	R	R	R	R	R	R/W

Reset value = 0000 1111

Bit	Name	Function
7:1	Reserved	
0	LOS_EN [1:0]	Enable CKINn_q LOS Monitoring on the Specified Input (1 of 2).
		 Note: LOS_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS.

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				LOS_EN [0:0]				
Туре	R	R	R	R/W	R	R	R	R

Reset value = 1111 1111

Bit	Name	Function
7:5	Reserved	
4	LOS_EN [1:0]	Enable CKIN_q LOS Monitoring on the Specified Input (2 of 2).
		 Note: LOS_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS.
3:0	Reserved	



7.1. ICAL

The device registers must be configured for the device operation. After device configuration, a calibration procedure must be performed once a stable clock is applied to the selected CKINn input. The calibration process is triggered by writing a "1" to bit D6 in register 136. See the Family Reference Manual for details. In addition, after a successful calibration operation, changing any of the registers indicated in Table 8 requires that a calibration be performed again by the same procedure (writing a "1" to bit D6 in register 136).

Address	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
2	BSWEL_REG
2	RATE_REG
5	ICMOS
10	DSBL_REG
11	PD_CK
19	LOCKT
19	VALTIME
25	N1_HS
31	NC1_LS
40	N2_HS
40	N2_LS
43	N31
46	N32

Table 8. ICAL-Sensitive Registers



8. Pin Descriptions: Si5375



Bottom View Figure 10. Si5375 Pin Configuration (Bottom View)



Pin #	Pin Name	I/O	Signal Level	Description
D4	RSTL_A	I	LVCMOS	External Reset.
D6 F6 F4	RSTL_B RSTL_C RSTL_D			Active low input that performs external hardware reset of all four DSPLLs. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power-on to get a clock output. This pin has a weak pull-up.
B4	IRQ_A	0	LVCMOS	DSPLLq Interrupt Indicator.
D8 H6 F2	IRQ_B IRQ_C IRQ_D			This pin functions as a device interrupt output. The interrupt output, <i>IRQ_PINn</i> must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the <i>IRQ_POLn</i> register bit.
				0 = CKINn present
				1 = LOS on CKINn
				The active polarity is controlled by <i>CK_BAD_POL</i> . If no function is selected, the pin tri-states.
C1, C4, B5	VDD_A	V_{DD}	Supply	Supply.
A7, D5, D7	VDD_B			The device operates from a 1.8 or 2.5 V supply. A 0.1 µF bypass capacitive is required for every VDD_q pin. Bypass capacitors should be associated with the following VDD_q pins:
E7, F5, G9	VDD_C			0.1 μ F per V _{DD} pin.
E3 E3 13	ם חסע			Four 1.0 μ F should also be placed as close to each V _{DD} domain
20,10,00	VDD_D			as is practical. See recommended layout.
E5	OSC_P	Ι	Analog	External OSC.
E6	OSC_N			An external low jitter reference clock should be connected to these pins. See the any-frequency precision clocks family
				reference manual for oscillator selection details.
Note: Interna	Il register names a	re indica	ated by italics,	e.g., IRQ_PIN. See Si5375 Register Map.

Table 9. Si5375 Pin Descriptions



Pin #	Pin Name	I/O	Signal Level	Description
B2	GND	GND	Supply	Ground for each DSPLLq.
A3	GND			Must be connected to system ground. Minimize the ground path
B3	GND			impedance for optimal performance of this device. See
E4	GND			recommended layout.
C8	GND			
A8 D0	GND			
B8 C9	GND			
H7	GND			
J7	GND			
H8	GND			
H9	GND			
G1	GND			
H2	GND			
J2	GND			
G2	GND			
C2	CKIN1P_A	I	Multi	Clock Input for DSPLLq.
D2	CKIN1N_A			Differential input clock. This input can also be driven with a
B7	CKIN1P_B			single-ended signal. Input frequency range is 2 kHz to 710 MHz.
B6	CKIN1N_B			
G8	CKIN1P_C			
F8	CKIN1N_C			
H3	CKIN1P_D			
H4	CKIN1N_D			
E2	LOL_A	0	LVCMOS	DSPLLq Loss of Lock Indicator.
C5	LOL_B			These pins function as the active high PLL loss of lock indicator
E8	LOL_C			if the LOL_PIN register bit is set to 1.
H5	LOL_D			0 = PLL locked.
				1 = PLL unlocked.
				If $LOL_PINn = 0$, this pin will tri-state. Active polarity is
				controlled by the LOL_POLn bit. The PLL lock status will always
.		1		be reflected in the LOL_IVI read only register bit.
	US_UA_A			USPLLQ INPUt Clock Select/Active Clock Indicator.
A6	CS_CA_B			Input: This pin functions as the input clock selector between CKIN and OSC
F9	CS_CA_C			0 = Select CKIN1.
J4	CS_CA_D			1 = Select OSC (Internal).
				Must be high or low. Do not float. If a DSPLL is not used, its
				CS_CA_q pin should be tied high.
Note: Interna	I register names a	re indica	ted by italics,	e.g., IRQ_PIN. See Si5375 Register Map.

Table 9. Si5375 Pin Descriptions (Continued)



Pin #	Pin Name	I/O	Signal Level	Description	
G5	SCL	I	LVCMOS	I ² C Serial Clock.	
				This pin functions as the serial clock input.	
				This pin has a weak pull-down.	
G6	SDA	I/O	LVCMOS	I ² C Serial Data.	
				I ² C pin functions as the bi-directional serial data port.	
B1	CKOUT1P_A	0	Multi	Output Clock for DSPLLq.	
A2	CKOUT1N_A			Differential output clock with a frequency range of 0.002 to	
A9	CKOUT1P_B			808 MHz. Output signal format is selected by SFOUT_REG	
B9	CKOUT1N_B			register bits. Output is differential for LVPECL, LVDS, and CML	
J9	CKOUT1P_C			compatible modes. For CMOS format, both output pins drive in	
J8	CKOUT1N_C			phase single-ended clock outputs at the same frequency.	
J1	CKOUT1P_D				
H1	CKOUT1N_D				
A4, A5	NC	N/A	N/A	No Connection.	
C3, C6				Leave floating. Make no external connections to this pin for	
C7, D3				normal operation.	
D9, E1					
E9, F1					
F7, G3					
G4, G7					
J5, J6					
Note: Internal register names are indicated by italics, e.g., IRQ_PIN. See Si5375 Register Map.					

Table 9. Si5375 Pin Descriptions (Continued)



9. Ordering Guide

Ordering Part Number	Input/Output Clocks	PLL Bandwidth Range	Package	ROHS6 Pb-Free	Temperature Range
Si5375B-A-GL	4/4	60 Hz to 8.4 kHz	10x10 mm 80-PBGA	Yes	–40 to 85 °C
Si5375B-A-BL	4/4	60 Hz to 8.4 kHz	10x10 mm 80-PBGA	No	–40 to 85 °C
Si5375-EVB	Device Development Kit				



10. Package Outline

Figure 11 illustrates the package details for the Si5375. Table 10 lists the values for the dimensions shown in the illustration.



Figure 11. 80-Pin Plastic Ball Grid Array (PBGA)

Symbol	Min	Nom	Max		Min	Nom	Max
Α	1.22	1.39	1.56	E1		8.00 BSC	
A1	0.40	0.50	0.60	е		1.00 BSC	
A2	0.32	0.36	0.40	aaa		0.10	
A3	0.46	0.53	0.60	bbb		0.10	
b	0.50	0.60	0.70	CCC		0.12	
D	10.00 BSC			ddd		0.15	
E	10.00 BSC			eee		0.08	
D1	8.00 BSC						

Table 10. Package Dimensions

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

- 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
- 3. This drawing conforms to JEDEC outline MO-192.
- **4.** Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



11. Recommended PCB Layout



Figure 12. PBGA Card Layout

Table 11. Layout Dimensions

Symbol	MIN	NOM	MAX
Х	0.40	0.45	0.50
C1	8.00		
C2	8.00		
E1	1.00		
E2	1.00		

Notes:

General

- 1. All dimensions shown are in millimeters (mm) unless otherwise noted.
- 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
- 3. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be $60 \ \mu m$ minimum, all the way around the pad.

Stencil Design

- **5.** A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- 6. The stencil thickness should be 0.125 mm (5 mils).
- 7. The ratio of stencil aperture to land pad size should be 1:1.

Card Assembly

- 8. A No-Clean, Type-3 solder paste is recommended.
- **9.** The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.



12. Top Markings

12.1. Si5375 Top Marking (PBGA, Lead-Free)





12.2. Top Marking Explanation (PBGA, Lead-Free)

Mark Method:	Laser			
Logo Size:	6.1 x 2.2 mm Center-Justified			
Font Size:	0.80 mm Right-Justified			
Line 1 Marking:	Device Part Number Si5375B-A-GL			
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.		
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.		
Line 3 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified		
	"e1" Lead-free Finish Symbol (Pb-free BGA Balls)	Circle = 1.4 mm Diameter Center-Justified		
	Country of Origin	TW		



12.3. Si5375 Top Marking (PBGA, Lead-Finish)



12.4. Top Marking Explanation (PBGA, Lead-Finish)

Mark Method:	Laser			
Logo Size:	6.1 x 2.2 mm Center-Justified			
Font Size:	0.80 mm Right-Justified	0.80 mm Right-Justified		
Line 1 Marking:	Device Part Number	Si5375B-A-BL, Pb finish		
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.		
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.		
Line 3 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified		
	"e0" Lead Finish Symbol (SnPb BGA Balls)	Circle = 1.4 mm Diameter Center-Justified		
	Country of Origin	TW		



DOCUMENT CHANGE LIST

Revision 0.16 to Revision 0.2

- Improved the Functional Block Diagram.
- Added specifications for different output formats.
- Added 1.8 V operation.
- Added 40 MHz reference oscillator.
- Corrected Figure 11 title.
- Added comments to BYPASS and SFOUT registers.

Revision 0.2 to Revision 0.3

- Expanded and improved the specification tables.
- Added comments on when a heat sink is required.

Revision 0.3 to Revision 0.4

Added Silicon Labs logo to device top mark

Revision 0.4 to Revision 0.41

- Corrected Register Map numbering.
- Removed Register 185.

Revision 0.41 to Revision 0.45

- Added comments indicating that a crystal may not be used in place of an external oscillator.
- Updated specification Tables 3, 4, and 5.
- Added maximum jitter specifications to Table 5.
- Added Thermal Characteristics table on page 12.
- Added Figure 3, "Typical Application Schematic," on page 13.
- Added "5. Si5375 Application Examples and Suggestions" on page 16.
- Updated "7. Register Descriptions" on page 21.
- Added a part number for the non-RoHS6 device to "9. Ordering Guide" on page 48.
- Added recommendations on the four reset pins in "5.4. RSTL_x Pins" on page 16.
- Added Lead-Finish top marking.

Revision 0.45 to Revision 1.0

- Updated "Features" on page 1.
- Minor corrections to Tables 2, 3, and 5.



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