



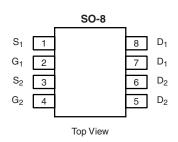
Dual P-Channel 60-V (D-S), 175 °C MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)	
- 60	0.120 at V _{GS} = - 10 V	± 3.1	
- 60	0.150 at V _{GS} = - 4.5 V	± 2.8	

FEATURES

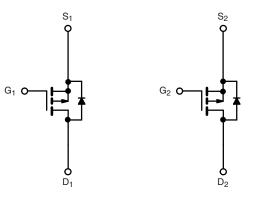
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- 175 °C Maximum Junction Temperature
- Compliant to RoHS Directive 2002/95/EC





Ordering Information: Si4948EY-T1-E3 (Lead (Pb)-free)

Si4948EY-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V_{DS}	- 60	V	
Gate-Source Voltage		V _{GS} ± 20]	
Continuous Drain Current /T 175 °C\a	T _A = 25 °C	. I _D	± 3.1	Α	
Continuous Drain Current (T _J = 175 °C) ^a	T _A = 70 °C		± 2.6		
Pulsed Drain Current		I _{DM}	I _{DM} ± 30		
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.0		
Maniana Panas Dianis ation d	T _A = 25 °C	P _D	2.4	W	
Maximum Power Dissipation ^a	T _A = 70 °C	' D	1.7		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W		

Notes

a. Surface Mounted on FR4 board, $t \le 10 \text{ s.}$

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SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 1			V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zara Cata Valtana Drain Correct	I _{DSS}	V _{DS} = - 60 V, V _{GS} = 0 V			- 2	μΑ
Zero Gate Voltage Drain Current		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 55 °C			- 25	
On-State Drain Current ^b	I _{D(on)}	$V_{DS} \le -5 \text{ V}, V_{GS} = -10 \text{ V}$	- 20			Α
D : 0	D	V _{GS} = - 10 V, I _D = - 3.1 A		0.100	0.120	Ω
Drain-Source On-State Resistance ^D	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 2.8 A		0.125	0.150	
Forward Transconductance ^b	9 _{fs}	$V_{DS} = -15 \text{ V}, I_{D} = -3.1 \text{ A}$		7.5		S
Diode Forward Voltage ^b	V _{SD}	I _S = - 2.0 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Dynamic ^a						
Total Gate Charge	Q_g			16	25	
Gate-Source Charge	Q _{gs}	$V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -3.1 \text{ A}$		4		nC
Gate-Drain Charge	Q _{gd}			1.6		
Turn-On Delay Time	t _{d(on)}			8	15	
Rise Time	t _r	V_{DD} = - 30 V, R_L = 30 Ω		10	20	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1 A, V_{GEN} = - 10 V, R_g = 6 Ω		35	50	ns
Fall Time	t _f]		12	25	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 2.0 A, dl/dt = 100 A/μs		60	90	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Guaranteed by design, not subject to production testing.

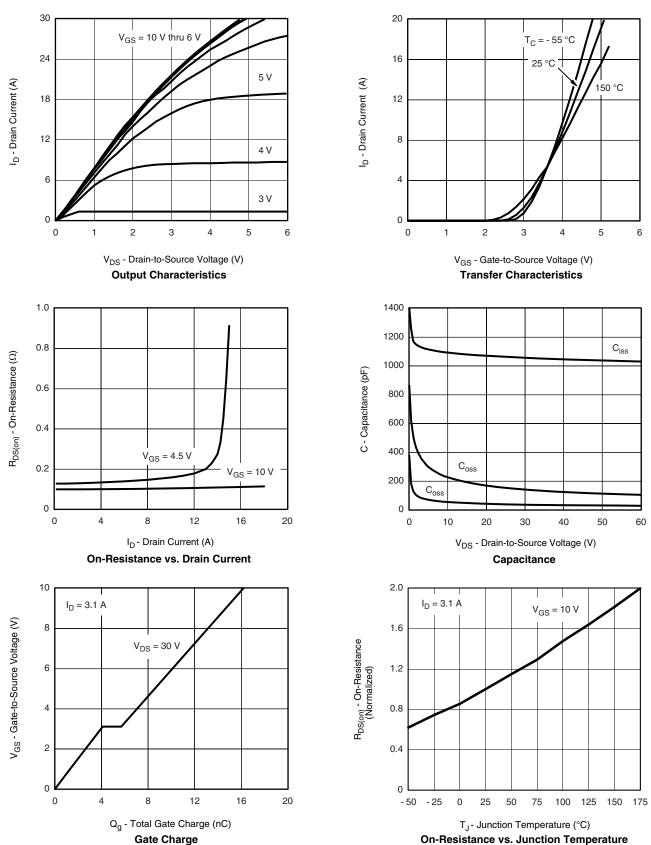
b. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.







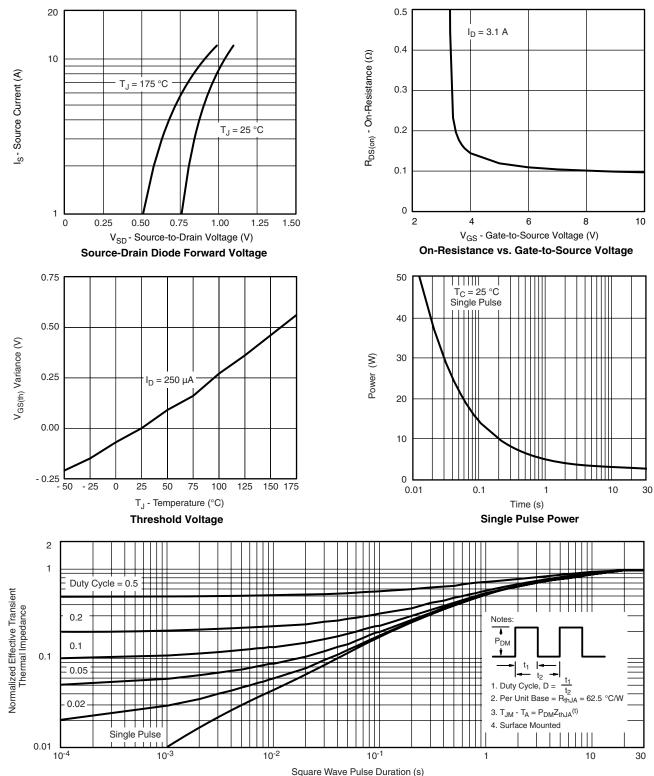
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70166.



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