



## Complementary 20-V (D-S) Low-Threshold MOSFET

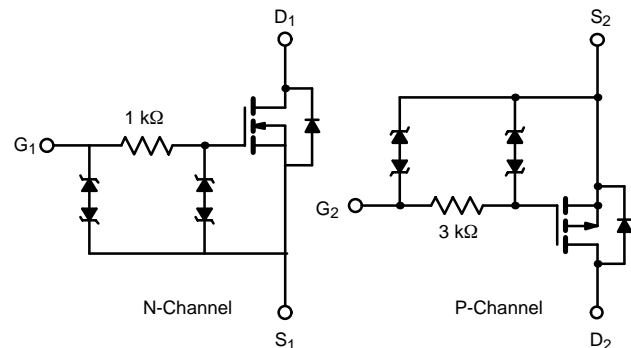
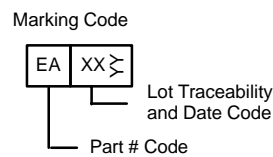
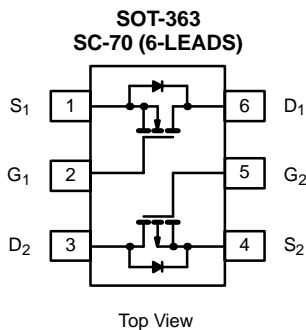
PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.280 @ $V_{GS} = 4.5$ V	1.28
		0.360 @ $V_{GS} = 2.5$ V	1.13
		0.450 @ $V_{GS} = 1.8$ V	1.00
P-Channel	-20	0.490 @ $V_{GS} = -4.5$ V	-1.00
		0.750 @ $V_{GS} = -2.5$ V	-0.81
		1.10 @ $V_{GS} = -1.8$ V	-0.67

## FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- ESD Protected: 2000 V
- Thermally Enhanced SC-70 Package

## APPLICATIONS

- Load Switching
- PA Switch
- Level Switch

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

Parameter	Symbol	N-Channel		P-Channel		Unit	
		5 secs	Steady State	5 secs	Steady State		
Drain-Source Voltage	$V_{DS}$	20		-20		V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$		$\pm 12$		V	
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	1.28	1.13	-1.00	-0.88	A
		$T_A = 85^\circ\text{C}$	0.92	0.81	-0.72	-0.63	
Pulsed Drain Current	$I_{DM}$	4.0		-3.0		A	
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	0.61	0.48	-0.61	-0.48	A	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	0.74	0.57	0.30	0.57	W
		$T_A = 85^\circ\text{C}$	0.38	0.30	0.16	0.3	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150				$^\circ\text{C}$	

## THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 5$ sec	$R_{thJA}$	130	170	$^\circ\text{C/W}$
	Steady State		170	220	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{thJF}$	80	100	$^\circ\text{C/W}$

## Notes

a. Surface Mounted on 1" x 1" FR4 Board.

## Si1563EDH



Vishay Siliconix

New Product

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA	N-Ch	0.45		V	
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -100 μA	P-Ch	-0.45			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±4.5 V	N-Ch		±1	μA	
			P-Ch		±1		
		V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	N-Ch		±10	mA	
			P-Ch		±10		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V	N-Ch		1	μA	
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V	P-Ch		-1		
		V <sub>DS</sub> = 16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C	N-Ch		5		
		V <sub>DS</sub> = -16 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C	P-Ch		-5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	2		A	
		V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-2			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.13 A	N-Ch		0.220	0.280	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.88 A	P-Ch		0.400	0.490	
		V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 0.99 A	N-Ch		0.281	0.360	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -0.71 A	P-Ch		0.610	0.750	
		V <sub>GS</sub> = 1.8 V, I <sub>D</sub> = 0.20 A	N-Ch		0.344	0.450	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -0.20 A	P-Ch		0.850	1.10	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.13 A	N-Ch		2.6	S	
		V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.88 A	P-Ch		1.5		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 0.48 A, V <sub>GS</sub> = 0 V	N-Ch		0.8	1.2	V
		I <sub>S</sub> = -0.48 A, V <sub>GS</sub> = 0 V	P-Ch		-0.8	-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.13 A P-Channel V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -0.88 A	N-Ch		0.65	1.0	nC
Gate-Source Charge	Q <sub>gs</sub>		N-Ch		0.2		
			P-Ch		0.3		
Gate-Drain Charge	Q <sub>gd</sub>	N-Ch		0.23			
		P-Ch		0.3			
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 10 V, R <sub>L</sub> = 20 Ω I <sub>D</sub> ≅ 0.5 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω P-Channel V <sub>DD</sub> = -10 V, R <sub>L</sub> = 20 Ω I <sub>D</sub> ≅ -0.5 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω	N-Ch		45	70	ns
			P-Ch		150	230	
Rise Time	t <sub>r</sub>		N-Ch		85	130	
			P-Ch		480	720	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		350	530	
			P-Ch		840	1200	
Fall Time	t <sub>f</sub>	N-Ch		210	320		
		P-Ch		850	1200		

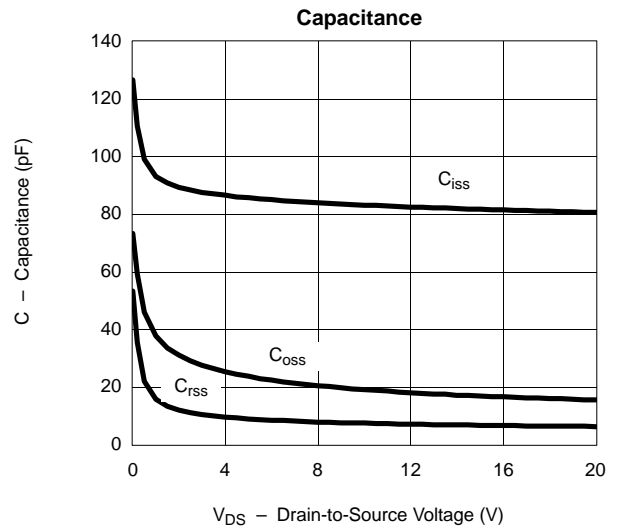
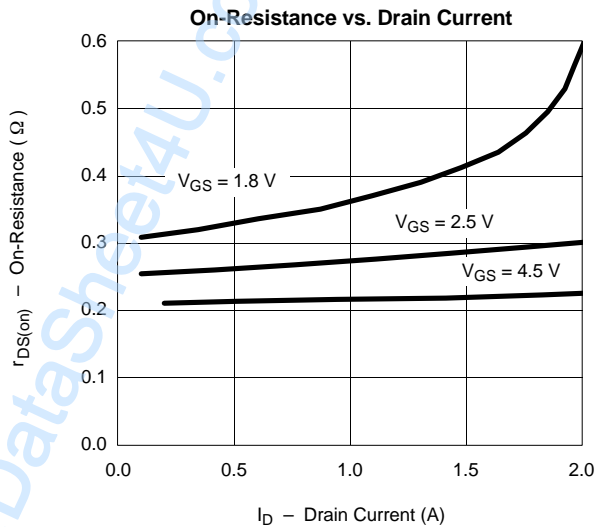
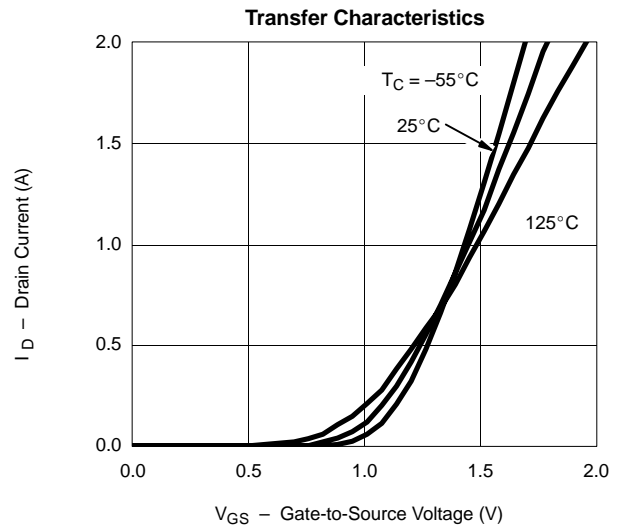
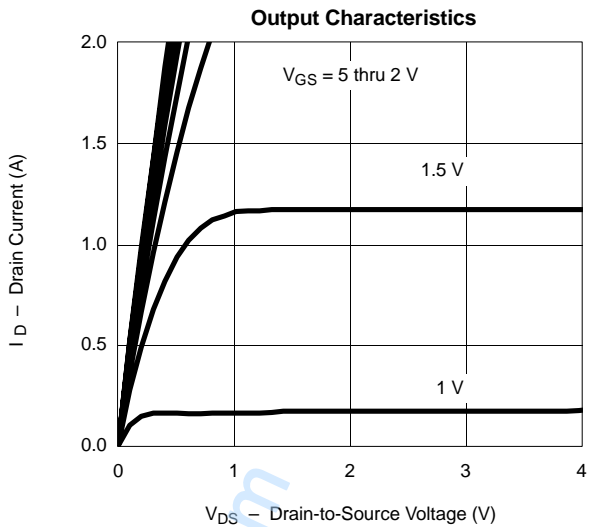
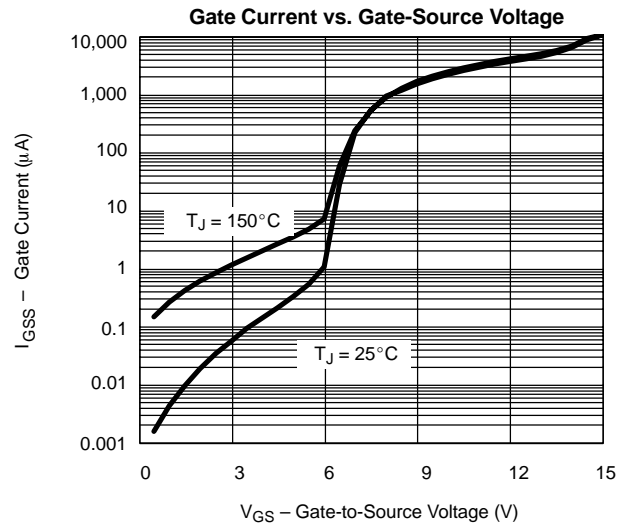
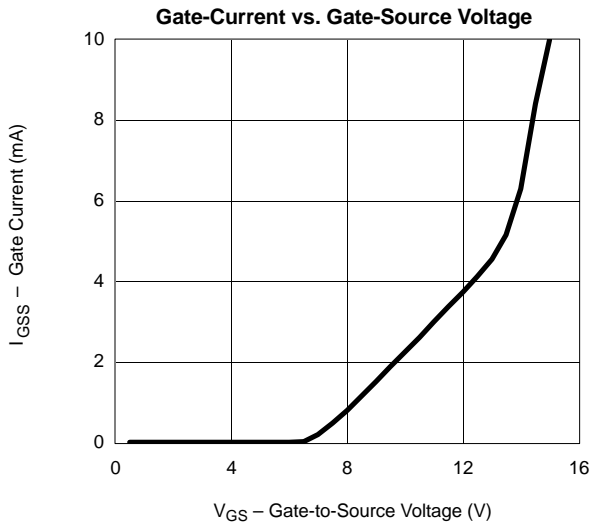
## Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.  
b. Guaranteed by design, not subject to production testing.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



# Si1563EDH

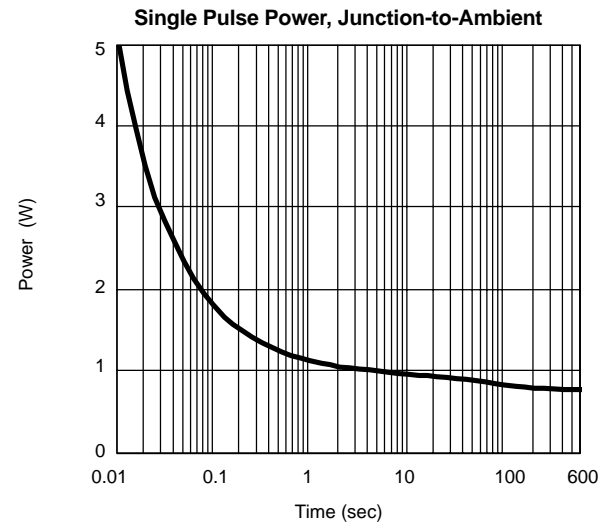
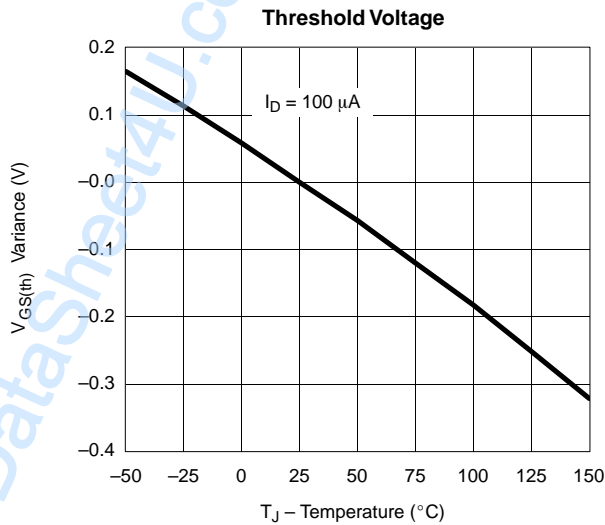
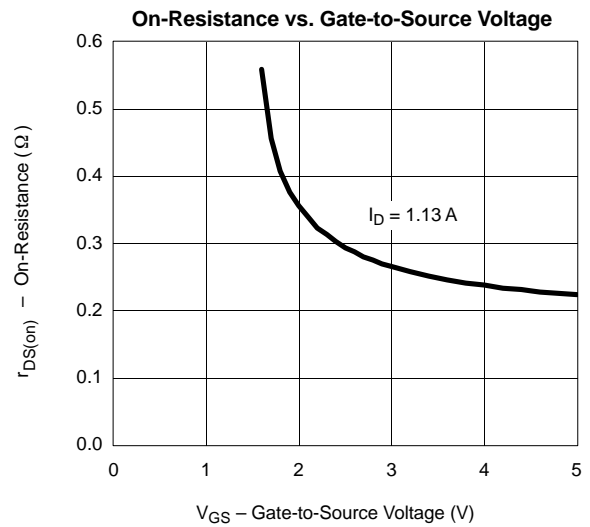
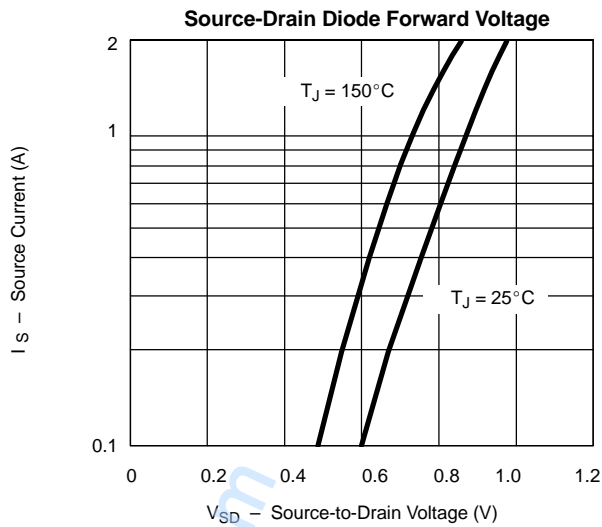
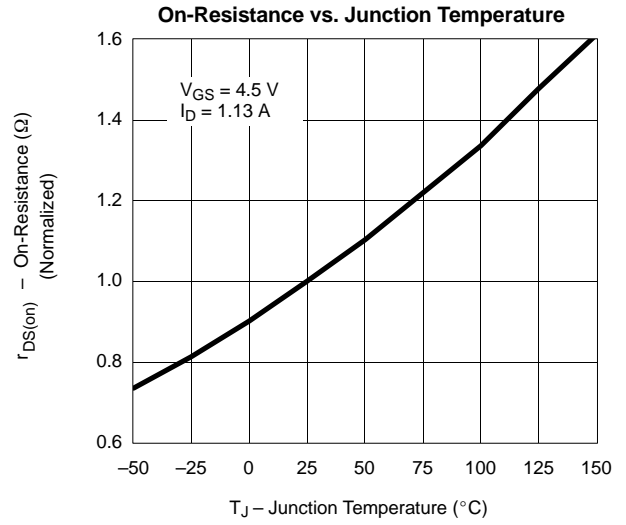
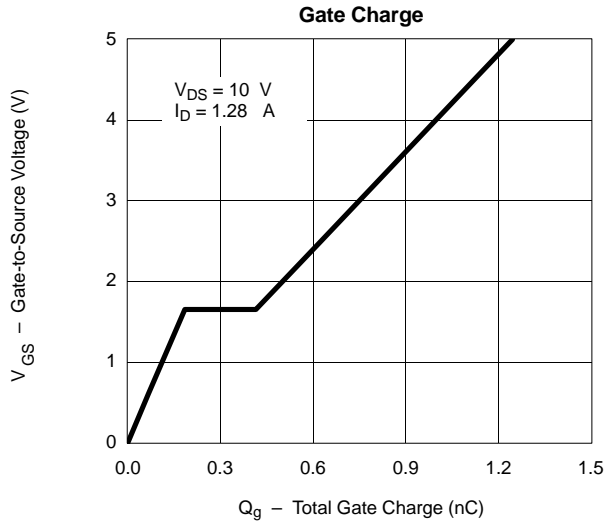


Vishay Siliconix

New Product

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

## N-CHANNEL

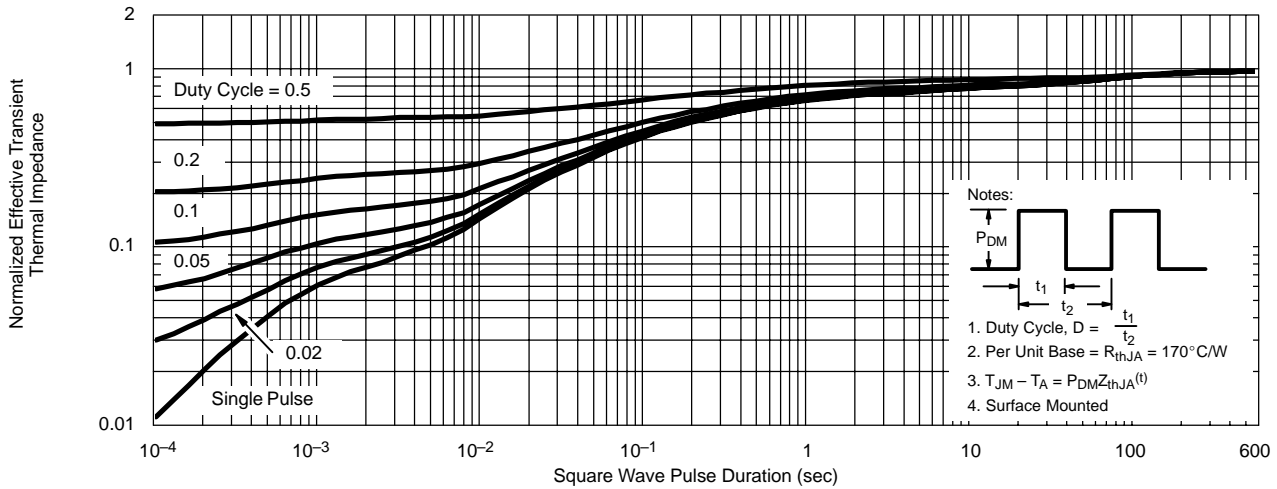




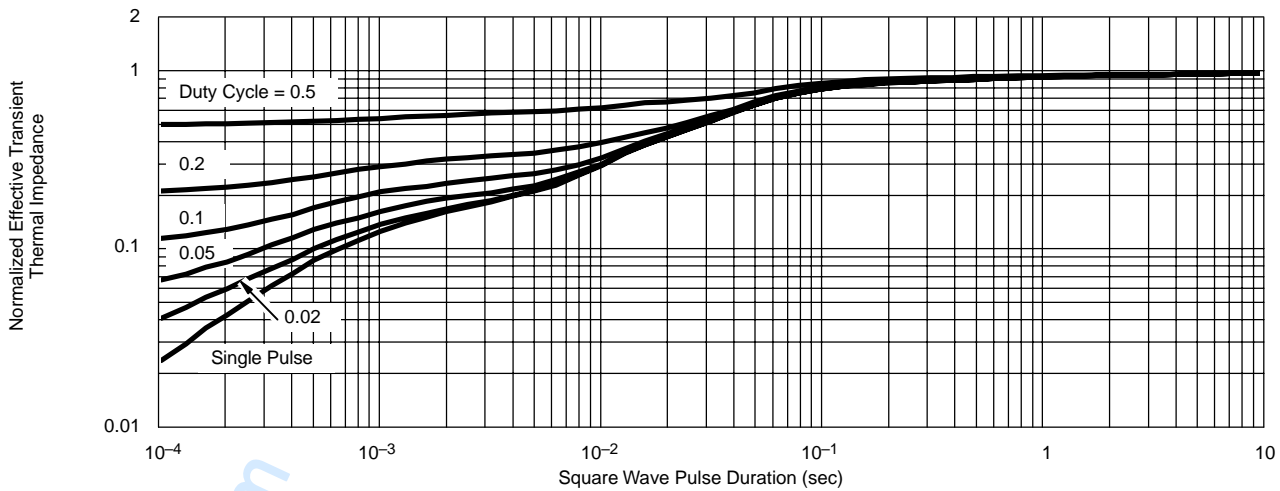
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**

Normalized Thermal Transient Impedance, Junction-to-Ambient



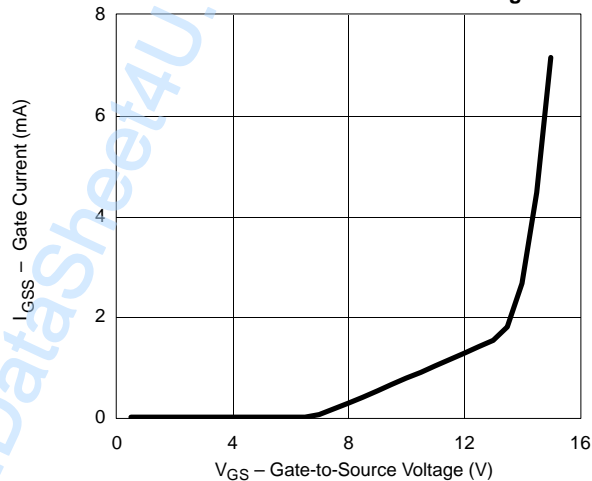
Normalized Thermal Transient Impedance, Junction-to-Foot



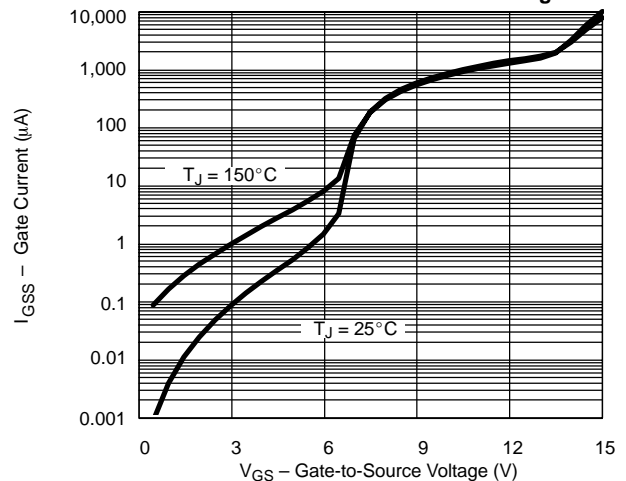
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**

Gate Current vs. Gate-Source Voltage



Gate Current vs. Gate-Source Voltage



# Si1563EDH

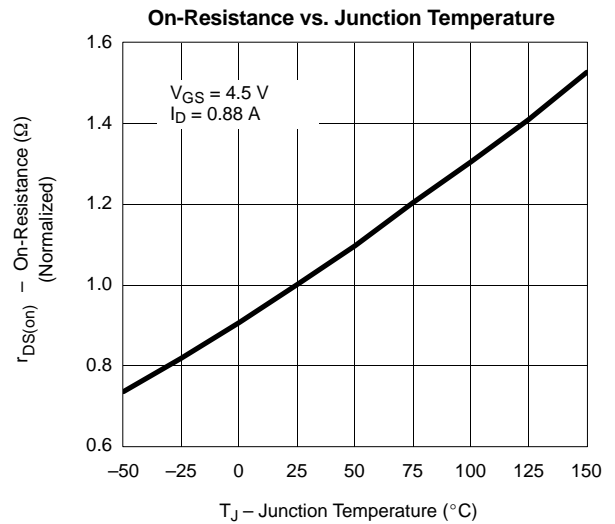
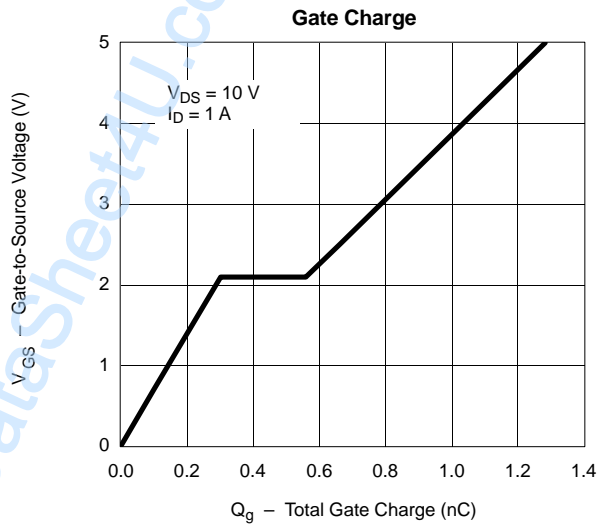
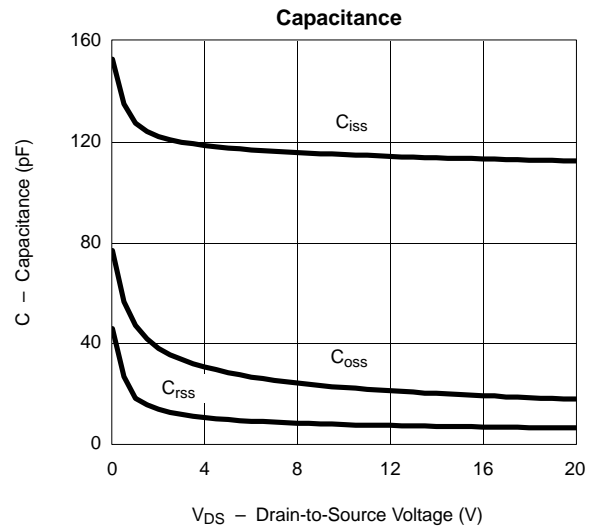
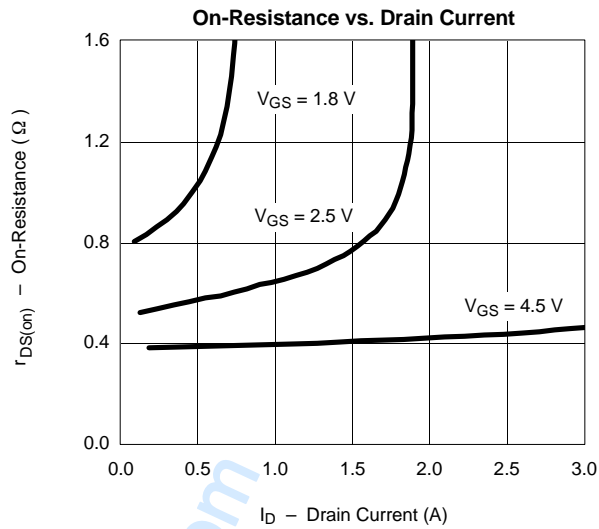
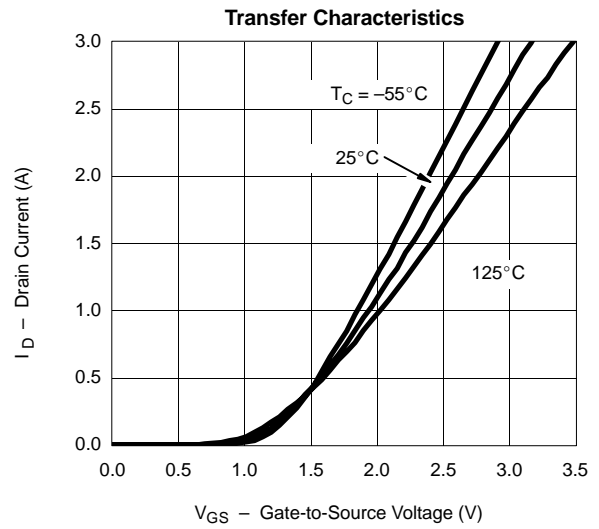
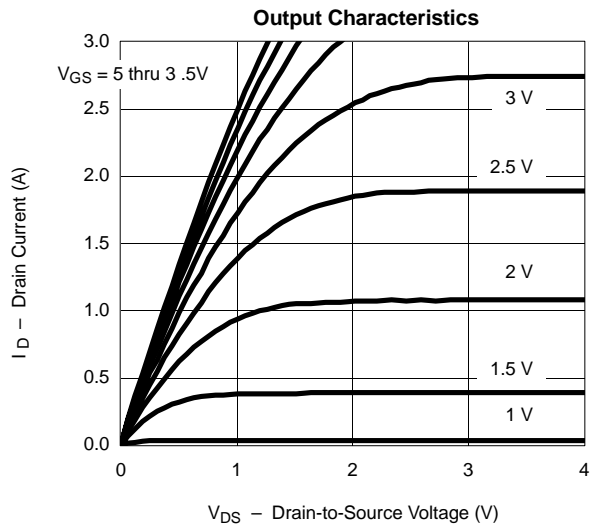


Vishay Siliconix

New Product

## TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

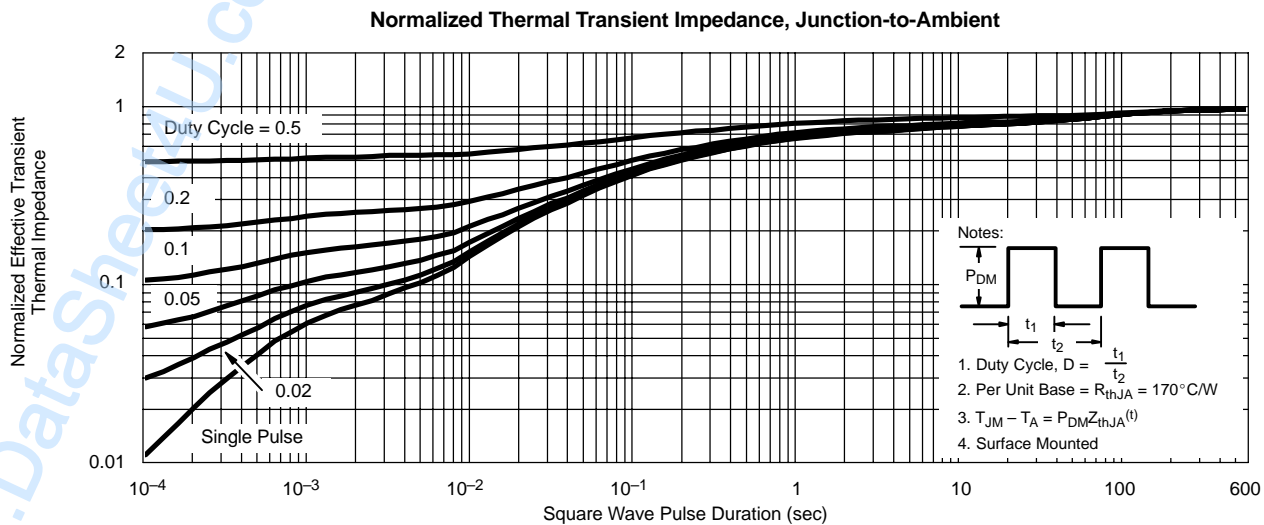
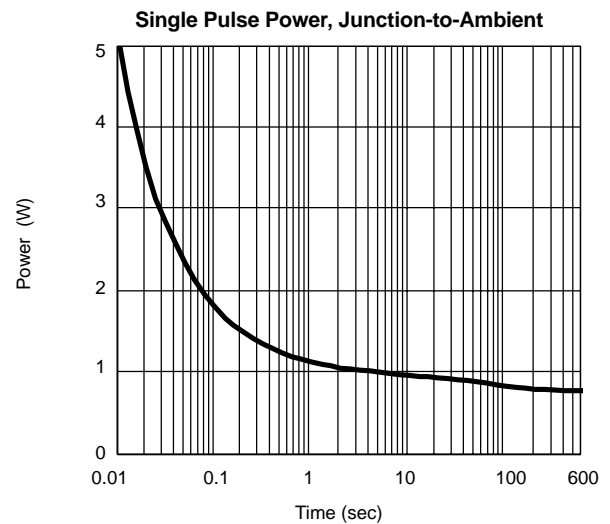
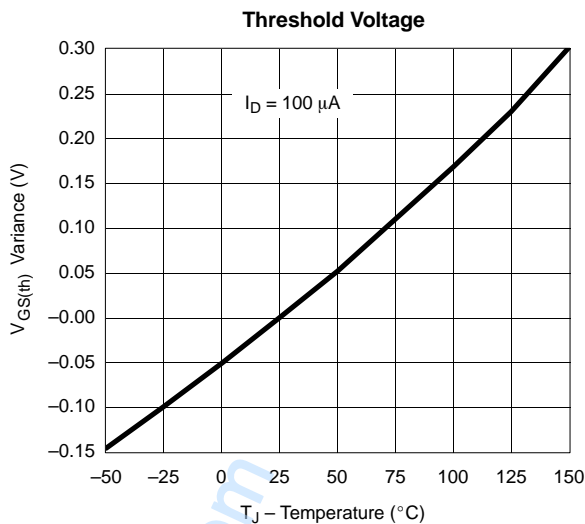
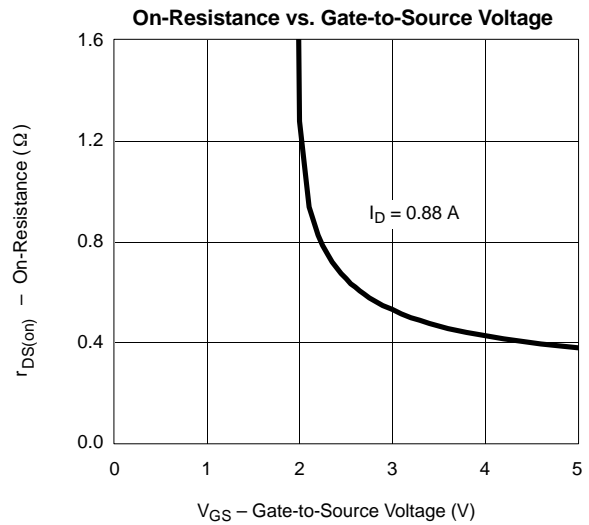
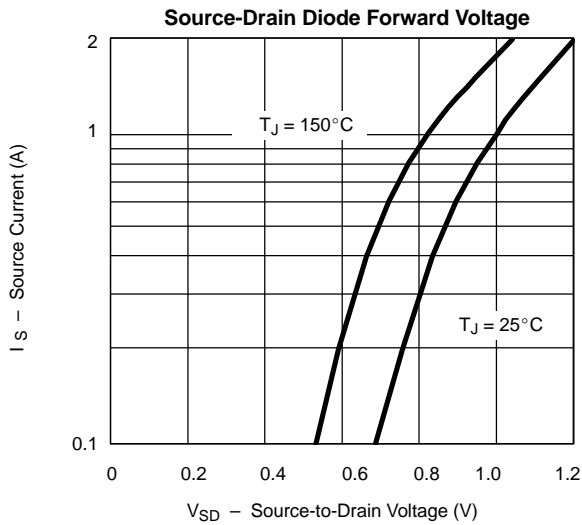
P-CHANNEL





**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**



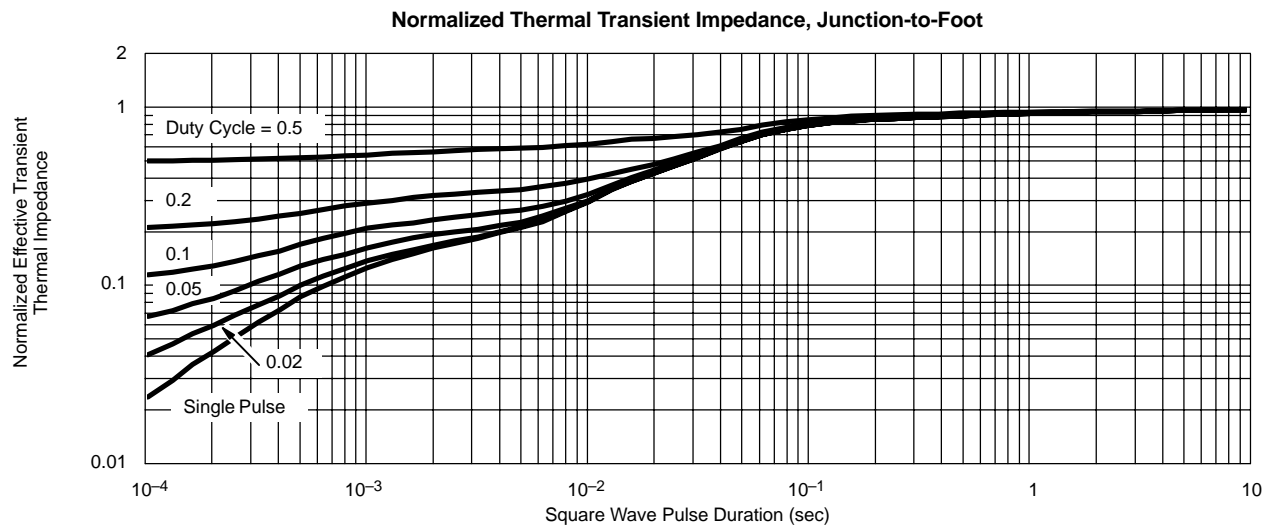
# Si1563EDH



Vishay Siliconix

New Product

## TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



www.DataSheet4U.com





www