

P-Channel 150-V (D-S) MOSFET



Product Is
Completely
Pb-free

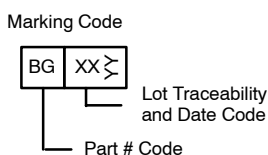
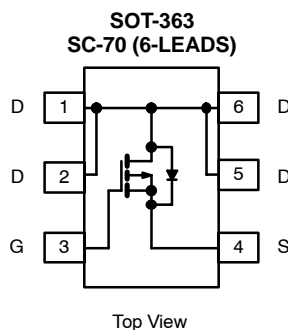
PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)	Q _g (Typ)
-150	2.6 @ V _{GS} = -10 V	-0.52	4.2 nC
	2.7 @ V _{GS} = -6 V	-0.51	

FEATURES

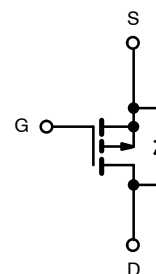
- TrenchFET® Power MOSFETS
- Small, Thermally Enhanced SC-70 Package
- Ultra Low On-Resistance

APPLICATIONS

- Active Clamp Circuits in DC/DC Power Supplies



Ordering Information: Si1411DH-T1—E3



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	-150		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	-0.52	-0.42	A
	T _A = 85°C		-0.38	-0.3	
Pulsed Drain Current		I _{DM}	-0.8		
Continuous Diode Current (Diode Conduction) ^a		I _S	-1.3	-0.83	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	-2.1		
Single Pluse Avalanch Energy		E _{AS}	0.22		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	1.56	1.0	W
	T _A = 85°C		0.81	0.52	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 5 sec	R _{thJA}	60	80	°C/W
	Steady State		100	125	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	34	45	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

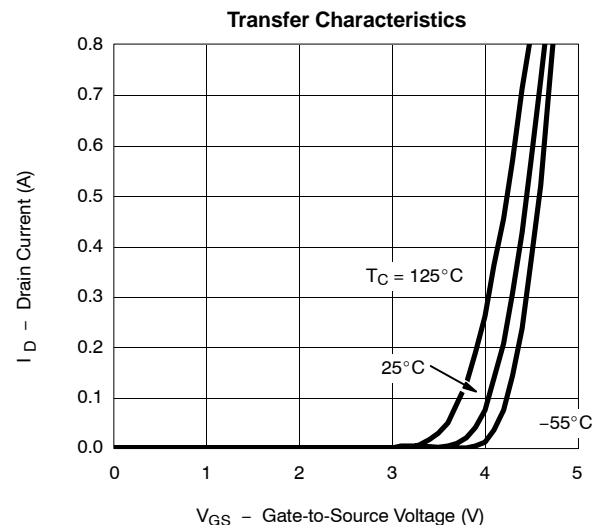
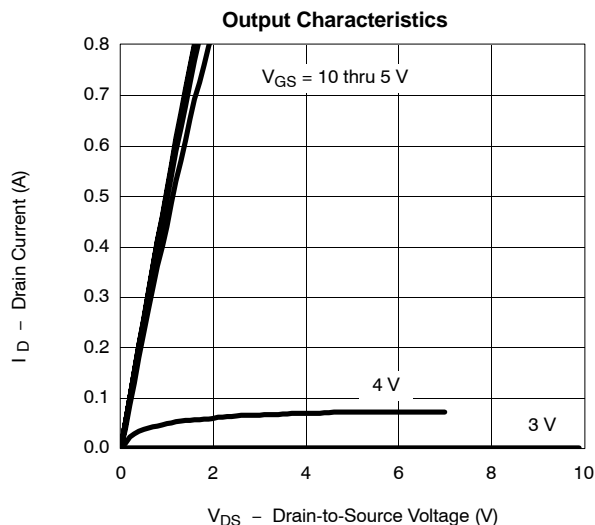
**SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -100\ \mu\text{A}$	-2.5		-4.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -150\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -150\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}$	-0.8			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -0.5\ \text{A}$		2.05	2.6	Ω
		$V_{GS} = -6\ \text{V}, I_D = -0.5\ \text{A}$		2.14	2.7	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -0.5\ \text{A}$		1.5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.4\ \text{A}, V_{GS} = 0\ \text{V}$		-0.80	-1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -75\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -0.5\ \text{A}$		4.2	6.3	nC
Gate-Source Charge	Q_{gs}			0.9		
Gate-Drain Charge	Q_{gd}			1.3		
Gate Resistance	R_g	$f = 1.0\ \text{MHz}$		8.5		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75\ \text{V}, R_L = 75\ \Omega$ $I_D \approx -1\ \text{A}, V_{GEN} = -4.5\ \text{V}, R_g = 6\ \Omega$		4.5	7	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			9	14	
Fall Time	t_f			11	17	
Reverse Recovery Time	t_{rr}	$I_F = -0.5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		36	55	
Body Diode Reverse Recovery Charge	Q_{rr}			65	100	nC

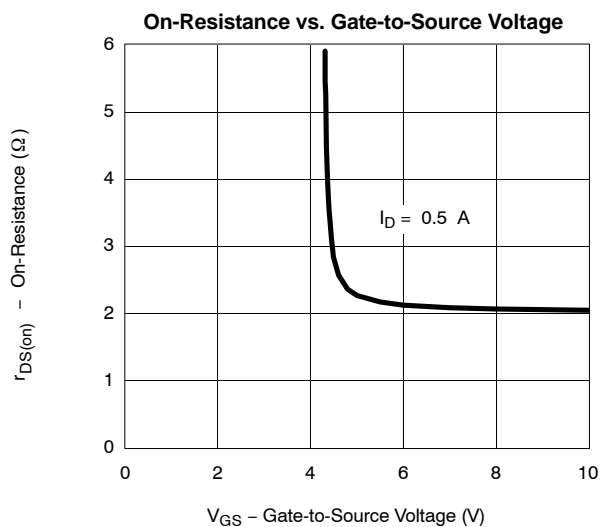
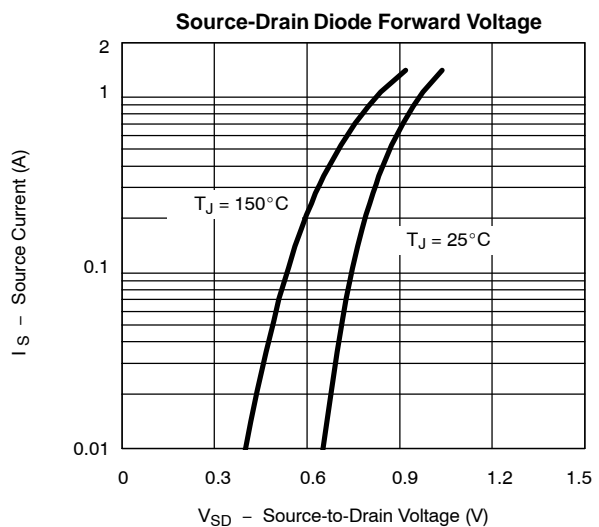
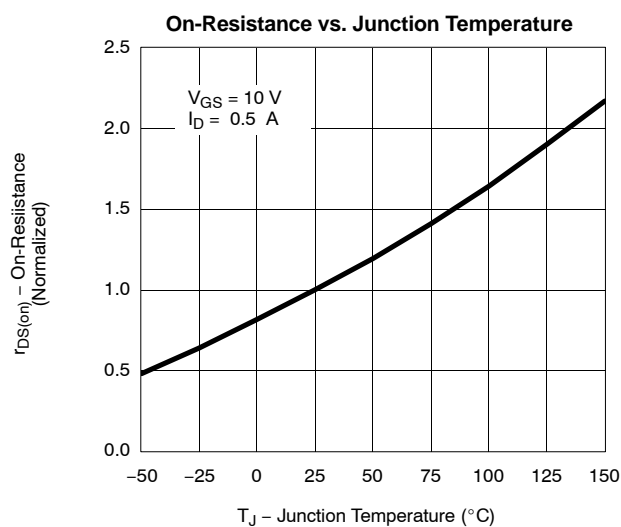
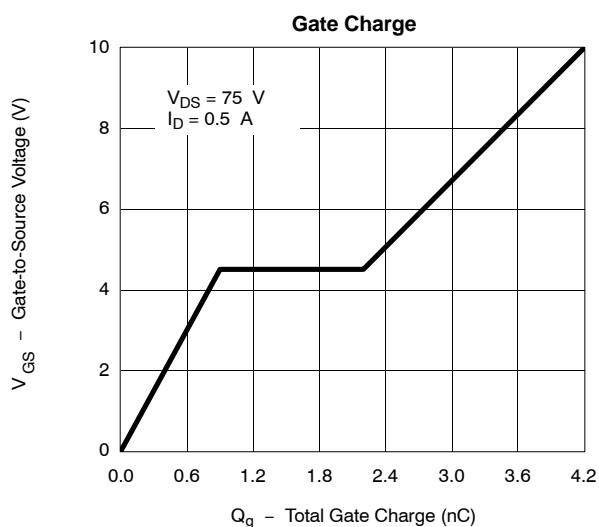
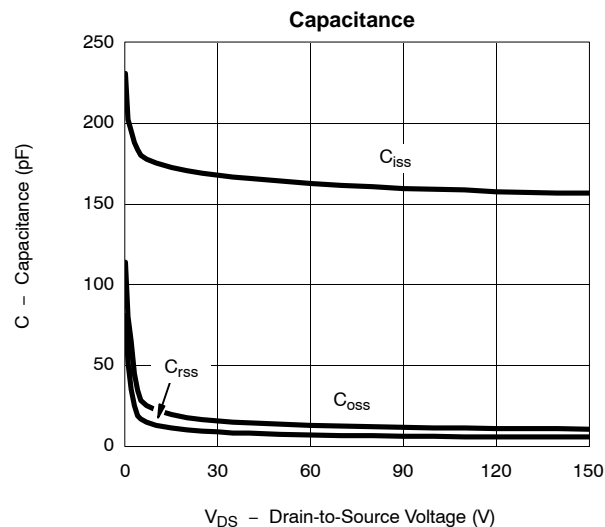
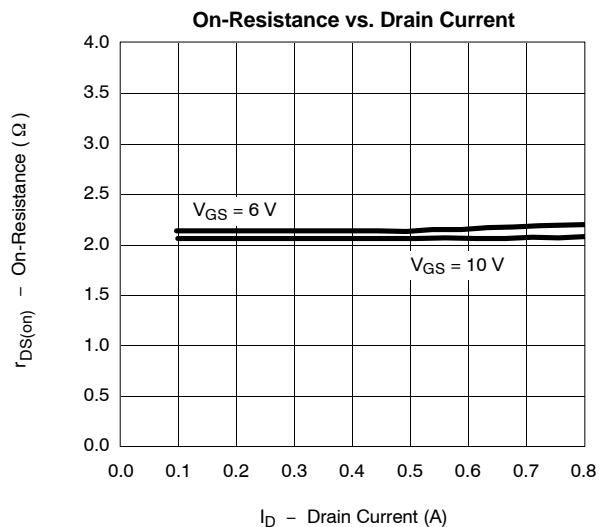
Notes

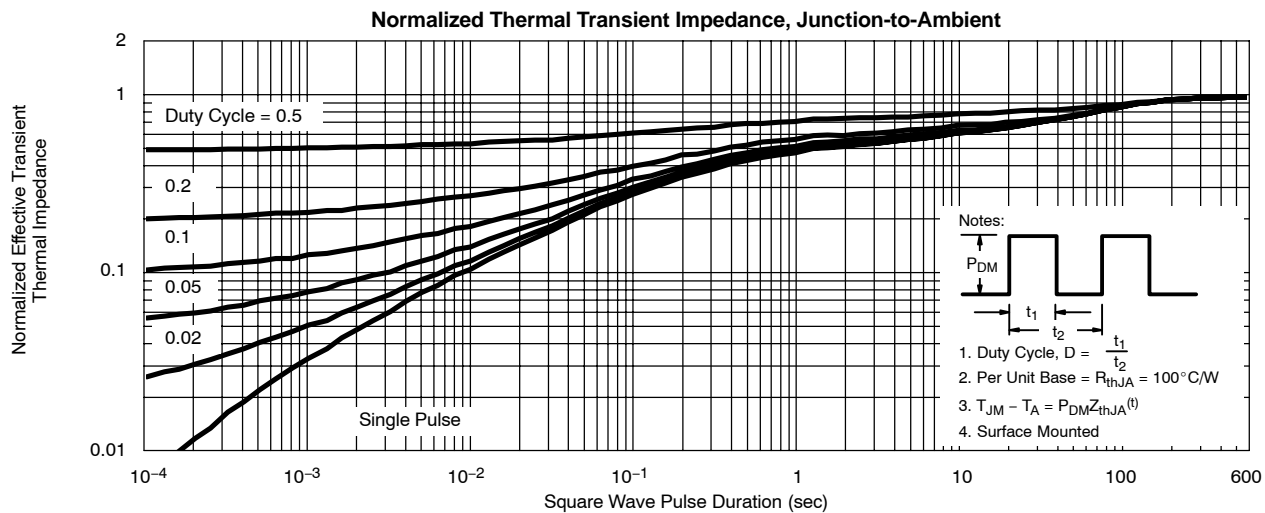
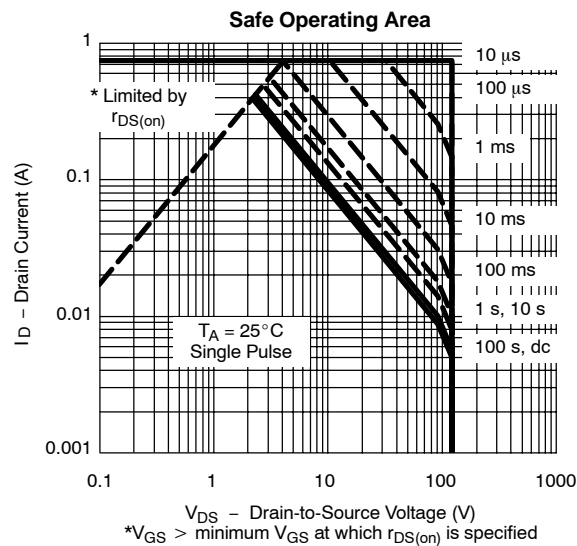
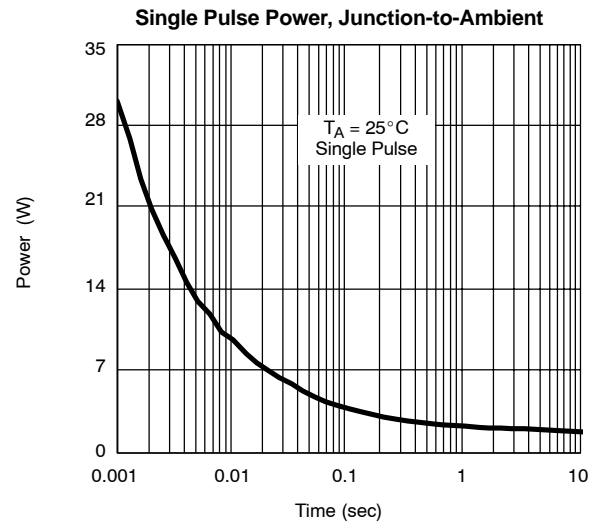
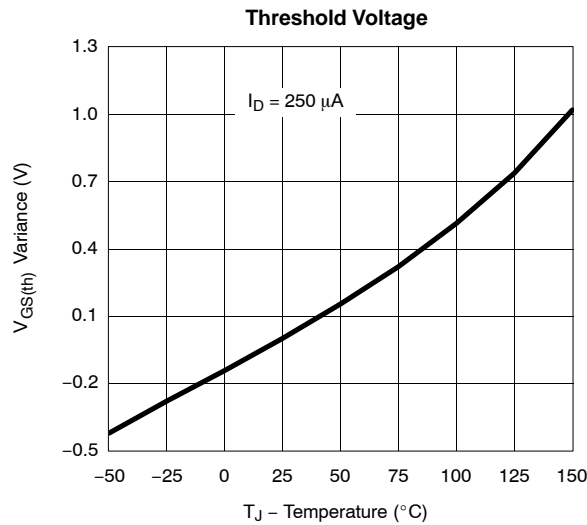
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

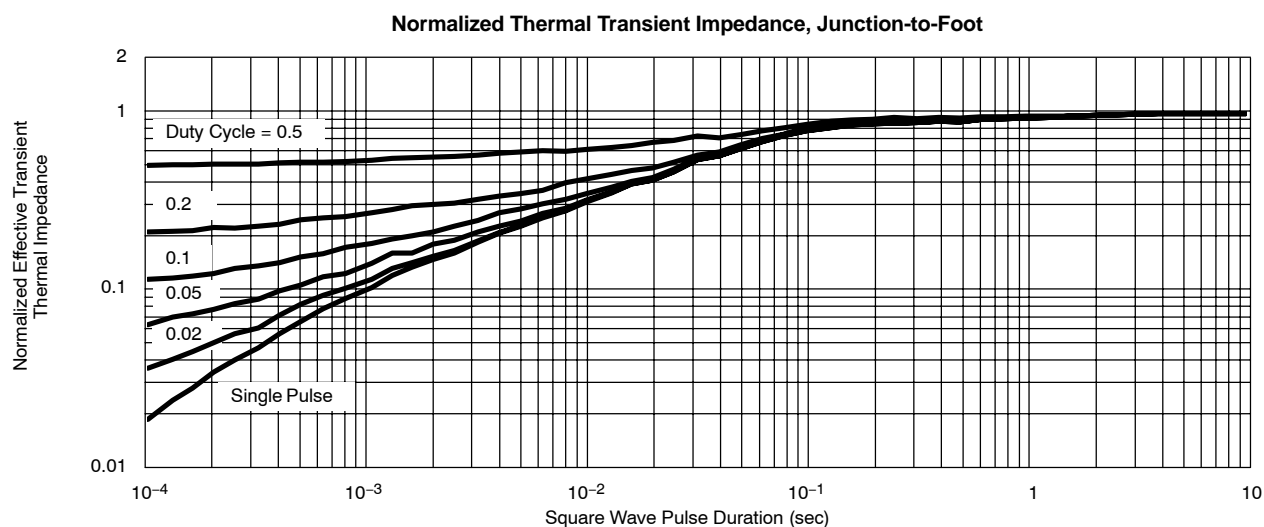
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