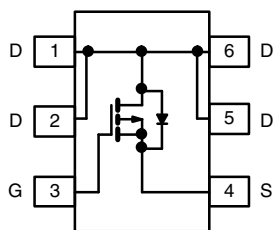


## P-Channel 1.8 V (G-S) MOSFET

### PRODUCT SUMMARY

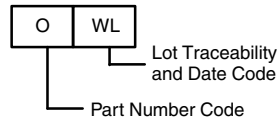
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
- 12	0.165 at $V_{GS} = - 4.5$ V	- 0.95
	0.220 at $V_{GS} = - 2.5$ V	- 0.82
	0.280 at $V_{GS} = - 1.8$ V	- 0.67

### SC-89 (6-LEADS)



Top View

### Marking Code



**Ordering Information:** Si1039X-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- TrenchFET® Power MOSFET
- Low Threshold
- Smallest LITTLE FOOT® Package: 1.6 mm x 1.6 mm
- Low 0.6 mm Profile
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Cell Phones and Pagers
- Load Switch

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	5 s	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	- 12		V
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current ( $T_J = 150$ °C) <sup>a</sup>	$I_D$	- 0.95	- 0.87	A
		- 0.76	- 0.69	
Pulsed Drain Current	$I_{DM}$	- 4		
Continuous Diode Current (Diode Conduction) <sup>a</sup>	$I_S$	- 0.18	- 0.14	
Maximum Power Dissipation <sup>a</sup>	$P_D$	0.21	0.17	W
		0.13	0.10	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150		°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	500	600	°C/W
		600	720	

Notes:

a. Surface mounted on 1" x 1" FR4 board with minimum copper.

**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

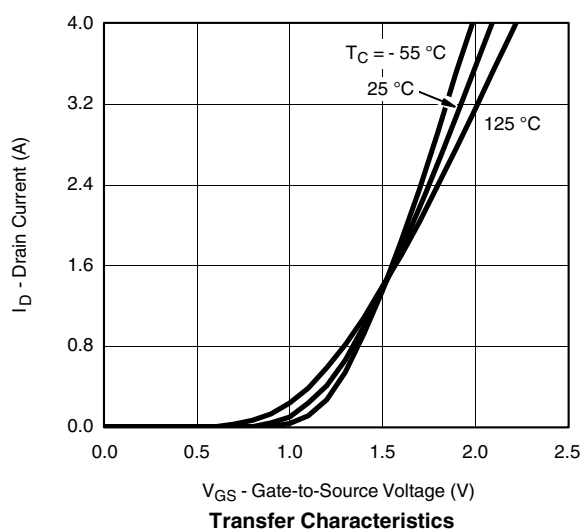
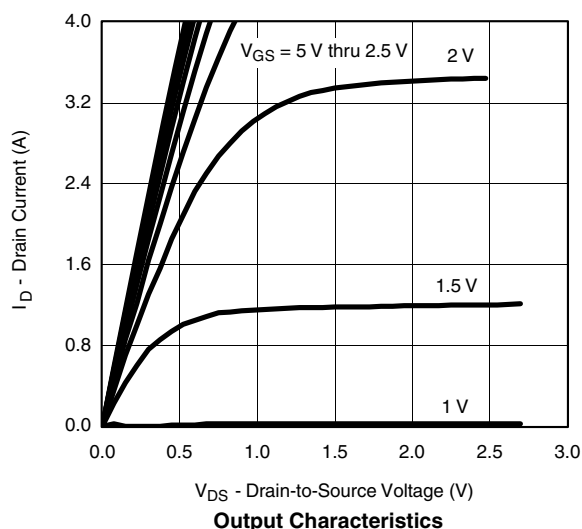
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	-0.45			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 8\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -12\text{ V}$ , $V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -12\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^{\circ}\text{C}$			-5	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\text{ V}$ , $V_{GS} = -4.5\text{ V}$	-4			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$ , $I_D = -0.87\text{ A}$		0.140	0.165	$\Omega$
		$V_{GS} = -2.5\text{ V}$ , $I_D = -0.75\text{ A}$		0.180	0.220	
		$V_{GS} = -1.8\text{ V}$ , $I_D = -0.2\text{ A}$		0.230	0.280	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}$ , $I_D = -0.87\text{ A}$		3.5		S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -0.14\text{ A}$ , $V_{GS} = 0\text{ V}$		-0.78	-1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = -6\text{ V}$ , $V_{GS} = -4.5\text{ V}$ , $I_D = -0.87\text{ A}$		3.8	6	nC
Gate-Source Charge	$Q_{gs}$			0.7		
Gate-Drain Charge	$Q_{gd}$			0.8		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6\text{ V}$ , $R_L = 12\text{ }\Omega$ $I_D \cong -0.5\text{ A}$ , $V_{GEN} = -4.5\text{ V}$ , $R_g = 6\text{ }\Omega$		15	30	ns
Rise Time	$t_r$			20	40	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	$t_f$			16	30	
Source-Drain Reverse Recovery Time	$t_{rr}$			20	40	

Notes:

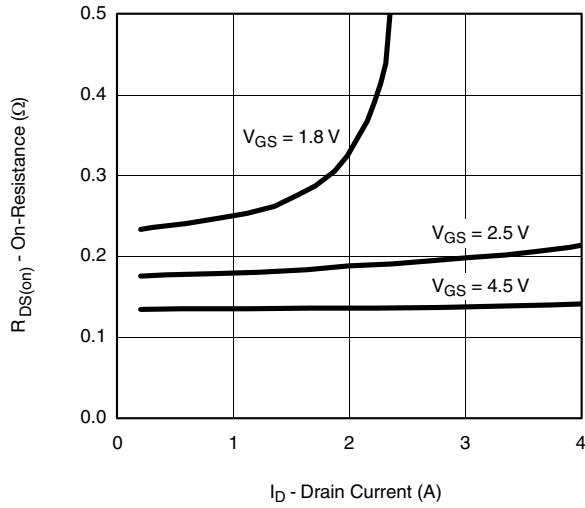
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

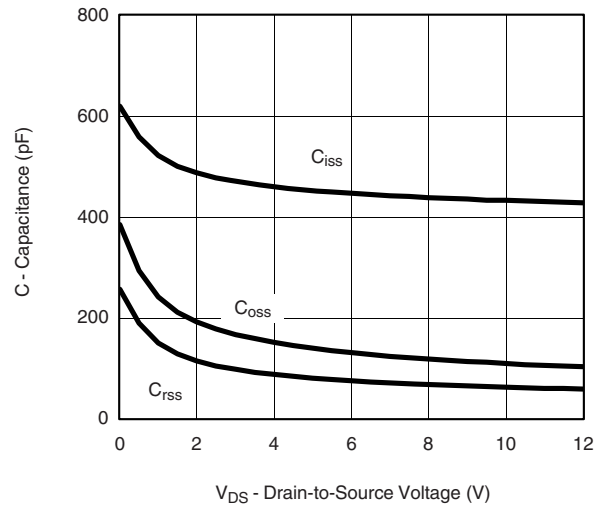
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** ( $25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

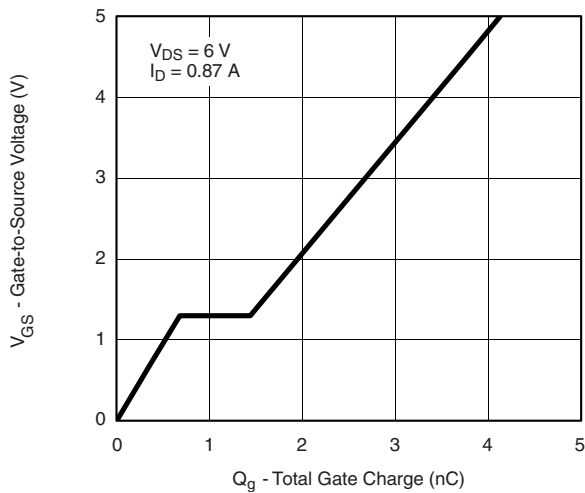
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



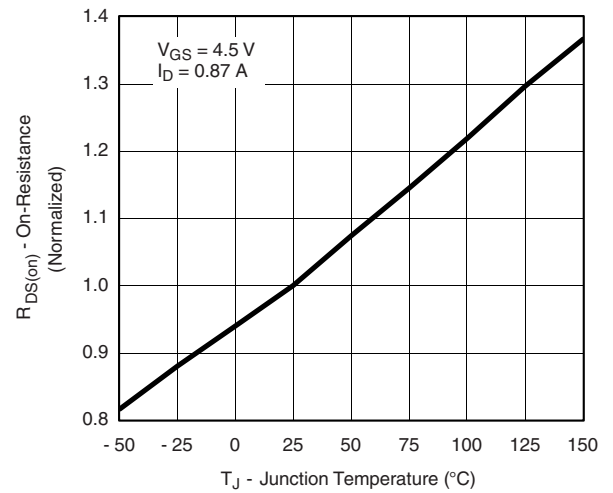
On-Resistance vs. Drain Current



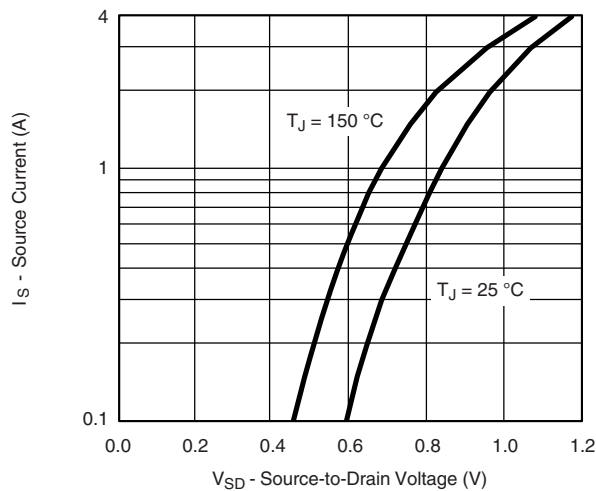
Capacitance



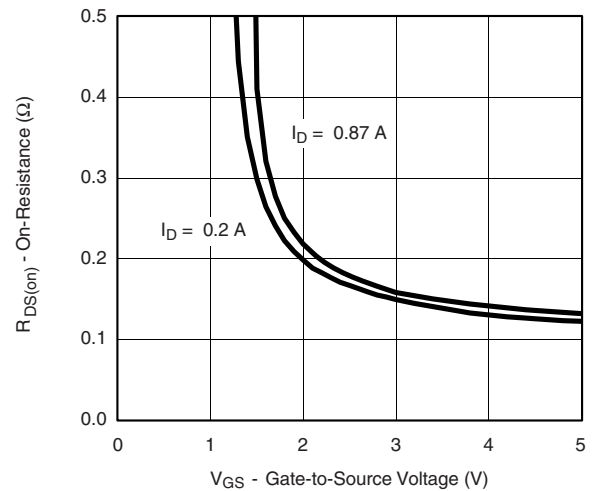
Gate Charge



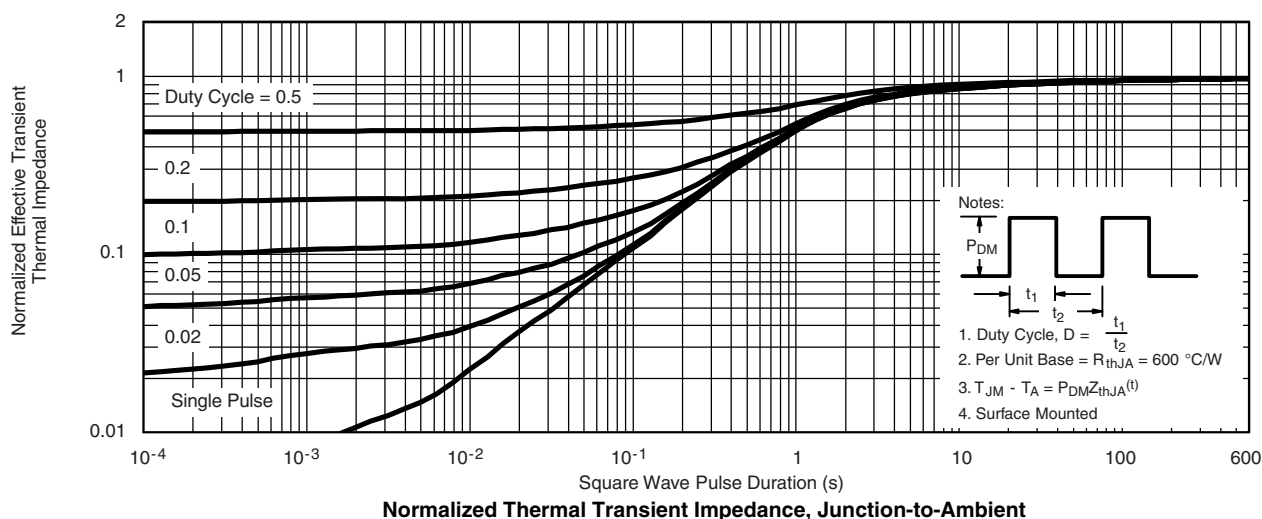
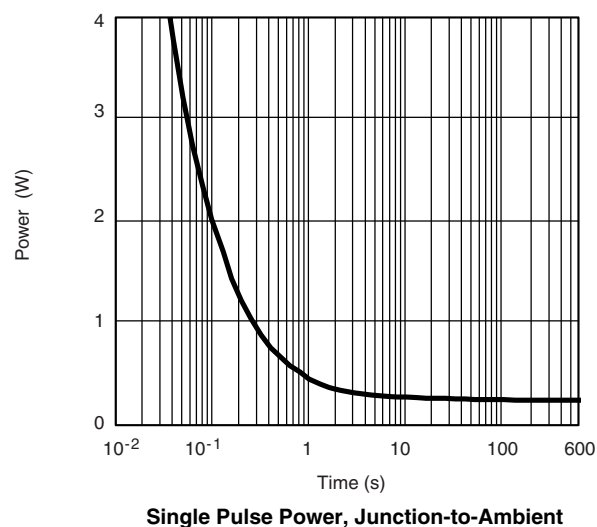
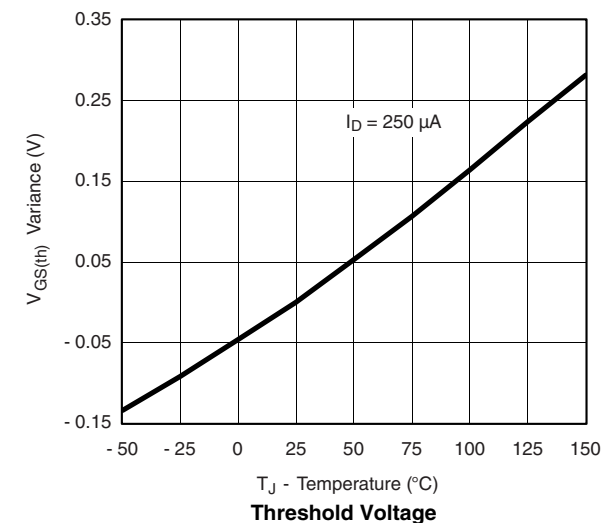
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

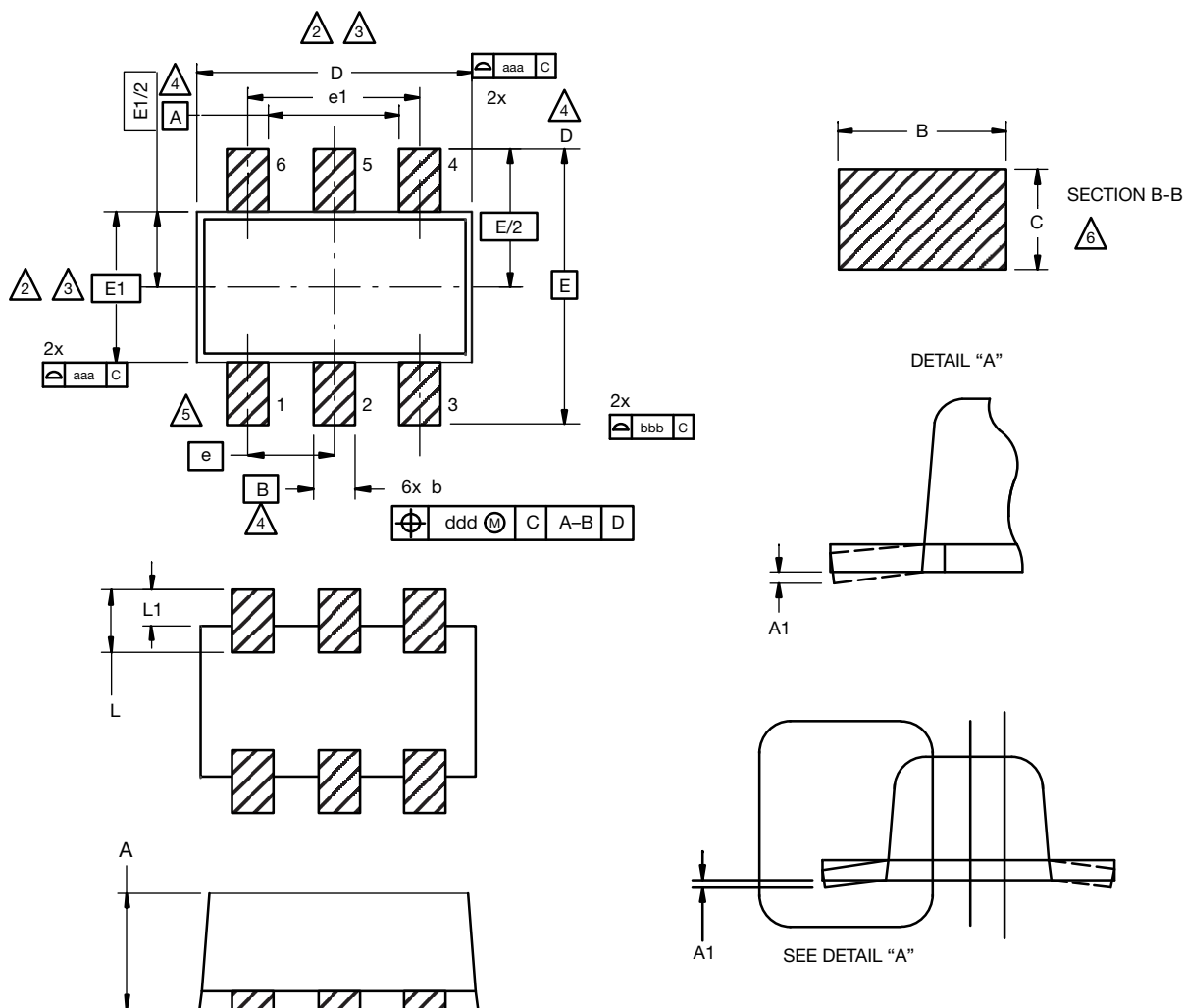


On-Resistance vs. Gate-to-Source Voltage

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70682](http://www.vishay.com/ppg?70682).

## SC-89 6-Leads (SOT-563F)



## Notes

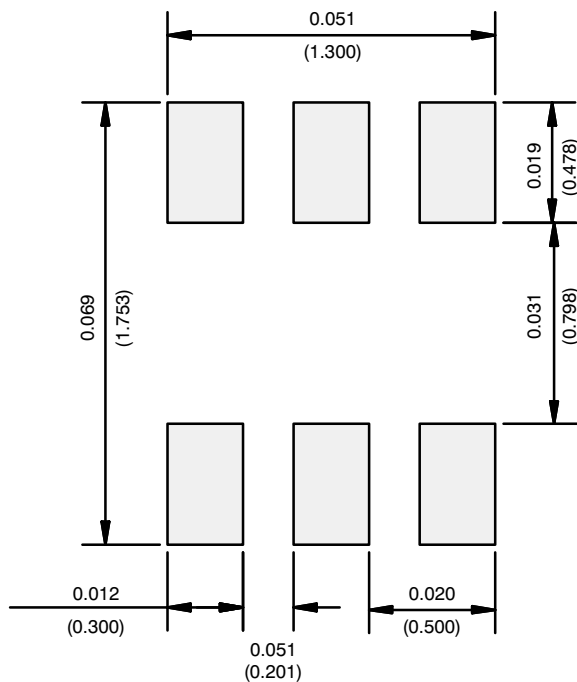
1. Dimensions in millimeters.

- ② Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- ③ Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- ④ Datums A, B and D to be determined 0.10 mm from the lead tip.
- ⑤ Terminal numbers are shown for reference only.
- ⑥ These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14  
DWG: 5880

## RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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