

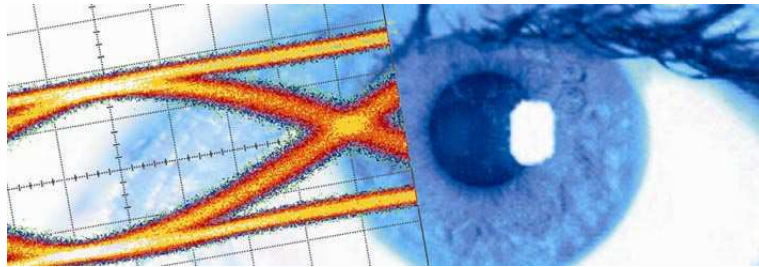


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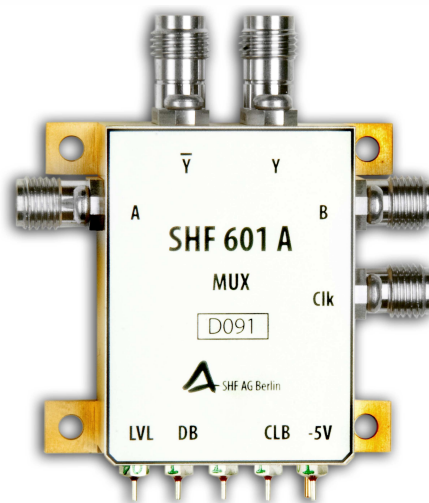


Datasheet

SHF 601 A

60 Gbps

2:1 Multiplexer





Description

The SHF 601 A is a 2:1 Multiplexer operating at data rates up to 60 Gbps for use in broadband test setups and telecom transmission systems. Two 30 Gbps single ended serial data streams are accepted by the multiplexer and converted into one differential data signal at a nominal output data rate of 60 Gbps. A single ended clock signal (nominally 30 GHz) with a frequency half of the output data rate drives the SHF 601 A. All in- and output ports are AC-coupled. Unused in- or output ports should be terminated.

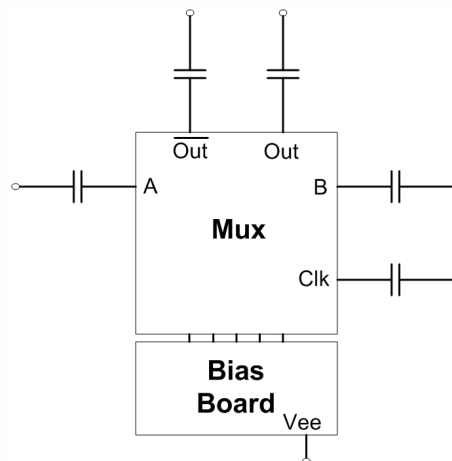
Features

- Broadband operation up to 60 Gbps
- Differential data output, 650mV single ended output swing
- Single ended clock and data inputs

Applications

- 100G Ethernet development and prototyping
- OC-768 / STM-256 applications
- Telecom transmission
- Fibre Channel
- Broadband test and measurement equipment

Block Diagram



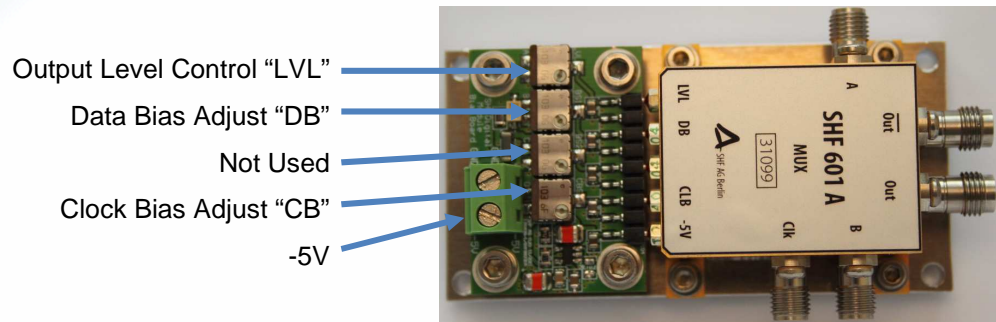


Bias Board

At delivery, the bias board is mounted on a common base plate, together with the SHF 601 A MUX. When using the bias board only one supply voltage of -5V needs to be applied; all operating voltages will be provided by the bias board.

With the factory settings all bias voltages are set to optimum / maximum output voltage. However, if required the customer can adjust the output level "LVL", the input data bias voltage "DB" and the clock bias voltage "CB" with the appropriate trim potentiometers on the bias board.

For system applications it is possible to remove the bias board. In that case the operating voltages have to be supplied by the customer's circuitry.





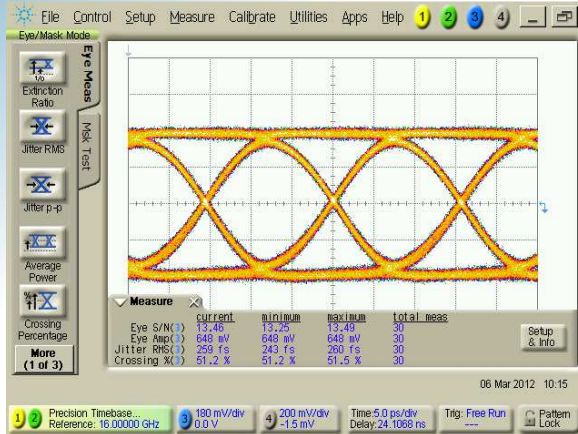
Specifications

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Input Parameters						
Data Input Voltage	$V_{data\ in}$	mV	200		1000	
Clock Input Frequency	f_{in}	GHz	1		30	
Clock Input Voltage	$V_{clk\ in}$	mV _{pp}	300		1000	
Output Parameters						
Minimum Output Data Rate	$R_{in,min}$	Gbps		1	2	@ 500mV _{pp} clock input
Maximum Output Data Rate	$R_{in,max}$	Gbps	60	64		@ 500mV _{pp} clock input
Output Amplitude	V_{out}	mV		630	800	Single ended
Rise / Fall time	t_r/t_f	ps		8		20% / 80%
Output Jitter, RMS value	J_{rms}	fs		350	500	depends on jitter of clock input signal
Power Requirements						
Supply Voltage	V_{ee}	V	-4.8	-5	-5.2	
Supply Current	I_{ee}	mA		430	460	
Power Dissipation	P_d	mW		2150		@ $V_{EE} = -5V$; incl. Bias Board
Bias Voltages						
Output Level Adjust	V	LVL	-3.3		0	if not used, connect to gnd
Input Data Bias	DB	V	-3.3	-1,65	0	
Clock Bias	CB	V	-3.3	-1,65	0	
Conditions						
Operating Temperature	$T_{ambient}$	°C	15		35	

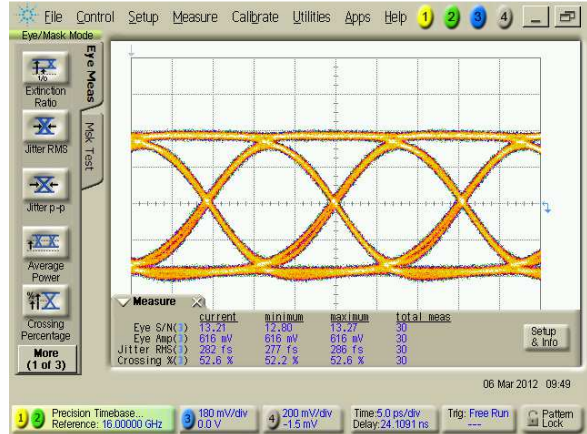


Typical Output Eye Diagrams

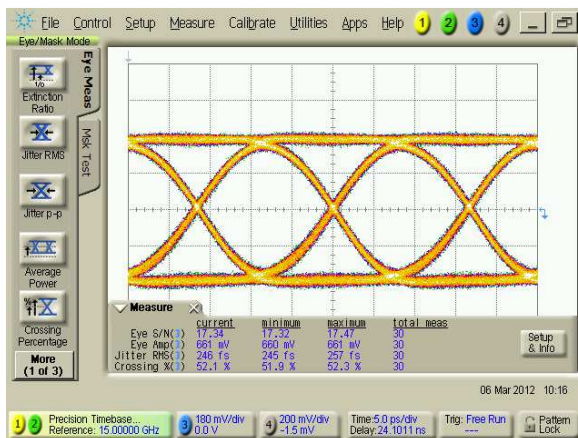
The measurements below had been performed using a SHF 12103 B BPG (PRBS $2^{31}-1$) and an Agilent 86100D DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The outputs of the multiplexer module had been connected directly to the DCA input.



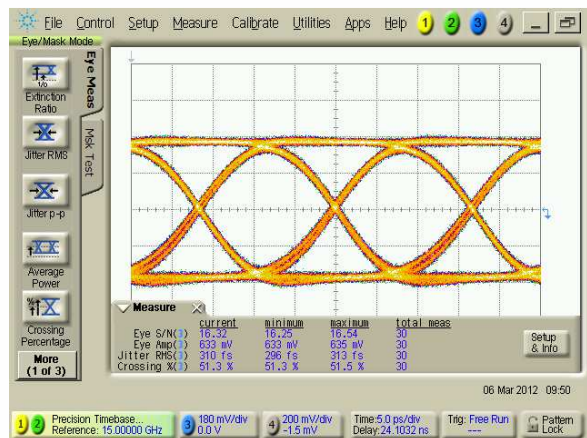
Out @ 64 Gbps



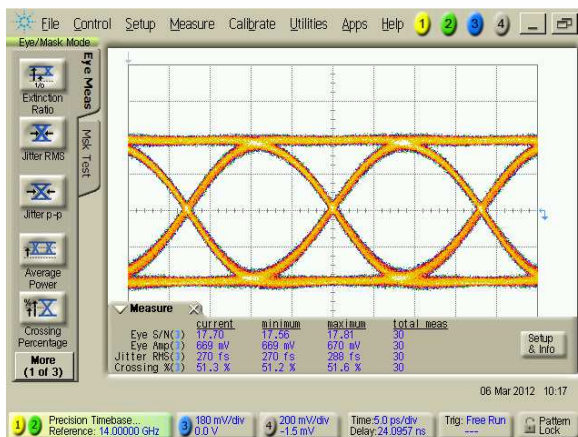
Out inv. @ 64 Gbps



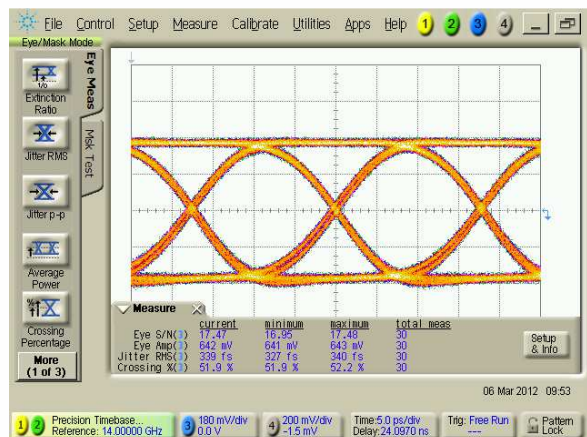
Out @ 60 Gbps



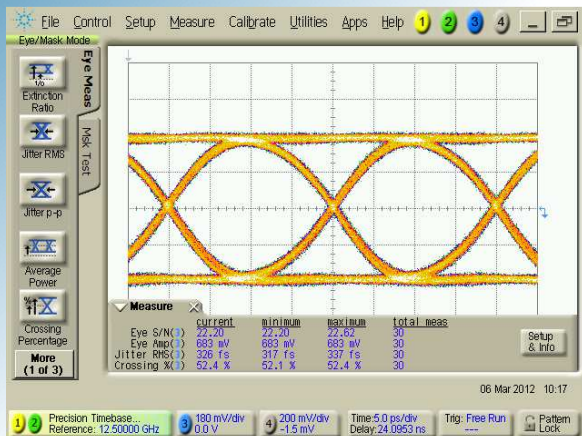
Out inv. @ 60 Gbps



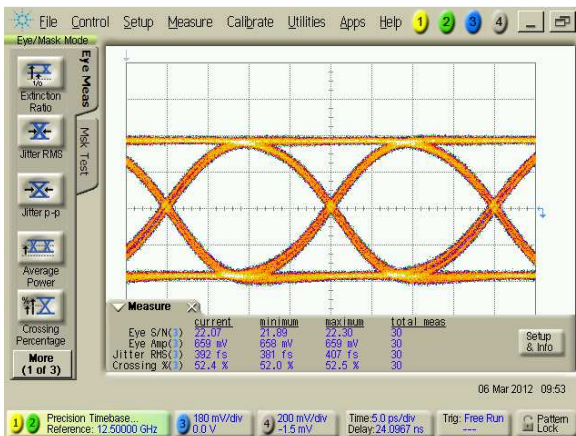
Out @ 56 Gbps



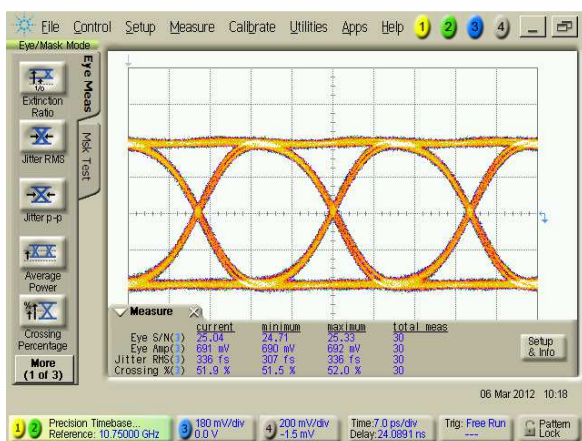
Out inv. @ 56 Gbps



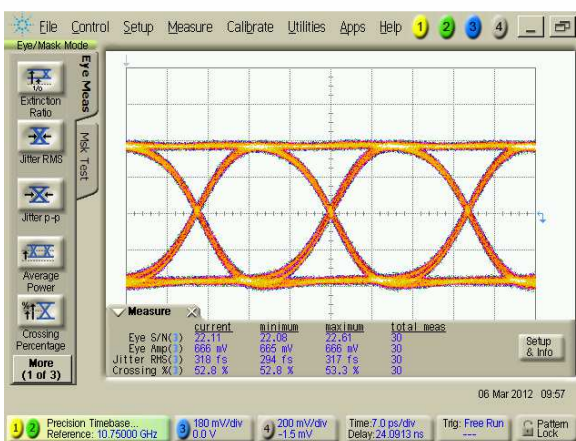
Out @ 50 Gbps



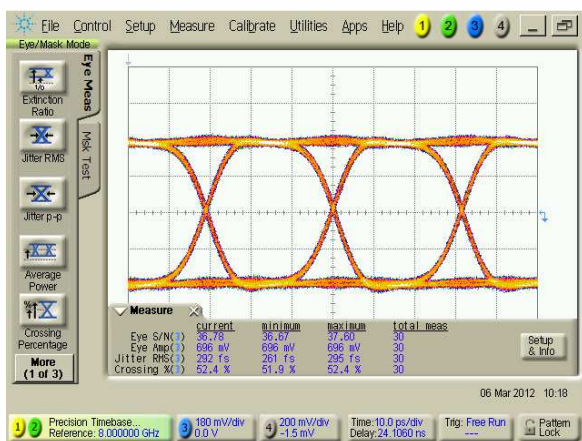
Out inv. @ 50 Gbps



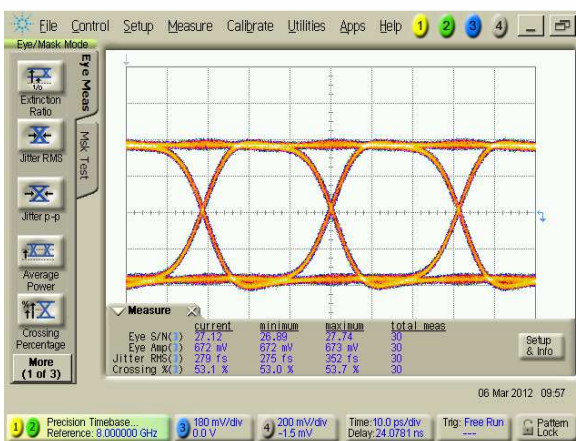
Out @ 43 Gbps



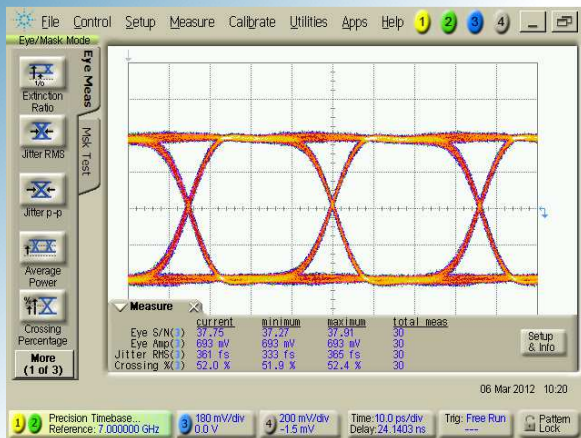
Out inv. @ 43 Gbps



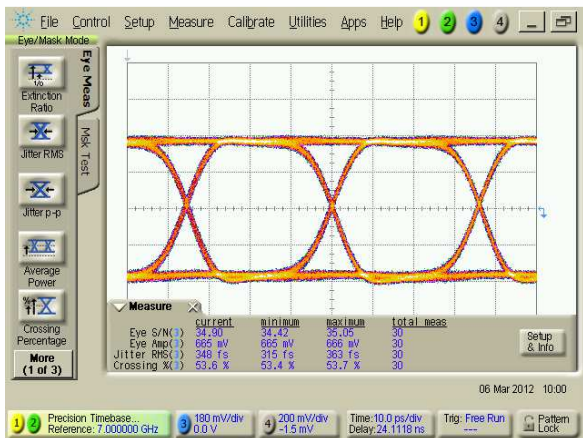
Out @ 32 Gbps



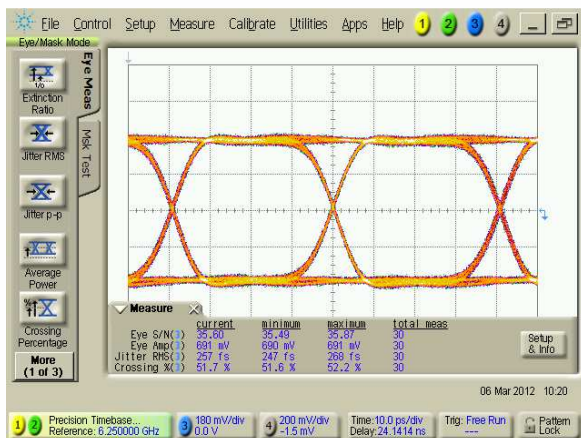
Out inv. @ 32 Gbps



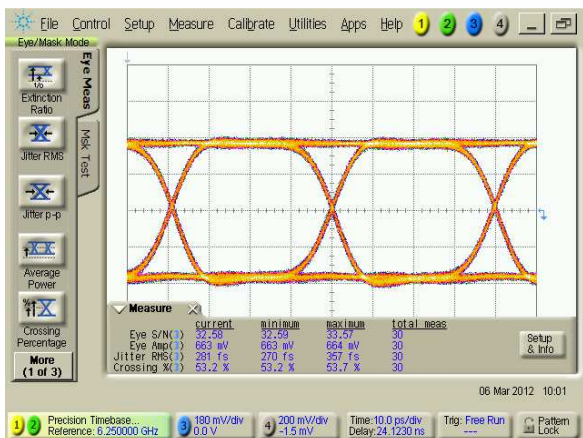
Out @ 28 Gbps



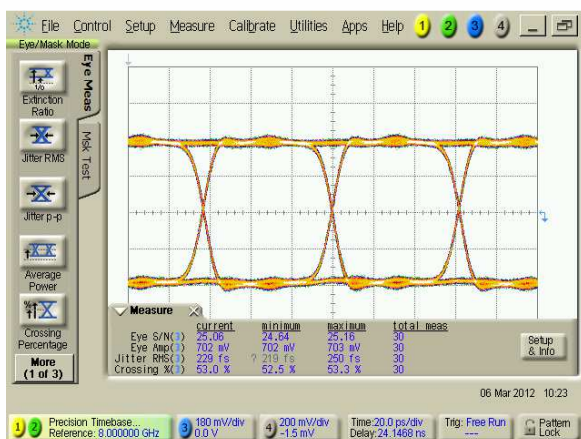
Out inv. @ 28 Gbps



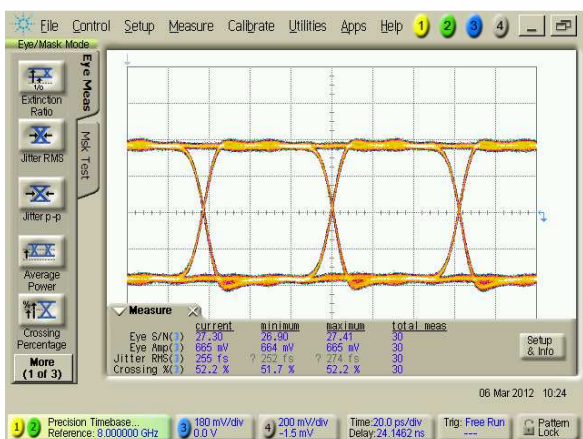
Out @ 25 Gbps



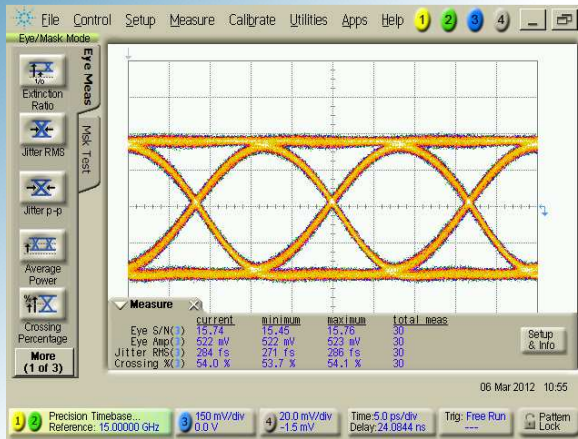
Out inv. @ 25 Gbps



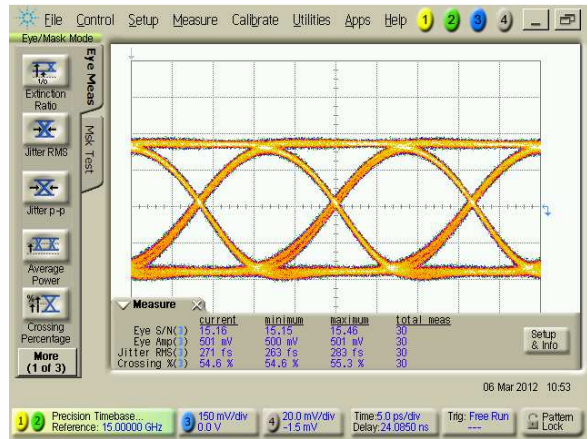
Out @ 16 Gbps



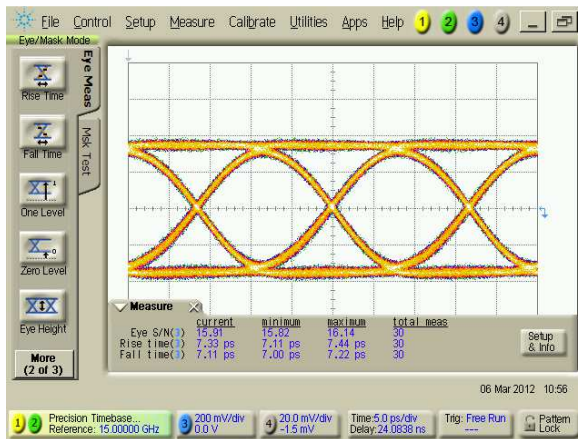
Out inv. @ 16 Gbps



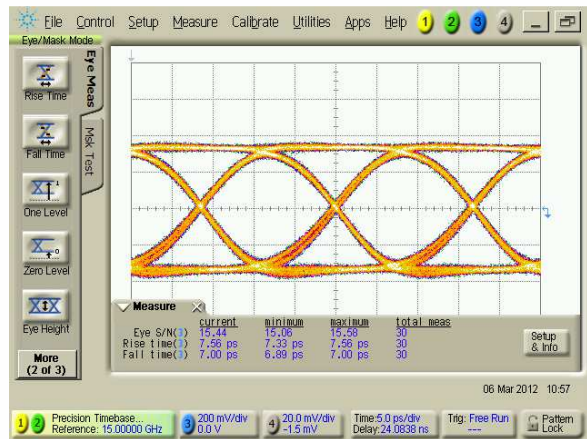
Out @ 60 Gbps, Level = -3dB



Out! @ 60 Gbps, Level = -3dB



Out @ 60 Gbps, t_r/t_f



Out! @ 60 Gbps, t_r/t_f



Outline Drawing

