SH66P58

OTP 6K 4-bit micro-controller with LCD Driver and 16-bit sigma-delta ADC

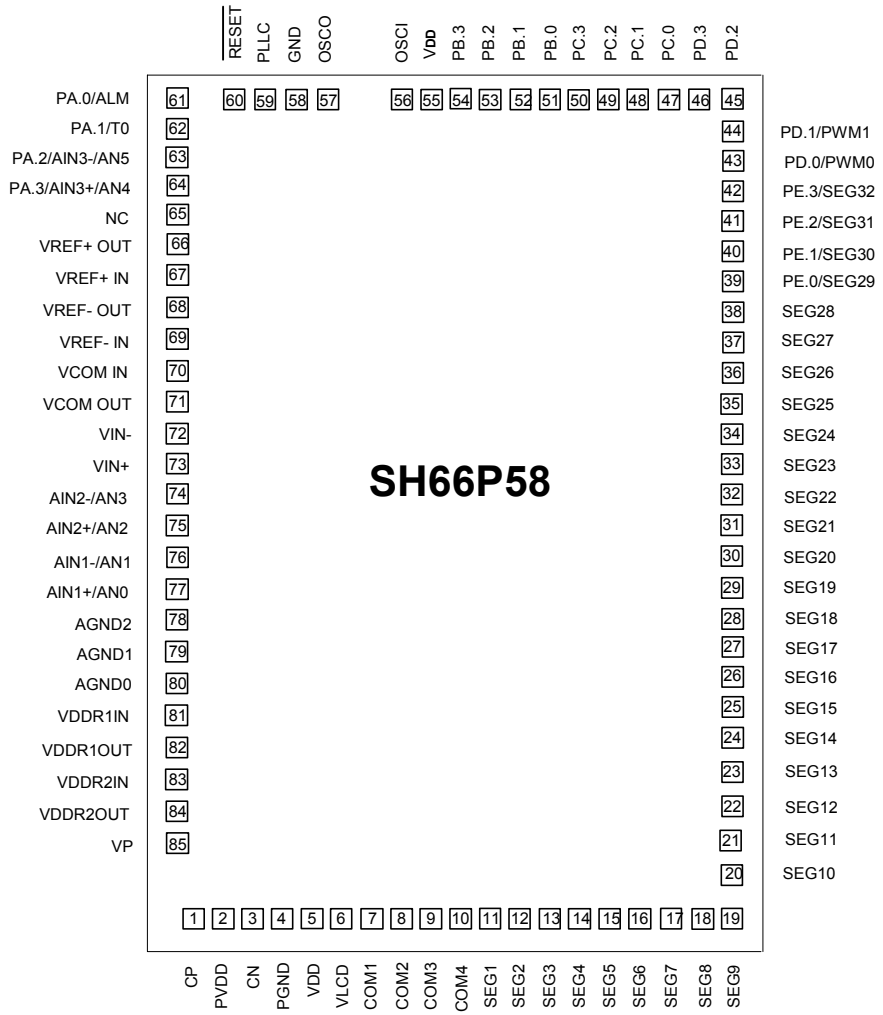
Features

- SH6610D-based Single-chip 4-bit Micro-controller With LCD Driver and 16-bit Sigma-delta ADC
- OTP ROM: 6K X 16 bits
- RAM:
  - 57 System Control Register
  - 464 Data Memory
  - 32 LCD RAM
- Operation Voltage: 2.4V - 5.5V
- 20 CMOS Bi-directional I/O Pins
- Built-in Pull-high Resistor For PORTA - PORTE
- 8-level Stack (Including Interrupts)
- One 8-bit Auto Re-loaded Timer/Counter
- Base Timer
- Warm-up Timer
- Read Rom Data Table Function (RDT)
- Powerful Interrupt Sources:
  - Timer0 Interrupt
  - Base Timer Interrupt
  - A/D Interrupt
  - External Interrupts: Port B (Falling Edge)
- Oscillator: 32.768kHz
- One Built-in PLL Oscillator: 4.2MHz
- Instruction Cycle Time (4/f**osc**)
- LCD Driver:
  - 32 SEG X 4 COM (1/4 Duty, 1/3 Bias)
- 16-bit Resolution, 14-bit Noise Free Sigma-Delta ADC
- Built-in Programmable Gain Instrument Amplifier (PGA)
- Built-in Alarm Generator
- Built-in Charge Pump and Regulator
- 2 Channels 8 bits PWM Output
- Reset
  - Built-in Watchdog Timer (WDT) (Code Option)
  - Built-in Power-on Reset (POR)
  - Built-in Low Voltage Reset (LVR) (Code Option)
- Built-in Low Power Detect (LPD)
- Two Low Power Operation Modes: HALT and STOP
- Available In CHIP FORM

General Description

SH66P58 is a single-chip 4-bit micro-controller. This device integrates a SH6610D CPU core, RAM, ROM, timer, LCD driver, I/O ports, 16-bit sigma-delta ADC, charge pump and regulator, alarm output, PWM, built-in PLL, watchdog timer, low voltage reset and low power detect circuit, The SH66P58 is suitable for high accuracy measurement application.

Pad Configuration



Pad Description

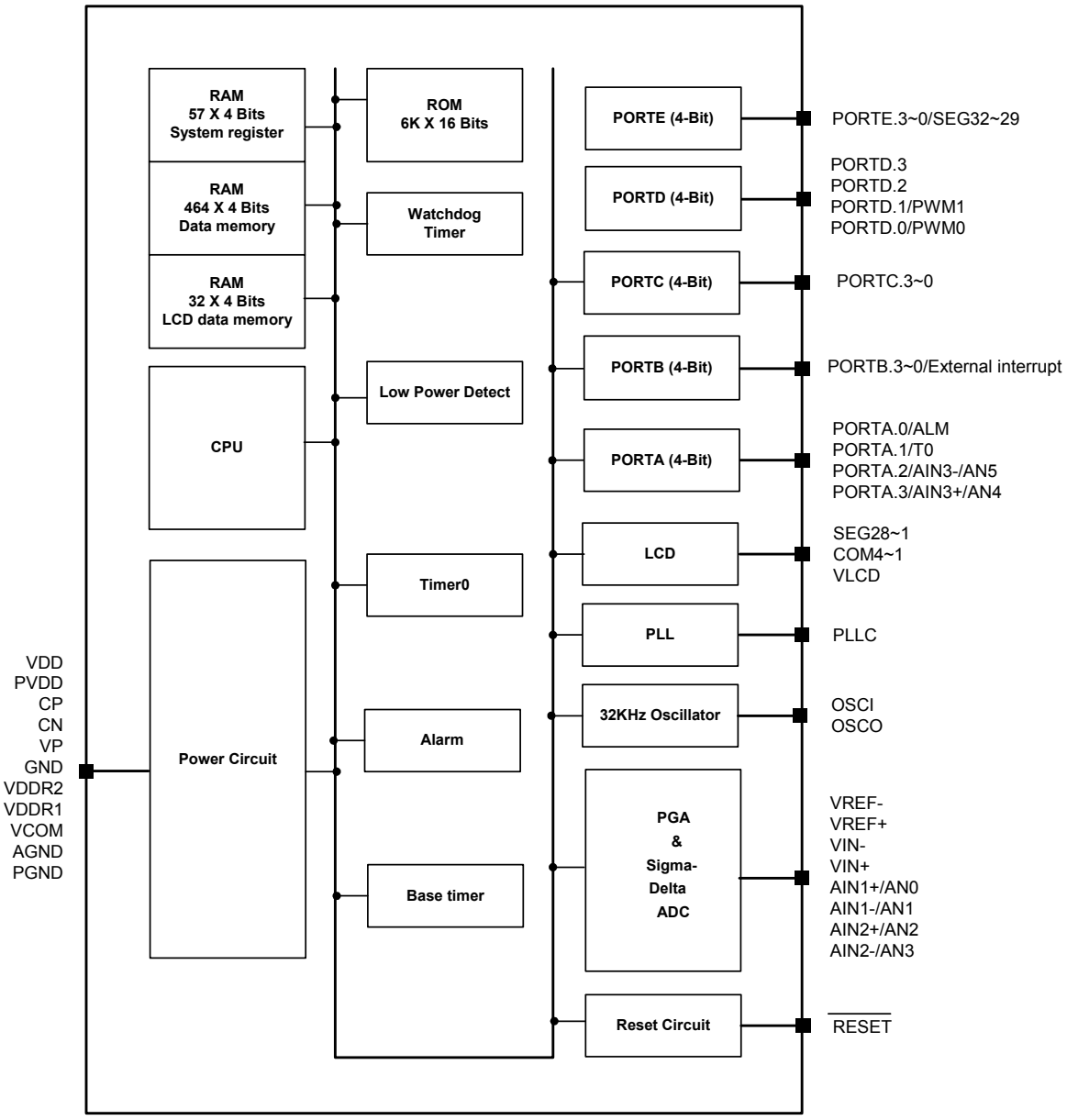
Pad No.	Pad Name	I/O	Descriptions
1	CP	I	Positive capacitor terminal for voltage pump
2	PVDD	P	Voltage pump power supply
3	CN	I	Negative capacitor terminal for voltage pump
4	PGND	P	Pump and regulator ground
5	V_{DD}	P	Digital power supply
6	VLCD	I	LCD power supply input pin
10 - 7	COM4 - 1	O	Common signal output for LCD display
38 - 11	SEG28 - 1	O	Segment signal output for LCD display
39	PE.0 /SEG29	I/O O	Bit programmable bi-directional I/O port Segment signal output for LCD display
40	PE.1 /SEG30	I/O O	Bit programmable bi-directional I/O port Segment signal output for LCD display
41	PE.2 /SEG31	I/O O	Bit programmable bi-directional I/O port Segment signal output for LCD display
42	PE.3 /SEG32	I/O O	Bit programmable bi-directional I/O port Segment signal output for LCD display
43	PD.0 /PWM0	I/O O	Bit programmable bi-directional I/O port PWM0 out
44	PD.1 /PWM1	I/O O	Bit programmable bi-directional I/O port PWM1 out
46 - 45	PD.3 - 2	I/O	Bit programmable bi-directional I/O port
50 - 47	PC.3 - 0	I/O	Bit programmable bi-directional I/O port
54 - 51	PB.3 - 0	I/O	Bit programmable bi-directional I/O port
55	V_{DD}	P	Digital power supply
56	OSCI	I	Oscillator input pin
57	OSCO	O	Oscillator output pin
58	GND	P	Digital power ground
59	PLLC	I	Built-in PLL capacitor connection (a 1000pf capacitor to GND)
60	/RESET	I	Reset pin input (low active)
61	PA.0 /ALM	I/O O	Bit programmable bi-directional I/O port Buzzer output pin
62	PA.1 / T0	I/O I	Bit programmable bi-directional I/O port Timer 0 external clock source input
63	PA.2 /AIN3- /AN5	I/O I I	Bit programmable bi-directional I/O port Negative differential PGA input3 Single ended PGA input5
64	PA.3 /AIN3+ /AN4	I/O I I	Bit programmable bi-directional I/O port Positive differential PGA input3 Single ended PGA input4
65	NC		

Pad Description (continued)

Pad No.	Pad Name	I/O	Descriptions
66	VREF+OUT	O	Positive ADC reference output, must be connected with PAD67
67	VREF+IN	I	Positive ADC reference input, must be connected with PAD66
68	VREF-OUT	O	Negative ADC reference output, must be connected with PAD69
69	VREF-IN	I	Negative ADC reference input, must be connected with PAD68
70	VCOMIN	P	Single Ended amplifier Negative input voltage, must be connected with PAD71
71	VCOMOUT	P	Single Ended amplifier Negative input voltage, must be connected with PAD70
72	VIN-	I	Negative ADC differential input
73	VIN+	I	Positive ADC differential input (a 104 capacitor is need connect between VIN-)
74	AIN2- /AN3	I I	Negative differential PGA input2 Single Ended PGA input3
75	AIN2+ /AN2	I I	Positive differential PGA input2 Single Ended PGA input2
76	AIN1- /AN1	I I	Negative differential PGA input1 Single Ended PGA input1
77	AIN1+ /AN0	I I	Positive differential PGA input1 Single Ended PGA input0
78	AGND2	P	Analog power ground, must be connected with PAD79, PAD80
79	AGND1	P	Analog power ground, must be connected with PAD78, PAD80
80	AGND0	P	Analog power ground, must be connected with PAD78, PAD79
81	VDDR1IN	P	Regulator1 input, must be connected with PAD82
82	VDDR1OUT	P	Regulator1 output, must be connected with PAD81
83	VDDR2IN	P	Regulator2 input, must be connected with PAD84
84	VDDR2OUT	P	Regulator2 output, must be connected with PAD83
85	VP	P	Voltage Pump output

Which, I: input; O: output; P: Power; Z: High impedance

Block Diagram



Functional Description

1. CPU

The CPU contains the following functional blocks: Program Counter (PC), Arithmetic Logic Unit (ALU), Carry Flag (CY), Accumulator, Table Branch Register, Data Pointer (INX, DPH, DPM, and DPL) and Stacks.

1.1. PC

The PC is used for ROM addressing consisting of 12-bits: Page Register (PC11), and Ripple Carry Counter (PC10, PC9, PC8, PC7, PC6, PC5, PC4, PC3, PC2, PC1, PC0).

The program counter is loaded with data corresponding to each instruction. The unconditional jump instruction (JMP) can be set at 1-bit page register for higher than 2K.

The program counter can address only 4K program ROM address. (Refer to the ROM description).

1.2. ALU and CY

The ALU performs arithmetic and logic operations. The ALU provides the following functions:

Binary addition/subtraction (ADC, ADCM, ADD, ADDM, SBC, SBCM, SUB, SUBM, ADI, ADIM, SBI, SBIM)

Decimal adjustments for addition/subtraction (DAA, DAS)

Logic operations (AND, ANDM, EOR, EORM, OR, ORM, ANDIM, EORIM, ORIM)

Decisions (BA0, BA1, BA2, BA3, BAZ, BNZ, BC, BNC)

Logic Shift (SHR)

The Carry Flag (CY) holds the ALU overflow that the arithmetic operation generates. During an interrupt service or call instruction, the carry flag is pushed into the stack and recovered from the stack by the RTNI instruction. It is unaffected by the RTNW instruction.

1.3. Accumulator (AC)

The accumulator is a 4-bit register holding the results of the arithmetic logic unit. In conjunction with the ALU, data is transferred between the accumulator and system register, or data memory can be performed.

1.4. Table Branch Register (TBR)

Table Data can be stored in program memory and can be referenced by using Table Branch (TJMP) and Return Constant (RTNW) instructions. The Table Branch Register (TBR) and Accumulator (AC) are placed by an offset address in program ROM. TJMP instruction branch into address ((PC11 - PC8) X (2^8) + (TBR, AC)). The address is determined by RTNW to return look-up value into (TBR, AC). ROM code bit7-bit4 is placed into TBR and bit3-bit0 into AC.

1.5. Data Pointer

The Data Pointer can indirectly address data memory. Pointer address is located in register DPH (3-bit), DPM (3-bit) and DPL (4-bit). The addressing range is 000H - 3FFH. Pseudo index address (INX) is used to read or write Data memory, then RAM address Bit9 - 0 comes from DPH, DPM and DPL.

1.6. Stack

The stack is a group of registers used to save the contents of CY & PC (11-0) sequentially with each subroutine call or interrupt. The MSB is saved for CY and it is organized into 13 bits X 8 levels. The stack is operated on a first-in, last-out basis and returned sequentially to the PC with the return instructions (RTNI/RTNW).

Note:

The stack nesting includes both subroutine calls and interrupts requests. The maximum allowed for subroutine calls and interrupts are 8 levels. If the number of calls and interrupt requests exceeds 8, then the bottom of stack will be shifted out, that program execution may enter an abnormal state.

2. RAM

Built-in RAM contains general-purpose data memory and system register. Because of its static nature, the RAM can keep data after the CPU entering STOP or HALT.

2.1. RAM Addressing

Data memory and system register can be accessed in one instruction by direct addressing. The following is the memory allocation map:

System register: $000 - $02 F (exclude $01D), $320 - $329
Data memory: $030 - $1FF
LCD RAM space: $300 - $31F

RAM Bank Table:

Bank 0 B = 0	**Bank 1** B = 1	**Bank 2** B = 2	**Bank 3** B = 3	**Bank 4** B = 4	**Bank 5** B = 5	**Bank 6** B = 6	**Bank 7** B = 7
$020 - $07F	$080 - $0FF	$100 - $17F	$180 - $1FF	$200 - $27F	$280 - $2FF	$300 - $37F	$380 - $3FF

Where, B: RAM bank bit use in instructions

2.2. Configuration of System Register

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEADC	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQADC	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register
$02	-	T0S	T0M.1	T0M.0	R/W	Timer0 Mode register
$03	T0L.3	T0L.2	T0L.1	T0L.0	R/W	Timer0 load/counter low nibble register
$04	T0H.3	T0H.2	T0H.1	T0H.0	R/W	Timer0 load/counter high nibble register
$05	BTM1	BTM0	BTEN	-	R/W	Bit1: Base Timer control bit Bit2 - 3:BaseTimer overflow frequency setup
$06	FCT	FSTEN	RLCD0	-	R/W	LCD control register
$07	LCDON	O/S2	O/S1	O/S0	R/W	Bit2-0: LCD port share control register Bit3: LCD enable control bit
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$0D	PULLEN	ALMF1	ALMF0	ALMEN	R/W	Bit0: ALM control register Bit2-1: ALM output carrier frequency Bit3: Port pull-high control
$0E	TBR.3	TBR.2	TBR.1	TBR.0	R/W	Table Branch register
$0F	INX.3	INX.2	INX.1	INX.0	R/W	Pseudo index register
$10	DPL.3	DPL.2	DPL.1	DPL.0	R/W	Data pointer for INX low nibble register
$11	-	DPM.2	DPM.1	DPM.0	R/W	Data pointer for INX middle nibble register
$12	-	DPH.2	DPH.1	DPH.0	R/W	Data pointer for INX high nibble register
$13	FS1	FS0	OXS	PLLON	R/W	Oscillator control register
$14	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$15	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$16	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$17	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register
$1D	-	-	-	-	-	Reserved
$1E	WDTF	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
$1F	-	-	-	BNK0	R/W	Bit0: Bank register for ROM

Configuration of System Register (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	ADCEN	-	REFS1	REFS0	R/W	Bit1-0: ADC reference selection bits Bit3: ADC Enable/Disable control bit.
$21	PGAEN	GAIN2	GAIN1	GAIN0	R/W	Bit2-0: PGA gain selection bits Bit3: PGA Enable/Disable control bit.
$22	-	CHOPEN	CHOPCLK1	CHOPCLK0	R/W	Bit1-0: PGA chopper work clock selection bits Bit2: PGA chopper Enable/Disable control bit.
$23	CHS3	CHS2	CHS1	CHS0	R/W	Bit0-3: PGA&ADC channel select
$24	TADC3	TADC2	TADC1	TADC0	R/W	ADC clock select low nibble register
$25	TADC7	TADC6	TADC5	TADC4	R/W	ADC clock select high nibble register
$26	-	-	AN5S	AN4S	R/W	Bit1-0: ADC port share control register
$27	D3	D2	D1	D0	R	ADC data register0
$28	D7	D6	D5	D4	R	ADC data register1
$29	D11	D10	D9	D8	R	ADC data register2
$2A	D15	D14	D13	D12	R	ADC data register3
$2B	LPDEN	LPDF	LPDS1	LPDS0	R/W R	Bit3: Low Power Detect Enable control bit Bit2: Low Power Detect Flag Bit1 - 0: Power voltage point select
$2C	PMOD	PCLK	PAUTOEN	PEN	R/W	Bit0: Pump control bit Bit2-1: Pump clock select bits
$2D	-	R2S	REN2	REN1	R/W	Bit0: Regulator1 control bit. Bit2-1: Regulator2 control bits
$2E	PIEN.3	PIEN.2	PIEN.1	PIEN.0	R/W	PORTB interrupt enable flags register
$2F	PIF.3	PIF.2	PIF.1	PIF.0	R/W	PORTB interrupt request flags register
$320	PWM0S	T0CK1	T0CK0	PWM0_EN	R/W	Bit0: PWM0 output enable Bit2, Bit1: Select PWM0 clock Bit3: Set PWM0 output mode of duty cycle
$321	PWM1S	T1CK1	T1CK0	PWM1_EN	R/W	Bit0: PWM1 output enable Bit2, Bit1: Select PWM1 clock Bit3: Set PWM1 output mode of duty cycle
$322	PP0.3	PP0.2	PP0.1	PP0.0	R/W	PWM0 period low nibble
$323	PP0.7	PP0.6	PP0.5	PP0.4	R/W	PWM0 period high nibble
$324	PD0.3	PD0.2	PD0.1	PD0.0	R/W	PWM0 duty low nibble
$325	PD0.7	PD0.6	PD0.5	PD0.4	R/W	PWM0 duty high nibble
$326	PP1.3	PP1.2	PP1.1	PP1.0	R/W	PWM1 period low nibble
$327	PP1.7	PP1.6	PP1.5	PP1.4	R/W	PWM1 period high nibble
$328	PD1.3	PD1.2	PD1.1	PD1.0	R/W	PWM1 duty low nibble
$329	PD1.7	PD1.6	PD1.5	PD1.4	R/W	PWM1 duty high nibble

3. ROM

The ROM can address 6144 X 16 bits of program area from $000 to $17FF.

3.1. Vector Address Area ($000 to $004)

The program is sequentially executed. There is an area address $000 through $004 that is reserved for a special interrupt service routine such as starting vector address.

Address	Instruction	Remarks
000H	JMP xxxx *	Jump to RESET service routine
001H	JMP xxxx *	Jump to A/D interrupt service routine
002H	JMP xxxx *	Jump to Timer0 interrupt service routine
003H	JMP xxxx *	Jump to Base Timer interrupt service routine
004H	JMP xxxx *	Jump to Port interrupt service routine

*JMP instruction can be replaced by any instruction.

3.2. Bank Switch Mapping

Program Counter (PC11 - PC0) can only address 4K ROM Space. The Bank switch technique is used to extend the CPU address space. The lower 2K of the CPU addressing space maps to the lower 2K of ROM space (BANK.0). The upper 2K of the CPU addressing space maps to one of the two banks (BNK.0 = $00 - $01) of the upper 4K of ROM.

The bank switch mapping is as follows:

CPU Address	ROM Space	
	BNK = $00	BNK = $01
Lower 2K address	$0000 - $07FF (BANK 0)	$0000 - $07FF (BANK 0)
Upper 2K address	$0800 - $0FFF (BANK 1)	$1000 - $17FF (BANK 2)

4. Initial State

4.1. System Register State

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset /Pin Reset /Low Voltage Reset	WDT Reset
$00	IEADC	IET0	IEBT	IEP	0000	0000
$01	IRQADC	IRQT0	IRQBT	IRQP	0000	0000
$02	-	T0S	T0M.1	T0M.0	0000	-uuu
$03	T0L.3	T0L.2	T0L.1	T0L.0	xxxx	uuuu
$04	T0H.3	T0H.2	T0H.1	T0H.0	xxxx	uuuu
$05	BTM1	BTM0	BTEN	-	000-	uuu-
$06	FCT	FSTEN	RLCD0	-	000-	000-
$07	LCDON	O/S2	O/S1	O/S0	0000	0000
$08	PA.3	PA.2	PA.1	PA.0	0000	0000
$09	PB.3	PB.2	PB.1	PB.0	0000	0000
$0A	PC.3	PC.2	PC.1	PC.0	0000	0000
$0B	PD.3	PD.2	PD.1	PD.0	0000	0000
$0C	PE3	PE.2	PE.1	PE.0	0000	0000
$0D	PULLEN	ALRMF1	ALRMF0	ALRMEN	0000	0000
$0E	TBR.3	TBR.2	TBR.1	TBR.0	xxxx	uuuu
$0F	INX.3	INX.2	INX.1	INX.0	xxxx	uuuu
$10	DPL.3	DPL.2	DPL.1	DPL.0	xxxx	uuuu
$11	-	DPM.2	DPM.1	DPM.0	-xxx	-uuu
$12	-	DPH.2	DPH.1	DPH.0	-xxx	-uuu
$13	FS1	FS0	OXS	PLLON	0000	0000
$14	RDT.3	RDT.2	RDT.1	RDT.0	xxxx	uuuu
$15	RDT.7	RDT.6	RDT.5	RDT.4	xxxx	uuuu
$16	RDT.11	RDT.10	RDT.9	RDT.8	xxxx	uuuu
$17	RDT.15	RDT.14	RDT.13	RDT.12	xxxx	uuuu
$18	PACR.3	PACR.2	PACR.1	PACR.0	0000	0000
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	0000	0000
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	0000	0000
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	0000	0000
$1C	PECR.3	PECR.2	PECR.1	PECR.0	0000	0000
$1D	-	-	-	-	xxxx	uuuu
$1E	WDTF	WDT.2	WDT.1	WDT.0	0000	1000
$1F	-	-	-	BNK0	---0	---0

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

System Register State: (continued)

Address	Bit 3	Bit 2	Bit 1	Bit 0	Power-on Reset /Pin Reset /Low Voltage Reset	WDT Reset
$20	ADCEN	-	REFS1	REFS0	0-00	0-00
$21	PGAEN	GAIN2	GAIN1	GAIN0	0000	0000
$22	-	CHOPEN	CHOPCLK1	CHOPCLK0	-000	-000
$23	CHS3	CHS2	CHS1	CHS0	0000	0000
$24	TADC3	TADC2	TADC1	TADC0	0000	0000
$25	TADC7	TADC6	TADC5	TADC4	0000	0000
$26	-	-	AN5S	AN4S	--00	--00
$27	D3	D2	D1	D0	0000	0000
$28	D7	D6	D5	D4	0000	0000
$29	D11	D10	D9	D8	0000	0000
$2A	D15	D14	D13	D12	0000	0000
$2B	LPDEN	LPDF	LPDS1	LPDS0	0000	0000
$2C	PMOD	PCLK	PAUTOEN	PEN	0000	0000
$2D	-	R2S	REN2	REN1	-000	-000
$2E	PIEN.3	PIEN.2	PIEN.1	PIEN.0	0000	0000
$2F	PIF.3	PIF.2	PIF.1	PIF.0	0000	0000
$320	PWM0S	T0CK1	T0CK0	PWM0_EN	0000	uuu0
$321	PWM1S	T1CK1	T1CK0	PWM1_EN	0000	uuu0
$322	PP0.3	PP0.2	PP0.1	PP0.0	xxxx	uuuu
$323	PP0.7	PP0.6	PP0.5	PP0.4	xxxx	uuuu
$324	PD0.3	PD0.2	PD0.1	PD0.0	xxxx	uuuu
$325	PD0.7	PD0.6	PD0.5	PD0.4	xxxx	uuuu
$326	PP1.3	PP1.2	PP1.1	PP1.0	xxxx	uuuu
$327	PP1.7	PP1.6	PP1.5	PP1.4	xxxx	uuuu
$328	PD1.3	PD1.2	PD1.1	PD1.0	xxxx	uuuu
$329	PD1.7	PD1.6	PD1.5	PD1.4	xxxx	uuuu

Legend: x = unknown, u = unchanged, - = unimplemented read as “0”.

4.2. Others Initial States

Others	After any Reset
Program Counter (PC)	$000
CY	Undefined
Accumulator (AC)	Undefined
Data Memory	Undefined

5. System Clock and Oscillator

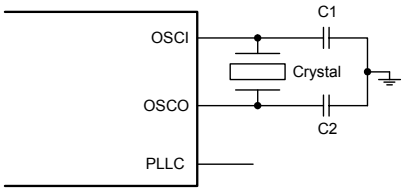
The oscillator generates the basic clock pulses that provide the system clock to supply CPU and on-chip peripherals.
System clock $f_{SYS} = f_{OSC}/4$

5.1. Instruction Cycle Time

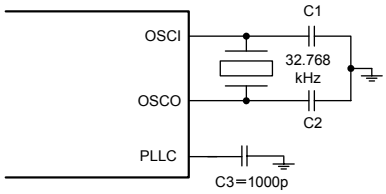
(1) 4/32.768kHz (≈ 122μs) for 32.768kHz oscillator.
(2) 4/4.2MHz (≈ 1μs) for PLL 4.2MHz oscillator.

5.2. Oscillator Type

(1) Crystal oscillator: 32.768kHz



(2) PLL oscillator: 4.2MHz



5.3. Control of Oscillator

Oscillator Control Register: $13

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$13	FS1	FS0	OXS	PLLON	R/W	Bit0: Turn on/off PLL Bit1: Clock source select (1: PLL, 0: 32.768kHz) Bit3 - 2: PLL Frequency select
	X	X	0	0	R/W	Turn off PLL, Clock source select 32kHz
	X	X	0	1	R/W	Turn on PLL, But clock source select 32kHz
	X	X	1	0	R/W	Invalid setup
	0	0	1	1	R/W	PLL provides 4.2MHz clock for clock source
	0	1	1	1	R/W	PLL provides 2.1MHz clock for clock source
	1	0	1	1	R/W	PLL provides 1.05MHz clock for clock source
	1	1	1	1	R/W	PLL provides 524kHz clock for clock source

Note 1:

Set PLL as system clock source:
1. Configure the FS1 and FS0 in oscillator control register.
2. Set PLLON = 1, turn on the PLL.
3. Wait at least 2ms.
4. Set OXS = 1, select PLL as the system clock source.

Note 2:

It is possible to select the high speed CPU processing by PLL clock and select low power operation by 32.768kHz clock. At starting of reset initialization, 32.768kHz clock starts oscillation. Immediately after reset initialization, the 32.768kHz clock is automatically selected as the system clock source.

5.4. Capacitor Selection for Oscillator

Crystal Oscillator			Recommend Type	Manufacturer
Frequency	C1	C2		
32.768kHz	5 - 12.5pF	5 - 12.5pF	DT 38 (ϕ 3x8)	KDS

Note:

1. Capacitor values are used for design guidance only!
2. These capacitors were tested with the crystals listed above for basic start-up and operation. They are not optimized.
3. Be careful for the stray capacitance on PCB board, the user should test the performance of the oscillator over the expected V_{DD} and the temperature range for the application.

Before selecting crystal/ceramic, the user should consult the crystal/ceramic manufacturer for appropriate value of external component to get best performance, visit http://www.sinowealth.com for more recommended manufactures

6. I/O Port

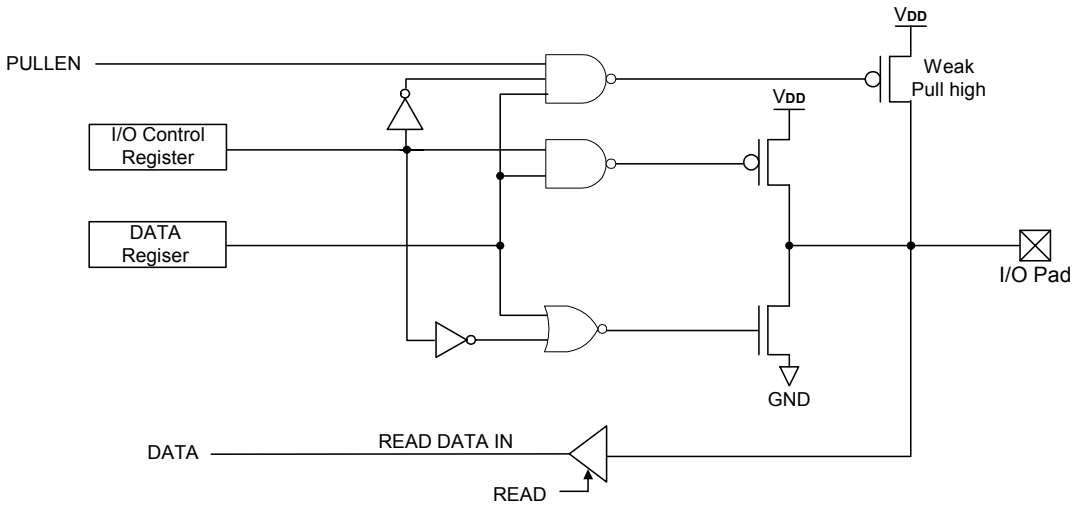
The SH66P58 provides 20 bi-directional I/O ports. The PORT data put in register $08 - $0C. The PORT control register ($18 - $1C) controls the PORT as input or output. Each I/O port has an internal pull-high resistor; Pull-high function is controlled by PULLEN of $0D and the data of the port, when the PORT is used as input.

I/O Register: $08 - $0C, $18 - $1C

Address	Bit3	Bit2	Bit1	Bit0	R/W	Remarks
$08	PA.3	PA.2	PA.1	PA.0	R/W	PORTA data register
$09	PB.3	PB.2	PB.1	PB.0	R/W	PORTB data register
$0A	PC.3	PC.2	PC.1	PC.0	R/W	PORTC data register
$0B	PD.3	PD.2	PD.1	PD.0	R/W	PORTD data register
$0C	PE.3	PE.2	PE.1	PE.0	R/W	PORTE data register
$18	PACR.3	PACR.2	PACR.1	PACR.0	R/W	PORTA input/output control register
$19	PBCR.3	PBCR.2	PBCR.1	PBCR.0	R/W	PORTB input/output control register
$1A	PCCR.3	PCCR.2	PCCR.1	PCCR.0	R/W	PORTC input/output control register
$1B	PDCR.3	PDCR.2	PDCR.1	PDCR.0	R/W	PORTD input/output control register
$1C	PECR.3	PECR.2	PECR.1	PECR.0	R/W	PORTE input/output control register

PA (/B/C/D/E) CR.x, (x = 0, 1, 2, 3)
0: Set I/O as an input state. (Power on initial)
1: Set I/O as an output state.

Equivalent Circuit for a Single I/O Pin



System Register: $0D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	PULLEN	ALMF1	ALMF0	ALMEN	R/W	Bit0: ALM control register Bit2-1: ALM output carrier frequency Bit3: Port pull-high control
	0	x	x	x	R/W	Ports pull-high disable
	1	x	x	x	R/W	Ports pull-high enable

Note:

1. To turn on the pull-high resistor, user must set I/O as an input state, and set PULLEN to “1”, and write “1” to the port data register.
2. User had better not use “ANDIM, ORIM, EORIM” instruction to operate these I/O Ports, because this can change I/O data register to “0” and cause pull-up resistor to be turned off.

Port Interrupt

The PORTB is used as port interrupt sources. Since PORTB I/O is bit programmable I/O, only when the PORTB is selected as normal I/O input, the voltage transition from V**DD** to GND applying to the digital input port can generate a port interrupt.

The PORTB interrupt control flags are mapped on $2E, $2F of the system register. They can be accessed or tested by the read/write operation. Those flags are clear to “0” at initialization by the chip reset.

Port Interrupts can be used to wake up the CPU from the HALT or the STOP mode.

System Register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	PIEN.3	PIEN.2	PIEN.1	PIEN.0	R/W	PORTB interrupt enable control register

PIEN.x (x = 0, 1, 2, 3)
0: Disable PB.x port interrupt. (Power on initial)
1: Enable PB.x port interrupt.

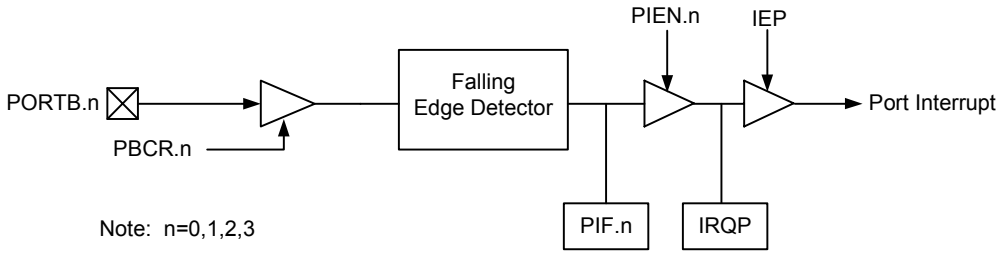
System Register: $2F

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2F	PIF.3	PIF.2	PIF.1	PIF.0	R/W	PORTB interrupt request flags register

PIF.x (x = 0, 1, 2, 3)
0: PB.x port interrupt is not presented. (Power on initial)
1: PB.x port interrupt is presented.

Only writing these bits to “0” is available.

Following is the port interrupt function block-diagram for reference.



Port Interrupt Programming Notes:

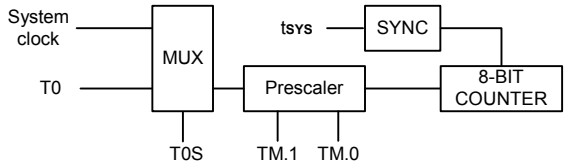
Any one of PORTB input pin transitions from V**DD** to GND would set PIF.x to “1”, in spite of level of the other PORTB pin.

If PIEN.x = 1and IEPB = 1, the x of PORTB input pin transitions from V**DD** to GND would generate an interrupt request (IRQP = 1) and interrupt the CPU, in spite of any level of the other pin of PORTB.

7. Timer0

The timer/counter has the following features:
- 8-bit up-counting timer/counter
- Automatic re-load counter
- 4-level prescaler
- Interrupt on overflow from $FF to $00

The following is a simplified Timer 0 block diagram.



The timer provide the following functions:
- Programmable interval timer function.
- Read counter value.

7.1. Timer0 Configuration and Operation

Timer0 consists of an 8-bit write-only timer load register (TL0L, TL0H) and an 8-bit read-only timer counter (TC0L, TC0H). Each of them has both low-order digits and high-order digits. Writing data into the timer load register (TL0L, TL0H) can initialize the timer counter.

The low-order digit should be written first, and then the high-order digit. The timer counter is automatically loaded with the contents of the load register when the high-order digit is written or the counter counts overflow from $FF to $00.

Timer Load Register: Since the register H controls the physical READ and WRITE operations.

Please follow these steps:

Write Operation:

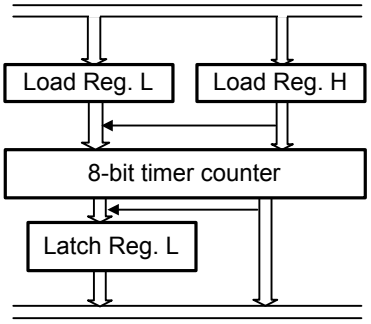
Low nibble first

High nibble to update the counter

Read Operation:

High Nibble first

Low nibble followed



7.2. Timer0 Mode Register

The Timer0 can be programmed in several different prescalers by setting Timer0 mode register (T0M). The clock source pre-scale by the 8-level counter first, then generate the output plus to timer counter. The Timer0 mode register (T0M) is 4-bit register used for the Timer0 control as shown in the following table.

Timer0 Mode Register: $02

T0M.1	T0M.0	Prescaler Divide Ratio	Clock Source
0	0	$/2^6$	System clock/T0
0	1	$/2^4$	System clock/T0
1	0	$/2^2$	System clock/T0
1	1	$/2^0$	System clock/T0

Also the clock source of Timer0 is set in timer control registers, as shown as follows.

Systems Register: $02

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$02		T0S	T0M.1	T0M.0	R/W	Bit2: T0 signal source select register
		0	X	X	R/W	Timer0 source is system clock
		1	X	X	R/W	Timer0 source is T0 input clock

7.3. External Clock/Event T0 as Timer0 Source

When external clock/event T0 input as Timer 0 clock source, it is synchronized with the CPU system clock. The external source must follow certain constraints. The system clock samples it in instruction frame cycle. Therefore it is necessary to be high (at least 2 t**osc**) and low (at least 2 t**osc**).

When the prescaler ratio selects $/2^0$, it is the same as the system clock input.

The requirement is as follows:

T0H (T0 high time) $\geq$ 2 * tosc + ΔT

T0L (T0 low time) $\geq$ 2 * tosc + ΔT ; ΔT = 20ns

When another clock rate is selected, the T0M is scaled by the asynchronous ripple counter and so the prescaler output is symmetrical. Then:

$$T0\ \text{high time} = T0\ \text{low time} = \frac{N * T0}{2}$$

Where: T0 = Timer0 input period
N = clock rate value

The requirement is:

$$\frac{N * T0}{2} \geq 2 * \text{tosc} + \Delta T \quad \text{or} \quad T0 \geq \frac{4 * \text{tosc} + 2 * \Delta T}{N}$$

So, the limitation is applied for the T0 period time only. The pulse width is not limited by this equation. It is summarized as follows:

$$T0 = \text{Timer0 period} \geq \frac{4 * \text{tosc} + 2 * \Delta T}{N}$$

8. Base Timer

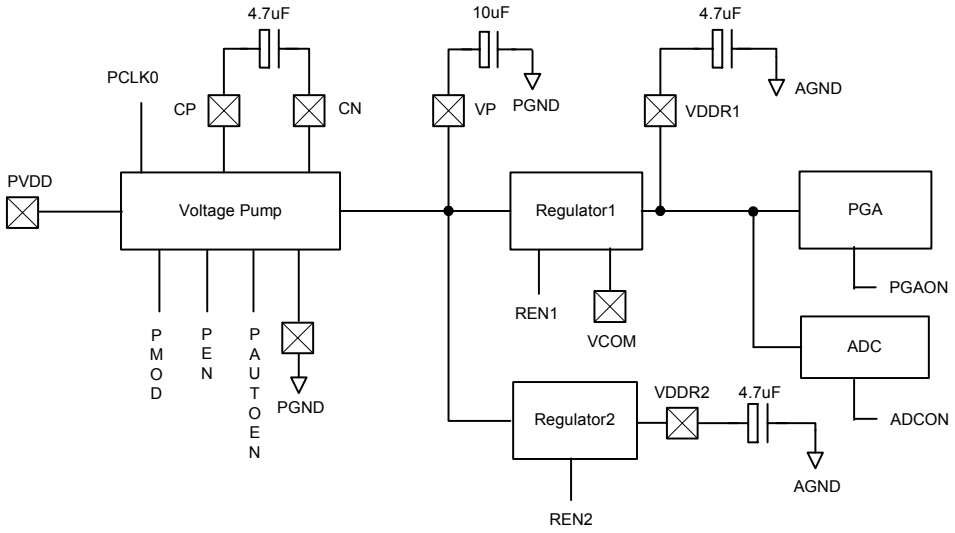
SH66P58 has a base timer, and it generates the different frequency interrupt for real time clock based on the value of BTM.

Base Time Control Register: $05

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$05	BTM1	BTM0	BTEN	-	R/W	Bit1: Base Timer control bit Bit2 - 3: Base Timer overflow frequency setup
	X	X	0	-	R/W	Disable base timer
	0	0	1	-	R/W	Enable base timer, overflow every 2Hz
	0	1	1	-	R/W	Enable base timer, overflow every 8Hz
	1	0	1	-	R/W	Enable base timer, overflow every 32Hz
	1	1	1	-	R/W	Enable base timer, overflow every 128Hz

9. Power Supply System

9.1. Power Supply Block Diagram



9.2. Register

PUMP Control Register: $2C

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2C	PMOD	PCLK0	PAUTOEN	PEN	R/W	Bit0: Pump control bit Bit2-1: Pump clock select bits
	X	X	X	0	R/W	Pump is always Disable, VP = PVDD
	X	X	0	1	R/W	Pump is always enable, VP = 2PVDD
	X	X	1	1	R/W	Pump is in auto mode if PVDD ≥ 3.6V, Pump is always disable, VP = PVDD If 3.6 > PVDD ≥ 2.75, Pump is on/off intermittently. VP = 5.5V If PVDD < 2.75, Pump is always enable. VP = 2PVDD
	X	0	X	X	R/W	Pump Clock = 2048Hz
	X	1	X	X	R/W	Pump Clock = 16384Hz
	0	X	X	X	R/W	Pump is in normal mode
	1	X	X	X	R/W	Pump is in low circuit consuming mode

Regulator1 and Regulator2 are all output 3.0V or 1.5V, Regulator1 provide PGA and ADC power, and if LCD needs a stable display, which is not effected by ripple of VDD, you should connect VLCD to VDDR1. VDDR2 provided a stable voltage for outside sensor, it can be disable separately to save power consuming,

If V_{DD} > 3.6V, PEN shouldn't be set to 1 because 3.6V is higher enough to provided power for regulator. If charge Pump is enabled, all current consumption from VDDR1 and VDDR2 will be doubled.

If pump have no heavy load, it could be setup as a low circuit-consuming mode. For example, regulator2 disable, sensor needn't power supply. At the same time, regulator1 enable but PGA and ADC are disabling, VLCD connect to VDDR1, Regulator1 only provide power for LCD.

Regulator Control Register: $2D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2D	-	R2S	REN2	REN1	R/W	Bit0: Regulator1 control bit. Bit2-1: Regulator2 control bits
	-	X	X	0	R/W	Regulator1 Disable. VDDR1 = 0, PGA, ADC no power supply
	-	X	X	1	R/W	Regulator1 Enable. VDDR1 = 3.0V
	-	X	0	X	R/W	Regulator2 Disable, VDDR2 = 0, no power output for sensor
	-	0	1	X	R/W	Regulator2 Enable, VDDR2 = 3.0V, Output for sensor power
	-	1	1	X	R/W	Regulator2 Enable, VDDR2 = 1.5V, Output for sensor power

Note:

1. If regulator and charge pump are all need to be enable, REN1 or REN2 must be set after PEN about 10ms, Because regulator power source is from charge Pump, if charge Pump haven't been stable, and then REN is set, maybe charge Pump can't be setup up successfully.
2. If charge Pump is Enabled, all current consumption from VDDR1 And VDDR2 will be doubled.
3. CPU went into halt or stop mode will have no effect with PUMP or regulator, so, if you want cpu get into halt/stop mode to save power consuming, pump and regulator should be disable by software. After wake up, charge pump and regulator should be enable refer to Note 1 by software.

If VLCD connect to VDDR1 (recommend)

PMOD	PAUTOEN	PEN	REN1	REN2	VP	VDDR1	VDDR2	Use Condition Description
0	0	0	0		V_{DD}	0		All disable
0	0	0	1		V_{DD}	3.0V		V_{DD} >= 3.6V (PGA & ADC & LCD on)
0	0	1	1		$2V_{DD}$	3.0V		V_{DD} < 3.6V (PGA & ADC & LCD on)
1	0	1	1	0	$2V_{DD}$	3.0V	0	LCD on, PGA & ADC off
0	1	1	1		See note*	3.0V		Could be used in all condition

Note*:

In auto mode:

If PVDD ≥ 3.6V, Pump is always disable, VP = PVDD.
If 3.6 > PVDD ≥ 2.75, Pump is on/off intermittently. VP = 5.5V.
If PVDD < 2.75, Pump is always enable. VP = 2PVDD.

10. Analog Digital Converter (ADC)

The Σ-Δ ADC with 16-bit resolution is integrated in this micro-controller. The analog input will be amplified by the PGA (Programmable Gain Instrumentation Amplifier) before being input to ADC module. There are three kinds of analog input, differential input, single-ended input and short input. Six external ADC channels are differential input. They also could be configured as single-ended input. Short input, which is used in offset detect.

The approach for ADC conversion:
- Set REFS1 - 0 of Register ADCON to select ADC reference voltage.
- Set SCH [3:0] of Register CHSCON to select ADC channel.
- Set GAIN [2:0] of Register PGACON to select PGA gain.
- Set Register TADC to choose ADC clock.
- Set Register CHOPCON to enable chop and choose chop clock.
- Set ADCEN to start ADC conversion.
- IRQADC will be set when one ADC conversion is finished; the new ADC data will be stored in ADC Data Register. If IEADC ($00.3) is set, an interrupt request will transmit to cpu.
- Clear IRQADC for next ADC interrupt.

Note:

When ADCEN is set, the conversion is always doing, when one conversion is complete, IRQADC will be set. But the first three-conversion result is no use after ADCEN is set, because Σ-Δ ADC need setup time.

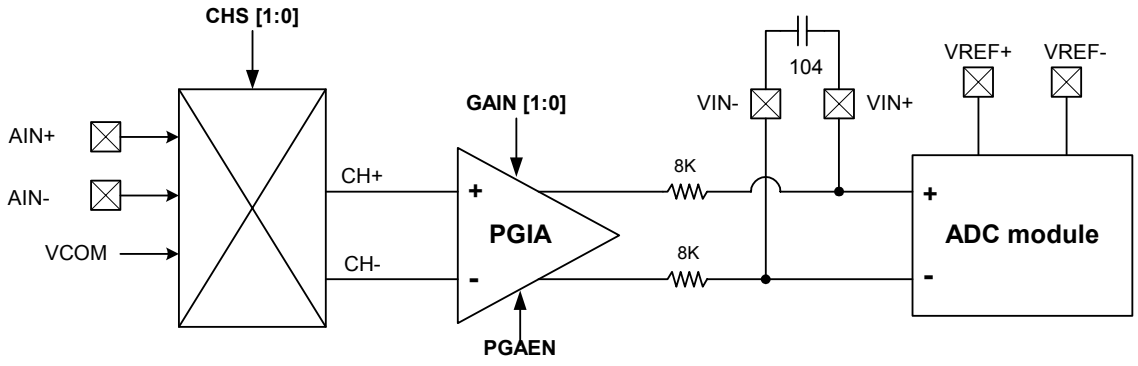
10.1. ADC Control Register: $20

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$20	ADCEN	-	REFS1	REFS0	R/W	Bit0-1: ADC reference selection bits Bit3: ADC Enable/Disable control bit
	0	-	X	X	R/W	ADC Disable
	1	-	X	X	R/W	ADC Enable
	X	-	1	X	R/W	Select ADC reference voltage from external reference VREF+, VREF-
	X	-	0	0	R/W	Internal reference voltage is 1.2V, 0.4V (VDDR2 = 3.0V)
	X	-	0	1	R/W	Internal reference voltage is 0.8V, 0.4V (VDDR2 = 3.0V)

Note:

Internal reference voltage if divided from VDDR2, so the internal reference voltage will follow the changing with VDDR2. If R2S is set to 1, VDDR2 output 1.5V. The VREF+ and VREF- will change to 0.6, 0.2V (if REFS0 = 0) or 0.4, 0.2V (if REFS0 = 1)

10.2. ADC Module Block Diagram



10.3. PGA (Programmable Gain Instrument Amplifier) Gain Register: $21

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$21	PGAEN	GAIN2	GAIN1	GAIN0	R/W	Bit2-0: PGA gain selection bits Bit3: PGA Enable/Disable control bit
	0	X	X	X	R/W	Disable PGA, signal is not amplified, Gain = 1
	1	0	0	0	R/W	Enable PGA, signal is amplified, Gain = 12.5
	1	0	0	1	R/W	Enable PGA, signal is amplified, Gain = 25
	1	0	1	0	R/W	Enable PGA, signal is amplified, Gain = 50
	1	0	1	1	R/W	Enable PGA, signal is amplified, Gain = 75
	1	1	0	0	R/W	Enable PGA, signal is amplified, Gain = 100
	1	1	0	1	R/W	Enable PGA, signal is amplified, Gain = 125
	1	1	1	0	R/W	Enable PGA, signal is amplified, Gain = 150
	1	1	1	1	R/W	Enable PGA, signal is amplified, Gain = 200

10.4. PGA Chopper Working Control: $22

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$22	-	CHOPEN	CHOPCLK1	CHOPCLK0	R/W	Bit0-1: PGA chopper work clock selection bits Bit2: PGA chopper Enable/Disable control bit
	-	0	X	X	R/W	Disable Chopper
	-	1	0	0	R/W	Enable Chopper, work clock = Fosc/128
	-	1	0	1	R/W	Enable Chopper, work clock = Fosc/64
	-	1	1	0	R/W	Enable Chopper, work clock = Fosc/32
	-	1	1	1	R/W	Enable Chopper, work clock = Fosc/16

Note:

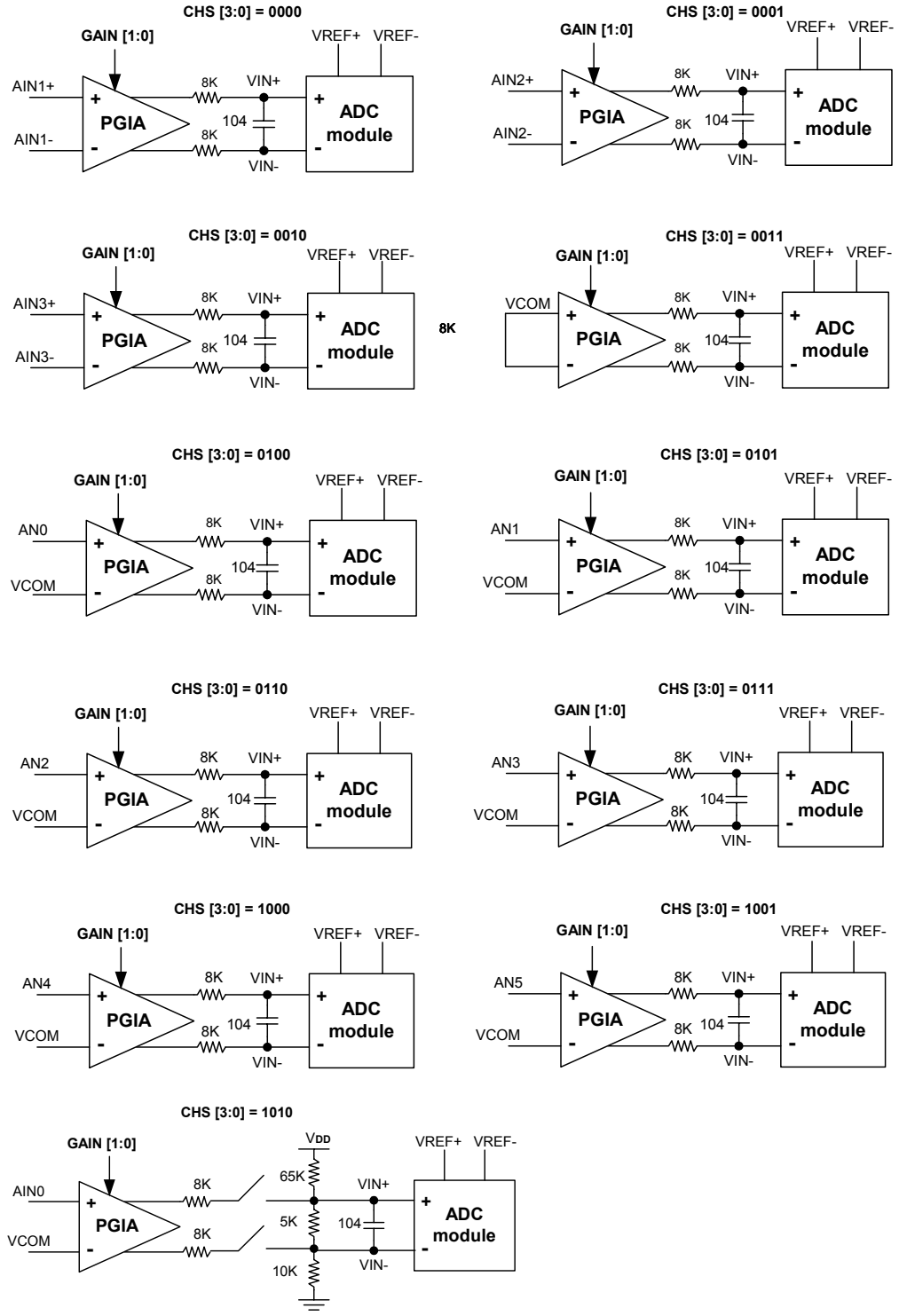
If chopper wants to be turn on, chopper work clock should be selected as 2KHz and register $22 should be written 0111B.

10.5. PGA and ADC channel select Register: $23

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$23	CHS3	CHS2	CHS1	CHS0	R/W	Bit3-0: PGA & ADC channel select
	0	0	0	0	R/W	Differential input, AIN1+, AIN1-
	0	0	0	1	R/W	Differential input, AIN2+, AIN2-
	0	0	1	0	R/W	Differential input, AIN3+, AIN3-
	0	0	1	1	R/W	AIN+, AIN- internal short (connect with VCOM)
	0	1	0	0	R/W	Single ended input0, AN0
	0	1	0	1	R/W	Single ended input1, AN1
	0	1	1	0	R/W	Single ended input2, AN2
	0	1	1	1	R/W	Single ended input3, AN3
	1	0	0	0	R/W	Single ended input4, AN4
	1	0	0	1	R/W	Single ended input5, AN5
	1	0	1	0	R/W	Power supply input measure. Vin+ = 3/16 V_{DD}, Vin- = 2/16V_{DD}
	1	0	1	1	R/W	Reserved
	1	1	x	x	R/W	Reserved

Note: When single ended input is selected, VCOM is auto connected to Negative input.

ADC Channel Selection Diagram:



Note:

If CHS[3:0] = 1010, it used to measure the power supply. An internal 80k resistor will connect V_{DD} to GND to provide sample point.

10.6. ADC Clock Register: $24 - $25

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$24	TADC3	TADC2	TADC1	TADC0	R/W	ADC clock select low nibble register
$25	TADC7	TADC6	TADC5	TADC4	R/W	ADC clock select high nibble register

TADC register sets the ADC working clock, 100kHz is recommended as ADC clock. When write these two register, Low nibble first, then write High nibble to update the counter initial value

The relation between ADC clock and TADC is:
ADC clock = 4194304/ 2 / (256-TADC [7:0]).
ADC conversion rate = ADC clock/4000

ADC clock is divided from PLL clock, so if ADC convert is needed, PLL must be enable, but sysck can be selected as 32kHz or PLL.

Note:
1. TADC7 - 0 Maxim value is FEH, Can't be set as FFH.
2. AC power 50Hz noise will be filtered out when ADC conversion rate is 25Hz.
3. AC power 60Hz noise will be filtered out when ADC conversion rate is 20Hz.
4. Both AC power 50Hz and 60Hz noise will be filtered out when ADC conversion rate is 10Hz.

10.7. ADC Port Share Register: $26

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$26	-	-	AN5S	AN4S	R/W	ADC port share register
	-	-	x	0	R/W	PORTA.3 as I/O ports
	-	-	x	1	R/W	PORTA.3 as AN4
	-	-	0	x	R/W	PORTA.2 as I/O ports
	-	-	1	x	R/W	PORTA.2 as AN5

10.8. ADC Data Register: $27 - $2A

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$27	D3	D2	D1	D0	R	ADC data register0
$28	D7	D6	D5	D4	R	ADC data register1
$29	D11	D10	D9	D8	R	ADC data register2
$2A	D15	D14	D13	D12	R	ADC data register3

ADC conversion result is stored in D15 - 0 with sign bit. D15 is the sign bit of ADC data. Refer to the following formula to calculate ADC conversion data value.

ADC data = ((VIN+) - (VIN-))/((VREF+) - (VREF-)) X 31250

When (VIN+) - (VIN-) is positive, D15 is 0 which means the ADC data is positive, the ADC value is D15 - 0.

When (VIN+) - (VIN-) is negative, D15 is 1 which means the ADC data is negative, the ADC value is 10000H minus D15 - 0.

ADC Data	7A12H	4000H	0001H	0000H	FFFFH	C000H	85EE
Decimal Value	31250	16384	1	0	-1	-16384	-31250

ADC Notes:
- To obtain maximum range of ADC output, the maximum absolute value of ADC input voltage VIN+ minus VIN- should be close to but can't over the reference voltage VREF+ minus VREF-.
- Clearing the ADCEN bit during a conversion will abort the current conversion.
- The ADC data register will not be updated with the partially completed ADC conversion.
- ADC could keep on working in HALT mode, and will stop automatically while executing "STOP" instruction.
- ADC could wake up the device from HALT mode if ADC interrupt is enabled.

11. LCD Driver

The LCD driver contains a controller, a voltage generator, 4 common driver pads and 32 segment driver pads. There is one driving programmable modes: 1/4 duty and 1/3 bias. The controller consists of display data RAM and a duty generator.

The LCD SEG29-32 can also be used as I/O port (PORTE), which is selected by bit 2-0 of the system register $07. LCD RAM can be used as data memory if needed.

When the “STOP” instruction is executed, the LCD will be turned off, but the data of LCD RAM keeps the value.

When LCD off, both common and segment output low.

11.1. LCD Control Register: $06

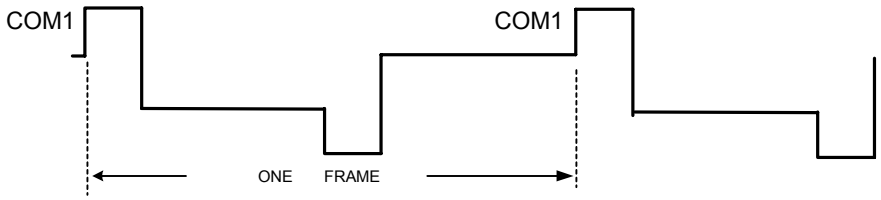
Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$06	FCT	FSTEN	RLCD0	-	R/W	LCD control register
	X	0	0	X	R/W	R1 = R2 = R3 = 150k (Default)
	X	0	1	X	R/W	R1 = R2 = R3 = 20k
	0	1	X	X	R/W	Fast charge mode, Fast charge time = 1/8 LCD Com duration
	1	1	X	X	R/W	Fast charge mode, Fast charge time = 1/32 LCD Com duration

11.2. LCD Port Control Register: $07

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$07	LCDON	O/S2	O/S1	O/S0	R/W	Bit2-0: LCD port control register Bit3: LCD on register
	X	X	X	0	R/W	PORTE.0 as I/O ports
	X	X	X	1	R/W	PORTE.0 as LCD SEG29
	X	X	0	X	R/W	PORTE.1 as I/O ports
	X	X	1	X	R/W	PORTE.1 as LCD SEG30
	X	0	X	X	R/W	PORTE.2-3 as I/O ports
	X	1	X	X	R/W	PORTE.2-3 as LCD SEG31-32
	0	X	X	X	R/W	Turn off LCD (Default)
	1	X	X	X	R/W	Turn on LCD

Note:

1. When large LCD panel is used, user can set the value of $06 to increase the bias current for better LCD performance, but it will cost more power, because smaller divider resistances are used.
2. When the CPU is in STOP mode, the COMx and SEGx are pulled low. It’s easy to be woken up by a keyboard scan (Port interrupt).

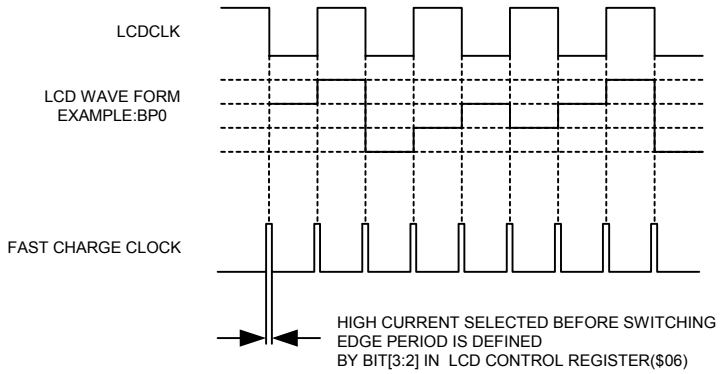


LCD Output Frame

11.3. Fast Charge Mode

The Default value of each bias resistor (RLCD) is 150k, the relatively high current drain through the 20k resistor will get better LCD display effect, but it may not be suitable for some low current consume application. Lowering this current is possible by setting the RLCD bit in the LCD control register, switching the RLCD value to 150k.Although the lower current drain is desirable, but in some LCD panel connections, LCD display may get worse because of weakly drain.

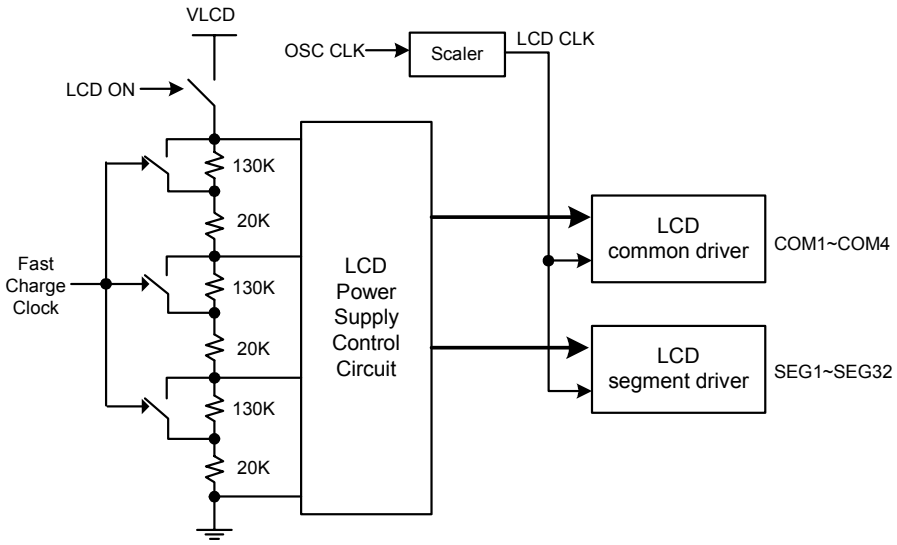
So there is a mode designed to get low power consuming and better display effect: Fast Charge Mode. It is designed to have the high current for the switching and low current for the steady state. Setting the FSTEN bit selects this mode. The RLCD value is set to 20k for a fraction of time for each LCD waveform switching edge, and the back to 150k for the steady state period. The duration of the fast charge time is set by configuring the FCT bit in the LCD clock register, and can be 1/8 LCD CLK, 1/32 LCD CLK.



11.4. Configuration of LCD RAM Area: (SEG 1-32, 1/4 duty)

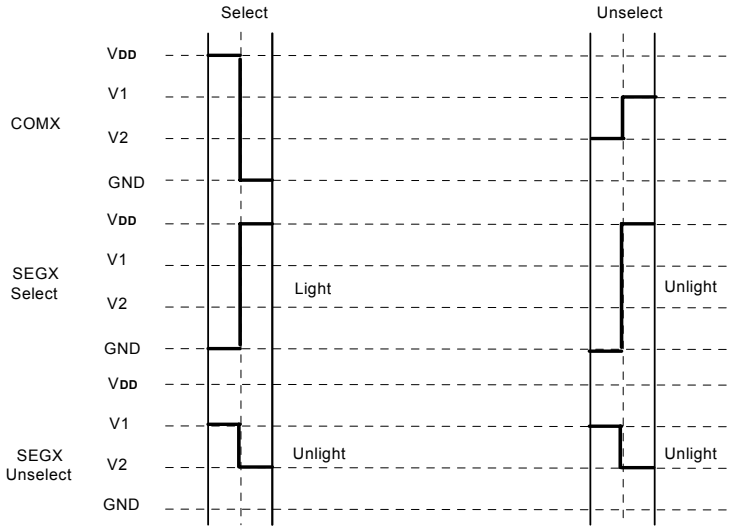
Address	Bit3	Bit2	Bit1	Bit0	Address	Bit3	Bit2	Bit1	Bit0
	COM4	COM3	COM2	COM1		COM4	COM3	COM2	COM1
300H	SEG1	SEG1	SEG1	SEG1	310H	SEG17	SEG17	SEG17	SEG17
301H	SEG2	SEG2	SEG2	SEG2	311H	SEG18	SEG18	SEG18	SEG18
302H	SEG3	SEG3	SEG3	SEG3	312H	SEG19	SEG19	SEG19	SEG19
303H	SEG4	SEG4	SEG4	SEG4	313H	SEG20	SEG20	SEG20	SEG20
304H	SEG5	SEG5	SEG5	SEG5	314H	SEG21	SEG21	SEG21	SEG21
305H	SEG6	SEG6	SEG6	SEG6	315H	SEG22	SEG22	SEG22	SEG22
306H	SEG7	SEG7	SEG7	SEG7	316H	SEG23	SEG23	SEG23	SEG23
307H	SEG8	SEG8	SEG8	SEG8	317H	SEG24	SEG24	SEG24	SEG24
308H	SEG9	SEG9	SEG9	SEG9	318H	SEG25	SEG25	SEG25	SEG25
309H	SEG10	SEG10	SEG10	SEG10	319H	SEG26	SEG26	SEG26	SEG26
30AH	SEG11	SEG11	SEG11	SEG11	31AH	SEG27	SEG27	SEG27	SEG27
30BH	SEG12	SEG12	SEG12	SEG12	31BH	SEG28	SEG28	SEG28	SEG28
30CH	SEG13	SEG13	SEG13	SEG13	31CH	SEG29	SEG29	SEG29	SEG29
30DH	SEG14	SEG14	SEG14	SEG14	31DH	SEG30	SEG30	SEG3	SEG30
30EH	SEG15	SEG15	SEG15	SEG15	31EH	SEG31	SEG31	SEG31	SEG31
30FH	SEG16	SEG16	SEG16	SEG16	31FH	SEG32	SEG32	SEG32	SEG32

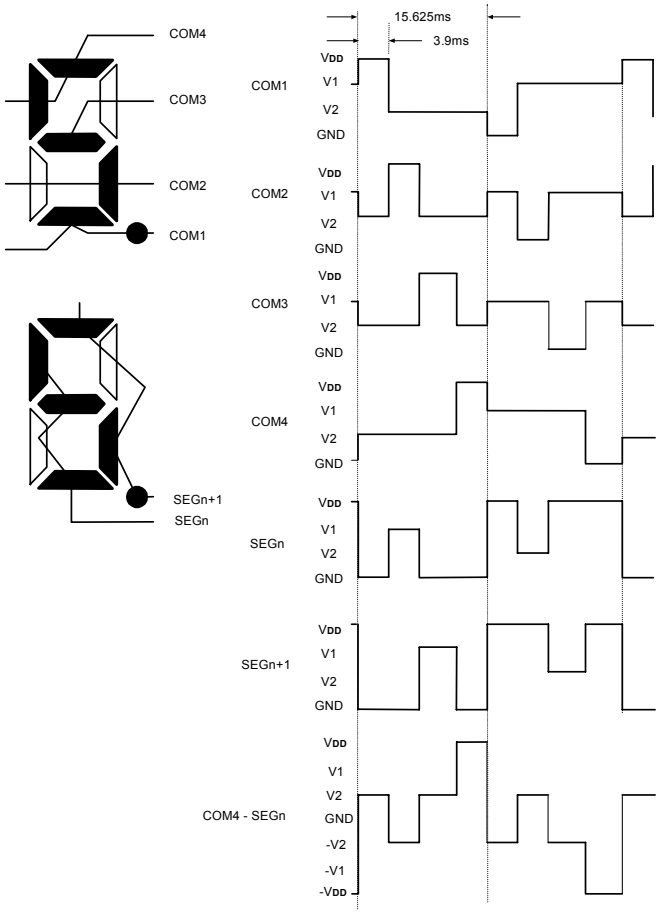
11.5. LCD Power supply



LCD Power if from VLCD pin, and LCD bias resistor connect to VLCD through LCDON switch.
You can connect VLCD to VDDR1 to get stable power supply for LCD display (REN1 must be set to enable VDDR1), the current consumption will be doubled if charge pump is enable. If V_{DD} > 3.6V, you can also disable pump.
You can also connect VLCD to V_{DD} directly (if V_{DD} is a stable power supply) to get very low current consumption.

11.6. 1/4 duty, 1/3 bias LCD Waveform





LCD waveform of 1/4 duty and 1/3 bias

12. Interrupt

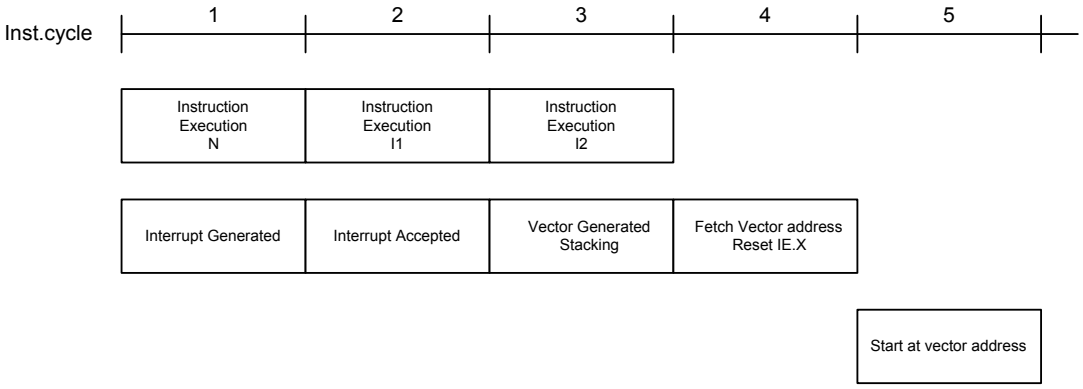
Four interrupt sources are available on SH66P58:
- A/D interrupt
- Timer0 interrupt
- Base Timer interrupt
- PORTB interrupts (Falling edge)

Interrupt Control Bits and Interrupt Service

The interrupt control flags are mapped on $00 and $01 of the system register. They can be accessed or tested by the program. Those flags are cleared to 0 at initialization by the chip reset.

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$00	IEADC	IET0	IEBT	IEP	R/W	Interrupt enable flags register
$01	IRQADC	IRQT0	IRQBT	IRQP	R/W	Interrupt request flags register

When IEx is set to 1 and the interrupt request is generated (IRQx is 1), the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources. When an interrupt occurs, the PC and CY flag will be saved into stack memory and jump to interrupt service vector address. After the interrupt occurs, all interrupt enable flags (IEx) are reset to 0 automatically, so when IRQx is 1 and IEx is set to 1 again, the interrupt will be activated and vector address will be generated from the priority PLA corresponding to the interrupt sources.



Interrupt Servicing Sequence Diagram

Interrupt Nesting

During the SH6610D CPU interrupt service, the user can enable any interrupt enable flag before returning from the interrupt. The servicing sequence diagram shows the next interrupt and the next nesting interrupt occurrences. If the interrupt request is ready and the instruction of execution N is IE enable, then the interrupt will start immediately after the next two instruction executions. However, if instruction I1 or instruction I2 disables the interrupt request or enable flag, then the interrupt service will be terminated.

ADC Interrupt

When ADCEN is set, an interrupt request (IRQADC) will be generate on every conversion is completed, if IEADC is set, an ADC interrupt service routine will start. ADC can be used to wake the CPU from HALT mode.

Timer0 Interrupt

The input clock of Timer0 is based on system clock or external clock/event T0 input. The timer overflow from $FF to $00 will generate an internal interrupt request (IRQT0 = 1). If the interrupt enable flag is enabled (IET0 = 1), a timer interrupt service routine will start. Timer0 interrupt can also be used to wake the CPU from HALT mode.

Base Timer Interrupt

The input clock of Base Timer is based on osc clock (32kHz). It overflow on every 2^{14} (2^{12}, 2^{10}, 2^{8}) osc clock and will generate an internal interrupt request (IRQBT = 1). If the interrupt enable flag is enabled (IEBT = 1), a timer interrupt service routine will start. Base Timer interrupt can also be used to wake the CPU from HALT mode.

Port Falling Edge Interrupt

The PORTB are used as external port interrupt sources. PortB can generate a port interrupt only it's in input state. The voltage transition from V_{DD} to GND applying to the input port can generate an interrupt request (IRQP = 1, PIF.X = 1). If the interrupt enable flag is enabled (IEP = 1, PIEN.X = 1), an interrupt service routine will start. Port Interrupts can be used to wake up the CPU from the HALT or the STOP mode.

Port Interrupt Enable Flags Register: $2E

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2E	PIEN.3	PIEN.2	PIEN.1	PIEN.0	R/W	PORTB interrupt enable control register

PIEN.x (x = 0, 1, 2, 3)
0: Disable PB.x port interrupt. (Default)
1: Enable PB.x port interrupt.

Port Interrupt Request Flags Register: $2F

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2F	PIF.3	PIF.2	PIF.1	PIF.0	R/W	PORTB interrupt request flags register

PIF.x (x = 0, 1, 2, 3)
0: PB.x port interrupt is not presented. (Default)
1: PB.x port interrupt is presented.

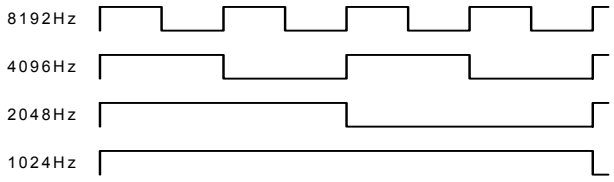
Note:
In input state, any pin of PortB can set PIF.x independently if a V_{DD} to GND transition occurs, regardless the other pin's level.

13. Alarm Output

Alarm carrier frequency setting register: $0D

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$0D	PULLEN	ALMF1	ALMF0	ALMEN	R/W	Bit0: ALM control register Bit2-1: ALM output carrier frequency Bit3: Port pull-high control
	x	X	X	0	R/W	Disable Alarm, PA.0 used as I/O
	x	0	0	1	R/W	Alarm carrier frequency is 1024Hz
	x	0	1	1	R/W	Alarm carrier frequency is 2048Hz
	x	1	0	1	R/W	Alarm carrier frequency is 4096Hz
	x	1	1	1	R/W	Alarm carrier frequency is 8192Hz
	0	x	x	x	R/W	Ports pull-high disable
	1	x	x	x	R/W	Ports pull-high enable

The programming alarm waveform is shown as follows:



Alarm output waveform

14. Pulse Width Modulation (PWM)

The SH66P58 consists of two 8 PWM modules. The PWM module can provide the pulse width modulation waveform with the period and the duty being controlled, individually. The PWMC is used to control the PWM module operation with proper clocks. The PWMP is used to control the period cycle of the PWM module output. And the PWMD is used to control the duty in the waveform of the PWM module output.

System Register $320, $321: PWM Control Register (PWMC)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$320, $321	PWMnS	TnCK1	TnCK0	PWMn_EN	R/W	Bit0: PWMn output enable Bit2, Bit1: Select PWMn clock Bit3: Set PWMn output mode of duty cycle
	X	X	X	0	R/W	Shared with I/O port (Default)
	X	X	X	1	R/W	Shared with PWMn, n = 0 or 1
	X	0	0	X	R/W	PWMn clock = t_{SYS} (Default)
	X	0	1	X	R/W	PWMn clock = $2t_{SYS}$
	X	1	0	X	R/W	PWMn clock = $4t_{SYS}$
	X	1	1	X	R/W	PWMn clock = $8t_{SYS}$
	0	X	X	X	R/W	PWMn output normal mode of duty cycle (high active) (Default)
	1	X	X	X	R/W	PWMn output negative mode of duty cycle (low active)

n = 0 or 1

The PWM0 output pin is shared with PORTD.0.

The PWM1 output pin is shared with PORTD.1.

System Register $322 - $323, $326 - $327: PWM Period Control Register (PWMP)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$322, $326	PPn.3	PPn.2	PPn.1	PPn.0	R/W	PWMn period low nibble
$323, $327	PPn.7	PPn.6	PPn.5	PPn.4	R/W	PWMn period high nibble

n = 0 or 1

PWM output period cycle = [PPn.7, PPn.0] X PWMn clock.

When [PPn.7, PPn.0] = 00H, PWMn will output GND if the PWMnS bit is set to “0”.

When [PPn.7, PPn.0] = 00H, PWMn will output high level if the PWMnS bit is set to “1”.

System Register $324 - $325, $328 - $329: PWM Duty Control Register (PWMD)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$324, $328	PDn.3	PDn.2	PDn.1	PDn.0	R/W	PWM0 duty low nibble
$325, $329	PDn.7	PDn.6	PDn.5	PDn.4	R/W	PWM0 duty high nibble

n = 0 or 1

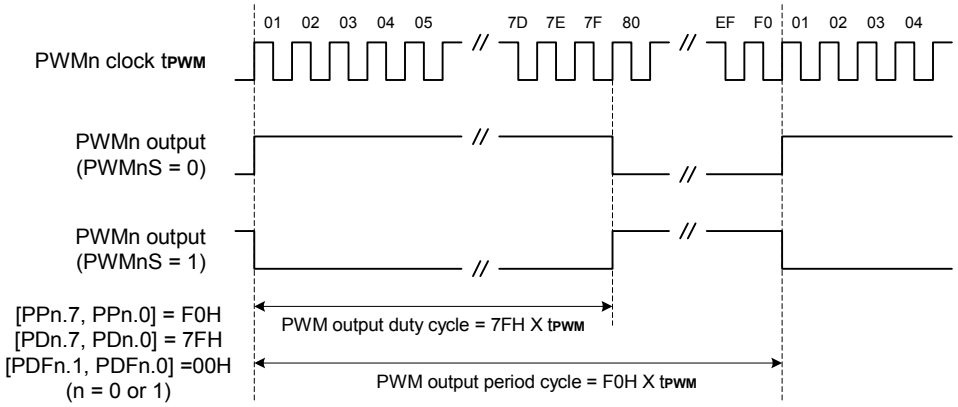
Average PWMn output duty cycle = ([PDn.7, PDn.0] + [PDFn.1, PDFn.0]/4) X PWMn clock.

If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs high when the PWMnS bit is set to “0”.

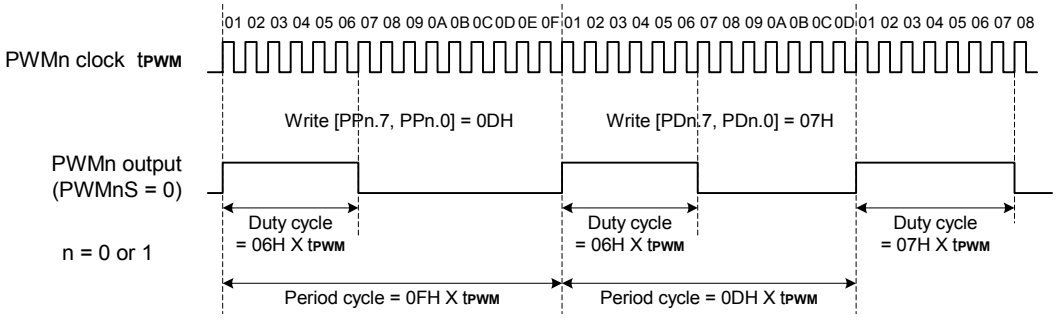
If [PPn.7, PPn.0] ≤ [PDn.7, PDn.0], PWMn outputs GND level when the PWMnS bit is set to “1”.

Note:

- Select the PWM module system clock.
- The writing flow of the PWMn duty control register is described as follows. First set the low nibble, and set the high nibble.
- The writing flow of the PWMn period control register is described as follows. First set the low nibble, and then set the high nibble.
- After the high nibble of the PWMn period or duty control register is written, the data are loaded into the re-load counter and start counting in the next period.
- The reading flow of the PWMn period or duty control register is at the reverse direction with that described above. First read the high nibble, and then read the low nibble.
- PWM can keep on working in the HALT mode, and will stop automatic when the "STOP" instruction is enabled.



PWM Output Example



PWM Output Period or Duty Cycle Changing Example

15. Low Voltage Reset (LVR)

The LVR function is to monitor the supply voltage and generate an internal reset in the device. It is typically used in AC line applications or large battery where large loads may be switched in and cause the device voltage to temporarily fall below the specified operating minimum.

The LVR function is selected by Code option.

The LVR circuit has the following functions when LVR function is enabled:

- Generates a system reset when $V_{DD} \leq V_{LVR}$.
- Cancels the system reset when $V_{DD} > V_{LVR}$.

LVR flag will always keep '1' when the LVR happens, LVR flag must be cleared to '0' by software.

16. Low Power Detect (LPD)

The LPD function monitors the supply voltage and generates the LPD flag.

LPD Control Register: $2B

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$2B	LPDEN	LPDF	LPDS1	LPDS0	R/W	Bit3: Low Power Detect Enable control bit Bit2: Low Power Detect Flag Bit1 - 0: Power voltage point select
	0	x	x	x	R/W	Disable Low Power Detect function
	1	x	0	0	R/W	Enable Low Power Detect, when V_{DD} < 2.4V, Flag is set
	1	x	0	1	R/W	Enable Low Power Detect, when V_{DD} < 3.0V, Flag is set
	1	x	1	0	R/W	Enable Low Power Detect, when V_{DD} < 3.3V, Flag is set
	1	x	1	1	R/W	Enable Low Power Detect, when V_{DD} < 3.6V, Flag is set
	x	0	x	x	R	No Flag
	x	1	x	x	R	Flag is set

17. ROM Data Table

System Register: $14 - $17

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$14	RDT.3	RDT.2	RDT.1	RDT.0	R/W	ROM Data table address/data register
$15	RDT.7	RDT.6	RDT.5	RDT.4	R/W	ROM Data table address/data register
$16	RDT.11	RDT.10	RDT.9	RDT.8	R/W	ROM Data table address/data register
$17	RDT.15	RDT.14	RDT.13	RDT.12	R/W	ROM Data table address/data register

The RDT register consists of a 13-bit write-only PC address load register (RDT.12 - RDT.0) and a 16-bit read-only ROM table data read-out register (RDT.15 - RDT.0).

To read out the ROM table data, users should fill 0 to higher 3 bits (Bit 13-15) first, then write the ROM table address to RDT register (high nibble first then low nibble), after one instruction, the right data will put into RDT register automatically (write lowest nibble of address into register will start the data read-out action).

18. Watch Dog Timer (WDT)

The watchdog timer is a down-count counter, and its clock source is an independent built-in RC oscillator, so that it will always run even in the STOP mode. The watchdog timer automatically generates a device reset when it overflows. It can be enabled or disabled permanently by using the code option.

The watchdog timer control bits ($1E Bit2 - Bit0) are used to select different overflow frequency. The watchdog timer overflow flag ($1E Bit3) will be automatically set to “1” by hardware when the watchdog timer overflows. By reading or writing the system register $1E, the watchdog timer should re-count before the overflow happens.

System Register $1E: Watchdog Timer (WDT)

Address	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Remarks
$1E	WDT	WDT.2	WDT.1	WDT.0	R/W R	Bit2-0: Watchdog timer control register Bit3: Watchdog timer overflow flag register
	X	0	0	0	R/W	Watchdog timer overflow period is 4096ms
	X	0	0	1	R/W	Watchdog timer overflow period is 1024ms
	X	0	1	0	R/W	Watchdog timer overflow period is 256ms
	X	0	1	1	R/W	Watchdog timer overflow period is 128ms
	X	1	0	0	R/W	Watchdog timer overflow period is 64ms
	X	1	0	1	R/W	Watchdog timer overflow period is 16ms
	X	1	1	0	R/W	Watchdog timer overflow period is 4ms
	X	1	1	1	R/W	Watchdog timer overflow period is 1ms
	0	X	X	X	R	No watchdog timer overflow resets
	1	X	X	X	R	Watchdog timer overflow, WDT reset happens

Note: Watchdog timer overflow period is valid for V_{DD} = 5V.

19. HALT and STOP Mode

After the execution of HALT instruction, SH66P58 will enter the HALT mode. In the HALT mode, CPU will stop operating. But peripheral circuit (Timer0, Base timer, ADC, PUMP, LPD, Regulator, PWM…) will keep status.

After the execution of STOP instruction, SH66P58 will enter the STOP mode. The most of chip (including oscillator) will stop operating and only ADC, PUMP, LPD and Regulator will keep status.

In the HALT mode, SH66P58 can be waked up if any interrupt occurs.

In the STOP mode, SH66P58 can be waked up if port interrupt occurs.

When CPU is awaked from the HALT/STOP by any interrupt source, it will execute the relevant interrupt serve subroutine at first. Then the instruction next to HALT/STOP is executed.

Note: For low power consumption, user must disable ADC, PUMP, LPD and Regulator before the HALT/STOP instruction.

20. Warm-up Timer

The device has a built-in warm-up timer to eliminate unstable state of initial oscillation when oscillator starts oscillating in the following conditions:
(1) Pin reset
(2) Power-on reset
(3) WDT reset
(4) LVR reset
(5) Wake up from stop mode
In Crystal oscillator, the warm-up counter prescaler divide ratio is $1/2^{14}$ (16384).

21. Code Option

(a) Watchdog Timer
OP_WDT:
0 = Disable (Default)
1 = Enable
(b) Low Voltage Reset
OP_LVR:
0 = Disable (Default)
1 = Enable

OTP Programming Pin Description (OTP Program Mode)

Pin No.	Symbol	I/O	Shared by	Description
	V_{DD}	P	V_{DD}	Programming Power supply (+5.5V)
	V_{PP}	P	$\overline{RESET}$	Programming high voltage Power supply (+11V)
	GND	P	GND	Ground
	SCK	I	OSCI	Programming Clock input pin
	SDA	I/O	PORTA.0	Programming Data pin

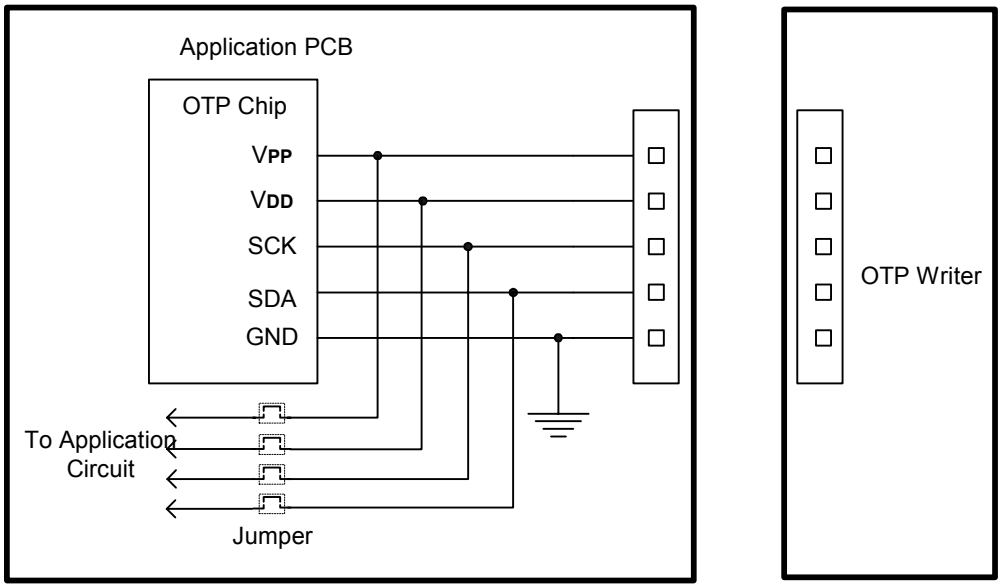
Which, I: Input; O: Output; P: Power; Z: High impedance

In System Programming Notice for OTP

The In System Programming technology is valid for OTP chip.

The Programming Interface of the OTP chip must be set on user's application PCB, and users can assemble all components including the OTP chip in the application PCB before programming the OTP chip. Of course, it's accessible bonding OTP chip only first, and then programming code and finally assembling other components.

Since the programming timing of Programming Interface is very sensitive, therefore four jumpers are needed (V_{DD}, V_{PP}, SDA, SCK) to separate the programming pins from the application circuit as shown in the following diagram.



The recommended steps are the followings:

(1) The jumpers are open to separate the programming pins from the application circuit before programming the chip.

(2) Connect the programming interface with OTP writer and begin programming.

(3) Disconnect OTP writer and shorten these jumpers when programming is completed.

For more detail information, please refer to the OTP writer user manual.

Instructions Set

All instructions are one cycle and one-word instructions. The characteristic is memory-oriented operation.

1. Arithmetic and Logical Instruction

1.1. Accumulator Type

Mnemonic	Instruction Code	Function	Flag Change
ADC X (, B)	00000 0bbb xxx xxxx	AC ← Mx + AC + CY	CY
ADCM X (, B)	00000 1bbb xxx xxxx	AC, Mx ← Mx + AC + CY	CY
ADD X (, B)	00001 0bbb xxx xxxx	AC ← Mx + AC	CY
ADDM X (, B)	00001 1bbb xxx xxxx	AC, Mx ← Mx + AC	CY
SBC X (, B)	00010 0bbb xxx xxxx	AC ← Mx + -AC + CY	CY
SBCM X (, B)	00010 1bbb xxx xxxx	AC, Mx ← Mx + -AC + CY	CY
SUB X (, B)	00011 0bbb xxx xxxx	AC ← Mx + -AC +1	CY
SUBM X (, B)	00011 1bbb xxx xxxx	AC, Mx ← Mx + -AC +1	CY
EOR X (, B)	00100 0bbb xxx xxxx	AC ← Mx ⊕ AC	
EORM X (, B)	00100 1bbb xxx xxxx	AC, Mx ← Mx ⊕ AC	
OR X (, B)	00101 0bbb xxx xxxx	AC ← Mx | AC	
ORM X (, B)	00101 1bbb xxx xxxx	AC, Mx ← Mx | AC	
AND X (, B)	00110 0bbb xxx xxxx	AC ← Mx & AC	
ANDM X (, B)	00110 1bbb xxx xxxx	AC, Mx ← Mx & AC	
SHR	11110 0000 000 0000	0 → AC[3], AC[0] → CY; AC shift right one bit	CY

1.2. Immediate Type

Mnemonic	Instruction Code	Function	Flag Change
ADI X,I	01000 iiii xxx xxxx	AC ← Mx + I	CY
ADIM X,I	01001 iiii xxx xxxx	AC, Mx ← Mx + I	CY
SBI X,I	01010 iiii xxx xxxx	AC ← Mx + -I + 1	CY
SBIM X,I	01011 iiii xxx xxxx	AC, Mx ← Mx + -I + 1	CY
EORIM X,I	01100 iiii xxx xxxx	AC, Mx ← Mx ⊕ I	
ORIM X,I	01101 iiii xxx xxxx	AC, Mx ← Mx | I	
ANDIM X,I	01110 iiii xxx xxxx	AC, Mx ← Mx & I	

1.3. Decimal Adjustment

Mnemonic	Instruction Code	Function	Flag Change
DAA X	11001 0110 xxx xxxx	AC, Mx ← Decimal adjust for add.	CY
DAS X	11001 1010 xxx xxxx	AC, Mx ← Decimal adjust for sub.	CY

2. Transfer Instruction

Mnemonic	Instruction Code	Function	Flag Change
LDA X (, B)	00111 0bbb xxx xxxx	AC ← Mx	
STA X (, B)	00111 1bbb xxx xxxx	Mx ← AC	
LDI X, I	01111 iiii xxx xxxx	AC, Mx ← I	

3. Control Instruction

Mnemonic	Instruction Code	Function	Flag Change
BAZ X	10010 xxxx xxx xxxx	PC ← X, if AC = 0	
BNZ X	10000 xxxx xxx xxxx	PC ← X, if AC ≠ 0	
BC X	10011 xxxx xxx xxxx	PC ← X, if CY = 1	
BNC X	10001 xxxx xxx xxxx	PC ← X, if CY ≠ 1	
BA0 X	10100 xxxx xxx xxxx	PC ← X, if AC (0) = 1	
BA1 X	10101 xxxx xxx xxxx	PC ← X, if AC (1) = 1	
BA2 X	10110 xxxx xxx xxxx	PC ← X, if AC (2) = 1	
BA3 X	10111 xxxx xxx xxxx	PC ← X, if AC (3) = 1	
CALL X	11000 xxxx xxx xxxx	ST ← CY, PC +1 PC ← X (Not include p)	
RTNW H, L	11010 000h hhh llll	PC ← ST; TBR ← hhhh, AC ← lll	
RTNI	11010 1000 000 0000	CY, PC ← ST	CY
HALT	11011 0000 000 0000		
STOP	11011 1000 000 0000		
JMP X	1110p xxxx xxx xxxx	PC ← X (Include p)	
TJMP	11110 1111 111 1111	PC ← (PC11-PC8) (TBR) (AC)	
NOP	11111 1111 111 1111	No Operation	

Where,

PC	Program counter	I	Immediate data
AC	Accumulator	⊕	Logical exclusive OR
-AC	Complement of accumulator	|	Logical OR
CY	Carry flag	&	Logical AND
Mx	Data memory	bbb	RAM bank
p	ROM page		
ST	Stack	TBR	Table Branch Register

Electrical Characteristics

Absolute Maximum Ratings*

DC Supply Voltage . . . . . -0.3V to +7.0V

Input Voltage . . . . . GND - 0.3V to V_{DD} + 0.3V

Operating Ambient Temperature . . . . . -40℃ to +85℃

Storage Temperature . . . . . -55℃ to +125℃

***Comments**

Stresses above those listed under "**Absolute Maximum Ratings**" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} =2.4 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.*	Max.	Unit	Condition
Operating Voltage	V_{DD}	2.4	3.0	5.5	V	32.768kHz ≤ f_{OSC} ≤ 4.192MHz
Low Voltage Reset voltage	V_{LVR}	2.3	2.4	2.5	V	LVR enable
Low Power Detect	V_{LPD}	3.5	3.6	3.7	V	LPD enable, and LPDS[1:0] = 11
Operating Current	I_{OP}	-	10	20	μA	f_{SYS} = 32.768kHz, All output pins unloaded, execute NOP instruction, WDT off, LVR off, LCD off, pump and regulator off, ADC disable. (V_{DD} = 3.0V)
		-	0.6	1.0	mA	f_{SYS} = 4.2MHz, All output pins unloaded, execute NOP instruction, WDT off, LCD off, pump and regulator off, ADC disable. (V_{DD} = 3.0V)
Stand by Current	I_{SB}	-	4	8	μA	f_{SYS} = 32.768kHz, All output pins unloaded (HALT mode), WDT off, LVR off, LCD off, ADC disable. Pump and regulator are all disable. (V_{DD} = 3.0V) (LCD on and RLCD0 = 0 will add 6 - 12uA; Base timer on will add 0.5 - 1uA)
		-	-	1.0	μA	All output pins unloaded (STOP mode), LCD off, ADC disable, pump and regulator are all disable. LVR off, WDT off, (V_{DD} = 3.0V)
WDT Current	I_{WDT}	-	-	10	μA	
LVR Current	I_{LVR}	-	2	3	μA	
LPD Current	I_{LPD}	-	-	20	μA	
Pump current	I_{PUMP}	-	5	10	μA	Pump output unloaded.
Regulator1 current	I_{R1}	-	20	30	μA	Regulator1 output unloaded, V_{DDR1} = 3.0V
Regulator2 current	I_{R2}	-	100	150	μA	Regulator2 output unloaded, V_{DDR2} = 3.0V
Input Low Voltage	V_{IL}	GND	-	V_{DD} X0.3	V	I/O ports, pins tri-state
		GND	-	V_{DD} X0.2	V	$\overline{RESET}$, T0 (Schmitt trigger input)
Input High Voltage	V_{IH}	V_{DD} X0.7	-	V_{DD}	V	I/O ports, pins tri-state
		V_{DD} X0.8	-	V_{DD}	V	$\overline{RESET}$, T0 (Schmitt trigger input)
Input Leakage Current	I_{IL}	-1	-	1	μA	I/O ports, GND < V_{IN} < V_{DD}
Pull-high Resistor	R_P	-	50	-	kΩ	Pull-high resistor (V_{DD} = 3.0V, V_{IN} = GND)
		-	30	-	kΩ	Pull-high resistor (V_{DD} = 5.0V, V_{IN} = GND)
Output Low Voltage	V_{OL1}			GND +0.6	V	I/O ports except PC.0, I_{OL} = 5mA. (V_{DD} = 3.0V)
						PC.0, I_{OL} = 10mA. (V_{DD} = 3.0V)

DC Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25°C, unless otherwise specified) (continued)

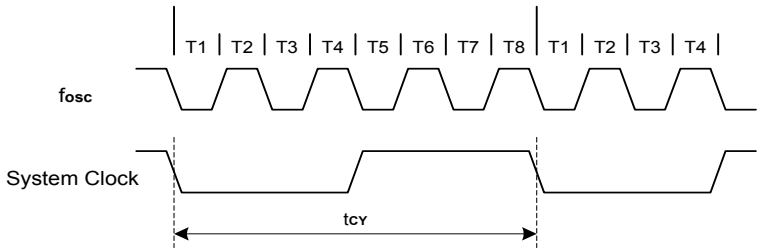
Parameter	Symbol	Min.	Typ. *	Max.	Unit	Condition
Output High Voltage	V_{OH1}	V_{DD} - 0.7	-	-	V	I/O ports, I_{OH} = - 3mA. (V_{DD} = 3.0V)
LCD Driving on resistor	R_{ON}	-	5	-	kΩ	LCD COMx, LCD SEGx, the voltage variation of V1, V2, V3 is less than 0.2V
LCD voltage divider resistor	R_{LCD}	-	150	-	kΩ	FSTEN = 0, RLCD0 = 0
		-	20	-	kΩ	FSTEN = 0, RLCD0 = 1
Regulator1 Output	V_{DDR1}	2.85	3.0	3.15	V	V_{DD} = 3.0V, Regulator1 unload
Regulator1 Output current capacity	I_{DRV1}	-	2	-	mA	V_{DD} = 3.0V, pump enable. △V_{DDR1} < 0.2V
Regulator2 Output	V_{DDR2}	2.85	3.0	3.15	V	V_{DD} = 3.0V, Regulator2 unload
Regulator2 Output current capacity	I_{DRV2}	-	10	-	mA	V_{DD} = 3.0V, pump enable. △V_{DDR2} < 0.2V
Regulator2 Output temperature coefficient	t_{VDDR2}	-	100	-	ppm/°C	T = 0 - 50°C
VCOM Output	V_{COM}	1.425	1.5	1.575	V	V_{DD} = 3.0V, ADC on
VCOM driving capacity	I_{SDR}	-	10	-	uA	V_{DD} = 3.0V, pump enable, ADC on. △V_{COM} < 0.1V
VCOM sinking capacity	I_{SNK}	-	1	-	mA	V_{DD} = 3.0V, pump enable, ADC on. △V_{COM} < 0.1V

AC Electrical Characteristics (V_{DD} = 2.4 - 5.5V, GND = 0V, T_A = 25℃, unless otherwise specified)

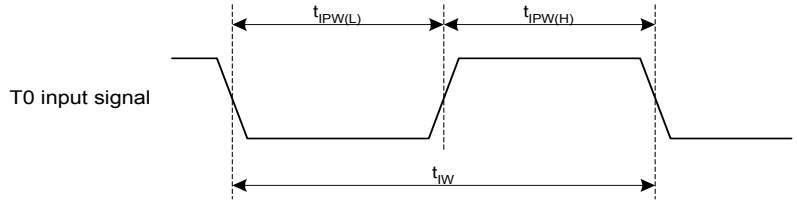
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Oscillator start time	t_{OSC}		1	2	s	Oscillator = 32.768KHz
RESET pulse width (low)	t_{RESET}	10	-	-	μs	V_{DD} = 3.0V
WDT Period	t_{WDT}	1	-	-	ms	V_{DD} = 3.0V
T0 input width	t_{IW}	(t_{CY} + 40)/N	-	-	ns	N = Prescaler divide ratio
Input pulse width	t_{IPW}	t_{IW}/2	-	-	ns	
Drop-Down Pulse Width for LVR	t_{LVR}	-	30	-	μs	
PLL Frequency variation	|ΔF|/F	-	-	0.5	%	Average frequency of continuous 256 clocks

Timing Waveform

(a) System Clock Timing Waveform:



(b) T0 Input Waveform:



ADC Electrical Characteristics

(V_{DD} = 2.4V - 5.5V, GND = 0V, PUMP ON, PGA Gain = 100, 200, T_A = 25°C, sysclk = 4.2MHz, unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Operation current	I_{ADC}	-	1	1.5	mA	
Resolution no missing code	NR	-	16	-	bit	$0.4 \le AIN \le V_{REF}$
Reference Voltage	V_{REF+}, V_{REF-}	0.4	-	1.2	V	Internal Reference
		0.4	-	2.0		External Reference
ADC Input Voltage	AIN+, AIN-	0.4	-	2.0	V	
Noise Free Code	NFC	-	14	16	bit	ADC Clock = 100 kHz
Differential non-linearity	DNL	-	±0.5	±0.5	LSB	ADC Clock = 100 kHz
Integral non-linearity	INL	-	±0.004	±0.008	% of FSR	$V_{REF±}$ = 0.60V, ADC Data = -25000 - 31250
Effective number of bits	ENOB	14	-	16	bit	
ADC Clock	F_{AD}	50	-	200	kHz	

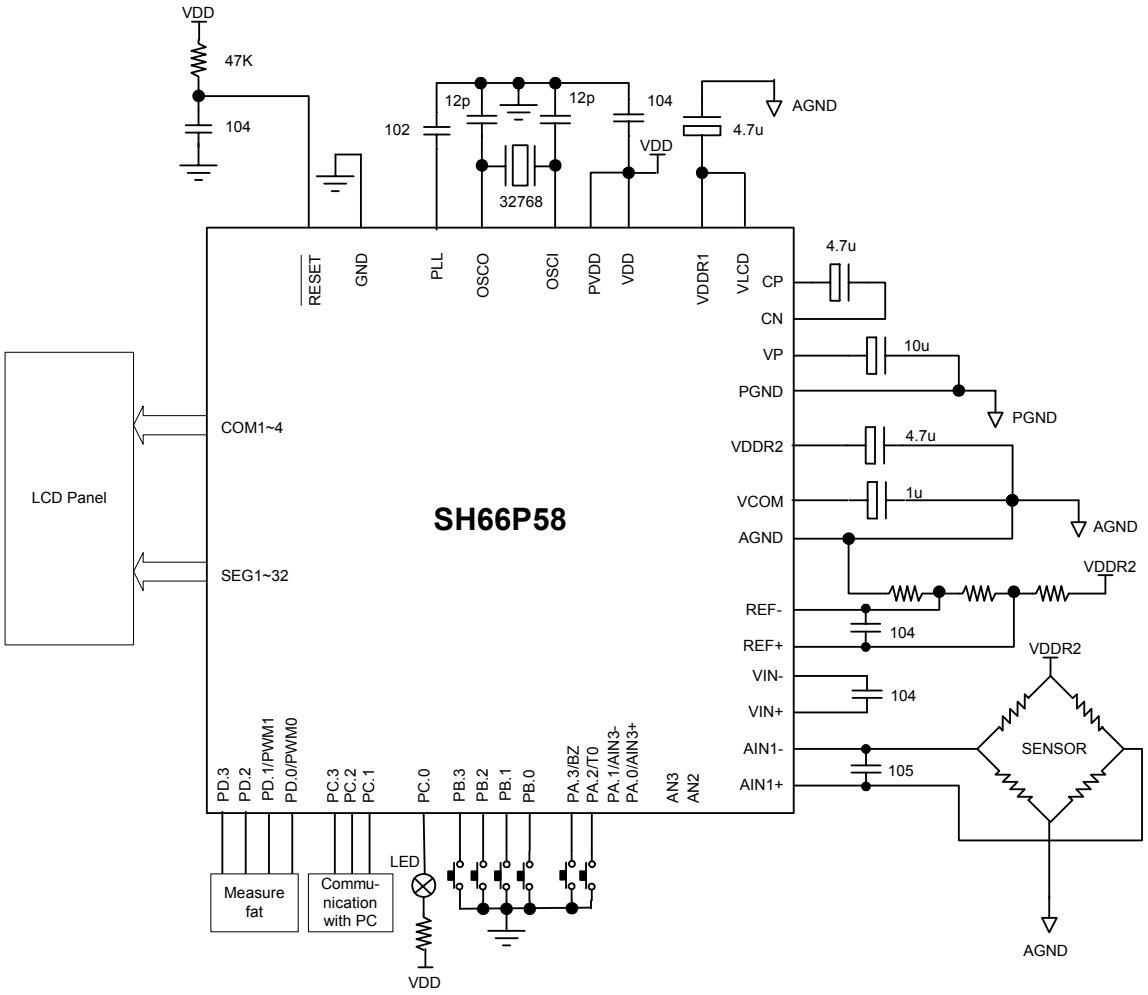
PGA Electrical Characteristics

(V_{DD} = 2.4V - 5.5V, GND = 0V, Pump Enable, PGA Gain = 100, 200, T_A = 25°C, sysclk = 4.2MHz, unless otherwise specified.)

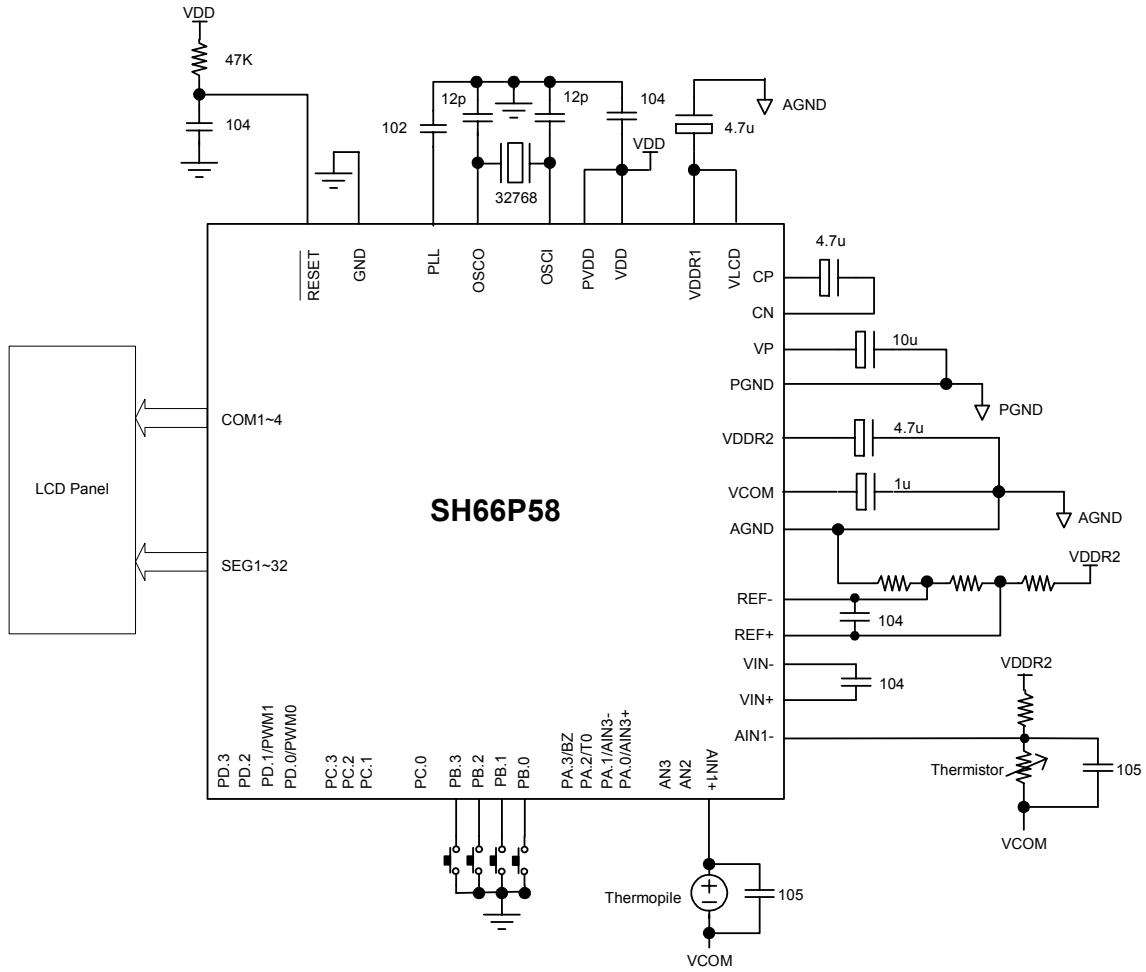
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Input offset	V_{ZER1}		20	50	uV	Chop Enable, Pump Disable
Input offset	V_{ZER2}		1	2	mV	Chop Disable, Pump Disable
PGA Input Range	V_{PGIN}	0.4	-	2.0	V	
PGA Output Range	V_{PGOUT}	0.4	-	2.0	V	
PGA Gain error	GAIN	0	-	4	%	GAIN = 200, chop disable

Application Circuit

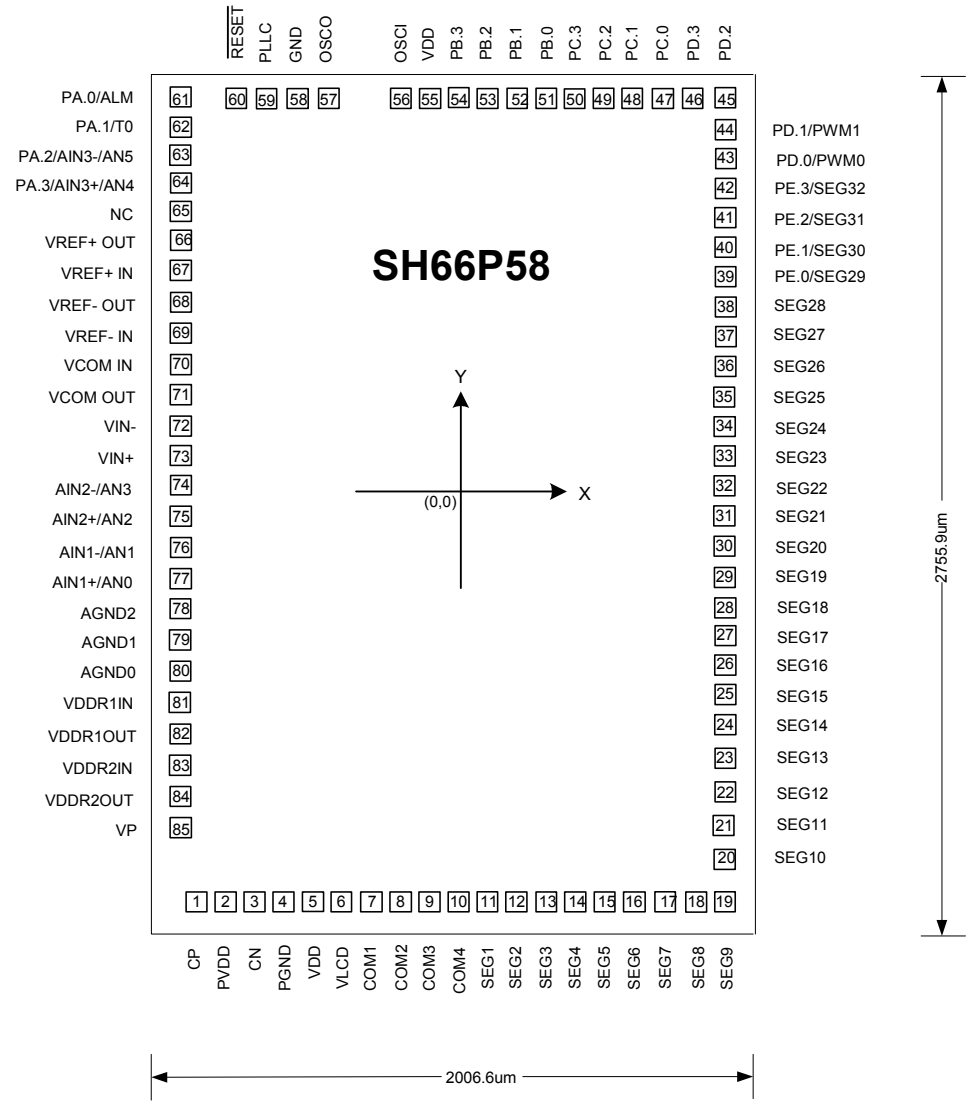
1. Scale Application Circuit



2. Thermometer Application Circuit



Bonding Diagram



Bonding Notice

1. Pad (VREF- OUT) and pad (VREF- IN) should be bonded at a pin.
2. Pad (VREF+ OUT) and pad (VREF+ IN) should be bonded at a pin.
3. Pad (VCOM OUT) and pad (VCOM IN) should be bonded at a pin.
4. Pad (AGND2), pad (AGND1) and pad (AGND0) should be bonded at a pin.
5. Pad (VDDR1 OUT) and pad (VDDR1 IN) should be bonded at a pin.
6. Pad (VDDR2 OUT) and pad (VDDR2 IN) should be bonded at a pin.

Pad Location Unit: μm

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	CP	-837.9	-1275.36	44	PD.1/PWM1	897.75	1159.34
2	PVDD	-726.75	-1274.76	45	PD.2	897.75	1274.76
3	CN	-624.15	-1274.76	46	PD.3	778.05	1274.76
4	PGND	-521.55	-1274.76	47	PC.0	675.45	1274.76
5	VDD	-427.5	-1274.76	48	PC.1	571.57	1274.76
6	VLCD	-333.45	-1274.76	49	PC.2	481.19	1274.76
7	COM1	-239.4	-1274.76	50	PC.3	390.82	1274.76
8	COM2	-149.03	-1274.76	51	PB.0	300.45	1274.76
9	COM3	-58.65	-1274.76	52	PB.1	210.07	1274.76
10	COM4	31.72	-1274.76	53	PB.2	119.7	1274.76
11	SEG1	122.09	-1274.76	54	PB.3	22.57	1274.76
12	SEG2	212.47	-1274.76	55	VDD	-67.8	1274.76
13	SEG3	302.84	-1274.76	56	OSCI	-158.17	1274.76
14	SEG4	393.21	-1274.76	57	OSCO	-389.54	1274.76
15	SEG5	483.59	-1274.76	58	GND	-484.53	1274.76
16	SEG6	573.96	-1274.76	59	PLLC	-579.52	1274.76
17	SEG7	675.45	-1274.76	60	$\overline{\text{RESET}}$	-684	1275.36
18	SEG8	778.05	-1274.76	61	PA.0/ALM	-897.75	1260.31
19	SEG9	897.75	-1274.76	62	PA.1/T0	-897.75	1146.6
20	SEG10	897.75	-1159.34	63	PA.2/AIN3-/AN5	-897.75	1044
21	SEG11	897.75	-1045.62	64	PA.3/AIN3+/AN4	-897.75	915.75
22	SEG12	897.75	-932.76	65	NC	-897.75	825.37
23	SEG13	897.75	-830.16	66	VREF+ OUT	-897.75	731.84
24	SEG14	897.75	-739.79	67	VREF+ IN	-897.75	641.46
25	SEG15	897.75	-649.41	68	VREF- OUT	-897.75	551.09
26	SEG16	897.75	-559.04	69	VREF- IN	-897.75	460.72
27	SEG17	897.75	-468.67	70	VCOM IN	-897.75	370.34
28	SEG18	897.75	-378.29	71	VCOM OUT	-897.75	279.97
29	SEG19	897.75	-287.92	72	VIN-	-897.75	189.6
30	SEG20	897.75	-197.55	73	VIN+	-897.75	99.22
31	SEG21	897.75	-107.17	74	AIN2-/AN3	-897.75	8.85
32	SEG22	897.75	-16.8	75	AIN2+/AN2	-897.75	-81.52
33	SEG23	897.75	73.57	76	AIN1-/AN1	-897.75	-171.9
34	SEG24	897.75	163.95	77	AIN1+/AN0	-897.75	-262.27
35	SEG25	897.75	254.32	78	AGND2	-897.75	-352.64
36	SEG26	897.75	344.69	79	AGND1	-897.75	-443.02
37	SEG27	897.75	435.07	80	AGND0	-897.75	-533.39
38	SEG28	897.75	525.44	81	VDDR1 IN	-897.75	-623.77
39	PE.0/SEG29	897.75	615.81	82	VDDR1 OUT	-897.75	-714.14
40	PE.1/SEG30	897.75	714.74	83	VDDR2 IN	-897.75	-804.51
41	PE.2/SEG31	897.75	821.61	84	VDDR2 OUT	-897.75	-907.11
42	PE.3/SEG32	897.75	928.49	85	VP	-898.35	-1018.26
43	PD.0/PWM0	897.75	1043.91				

Ordering Information

Part No.	Package
SH66P58H	Chip form

Data Sheet Revision History

Revision No.	Content	Date
V1.0	Original	Aug. 2009