

N - CHANNEL ENHANCEMENT MODE POWER MOS TRANSISTORS

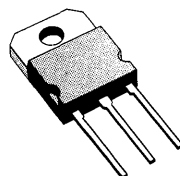
TYPE	V _{DSS}	R _{DS(on)}	I _D
SGSP481	60 V	0.06 Ω	30 A
SGSP482	50 V	0.06 Ω	30 A

- HIGH SPEED SWITCHING APPLICATIONS
- 60 VOLTS - DC/DC AND UPS APPLICATIONS
- ULTRA FAST SWITCHING
- EASY DRIVE FOR REDUCED COST AND SIZE

INDUSTRIAL APPLICATIONS:

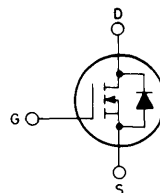
- DC/DC CONVERTERS AND UPS
- MOTOR CONTROLS

N - channel enhancement mode POWER MOS field effect transistors. Easy drive and very fast switching times make these POWER MOS transistors ideal for high speed switching applications. Typical uses include UPS, battery chargers, printer mechanism drives and motor speed control.



TO-218

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

		SGSP481	SGSP482	
V _{DS}	Drain-source voltage (V _{GS} = 0)	60	50	V
V _{DGR}	Drain-gate voltage (R _{GS} = 20 KΩ)	60	50	V
V _{GS}	Gate-source voltage		± 20	V
I _D	Drain current (cont.) at T _c = 25°C	30		A
I _D	Drain current (cont.) at T _c = 100°C	19		A
I _{DM} (*)	Drain current (pulsed)	120		A
I _{DLM} (*)	Drain inductive current, clamped	120		A
P _{tot}	Total dissipation at T _c < 25°C	125		W
	Derating factor	1		W/°C
T _{stg}	Storage temperature	- 65 to 150		°C
T _j	Max. operating junction temperature	150		°C

(*) Pulse width limited by safe operating area

THERMAL DATA

$R_{thj - case}$	Thermal resistance junction-case	max	1	°C/W
T_L	Maximum lead temperature for soldering purpose		275	°C

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

Parameters	Test Conditions	Min.	Typ.	Max.	Unit
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OFF

$V_{(BR) DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$ for SGSP481 for SGSP482	$V_{GS} = 0$	60 50		V V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$	$T_c = 125^{\circ}C$		250 1000	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

$V_{GS (th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$	$I_D = 250 \mu A$	2		4	V
$R_{DS (on)}$	Static drain-source on resistance	$V_{GS} = 10 V$ $V_{GS} = 10 V$	$I_D = 15 A$ $I_D = 15 A$			0.06 0.12	Ω Ω

DYNAMIC

g_{fs}	Forward transconductance	$V_{DS} = 25 V$	$I_D = 15 A$	5			mho
C_{iss}	Input capacitance	$V_{DS} = 25 V$	$f = 1 MHz$		1100	1400	pF
C_{oss}	Output capacitance	$V_{GS} = 0$				800	pF
C_{rss}	Reverse transfer capacitance					400	pF

SWITCHING

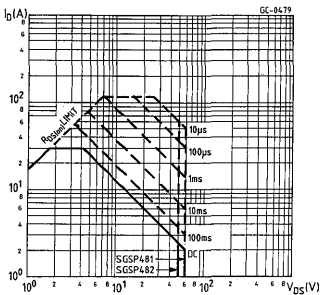
$t_d (on)$	Turn-on time	$V_{DD} = 25 V$	$I_D = 15 A$		25	35	ns
t_r	Rise time	$V_i = 10 V$	$R_i = 4.7 \Omega$		75	100	ns
$t_d (off)$	Turn-off delay time	(see test circuit)			50	65	ns
t_f	Fall time				40	55	ns

ELECTRICAL CHARACTERISTICS (Continued)

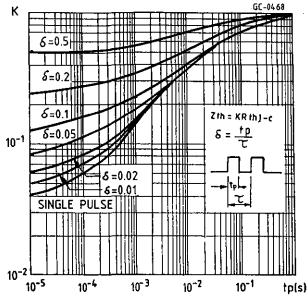
Parameters	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} Source-drain current I_{SDM} (*) Source-drain current (pulsed)				30 120	A A
V_{SD} Forward on voltage	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$			1.4	V
t_{rr} Reverse recovery time	$I_{SD} = 30\text{ A}$ $V_{GS} = 0$ $di/dt = 100\text{ A}/\mu\text{s}$		125		ns

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%
(*) Pulse width limited by safe operating area

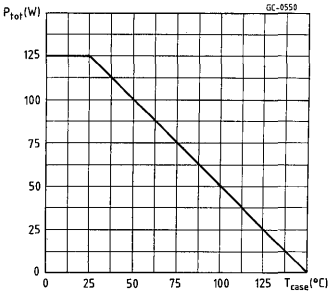
Safe operating areas



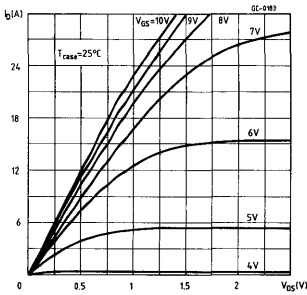
Thermal impedance



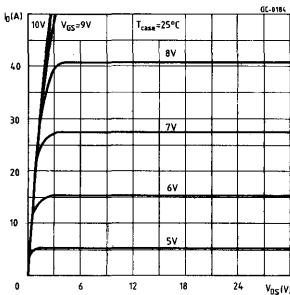
Derating curve



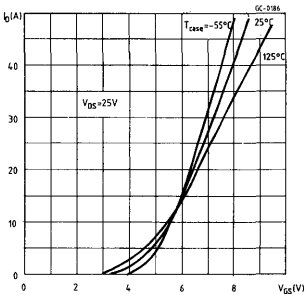
Output characteristics



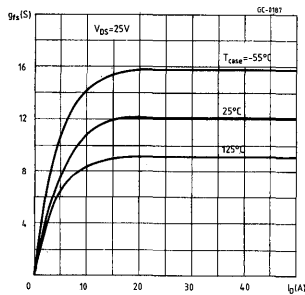
Output characteristics



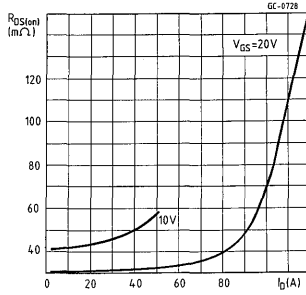
Transfer characteristics



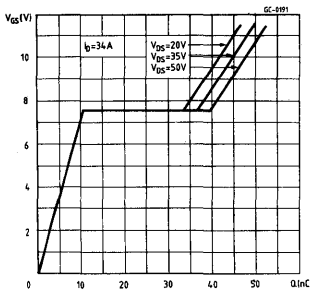
Transconductance



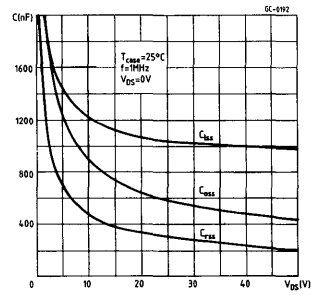
Static drain-source on resistance



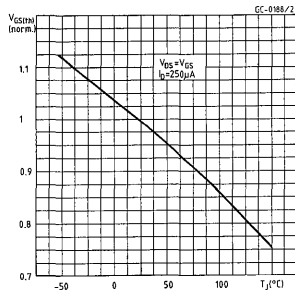
Gate charge vs gate-source voltage



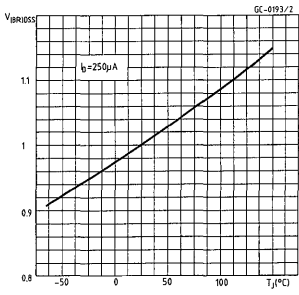
Capacitance variation



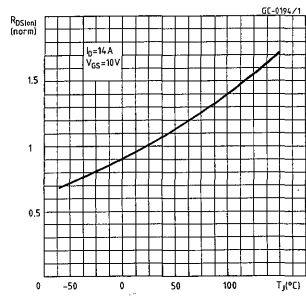
Normalized gate threshold voltage vs temperature



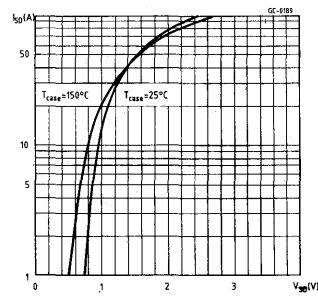
Normalized breakdown voltage vs temperature



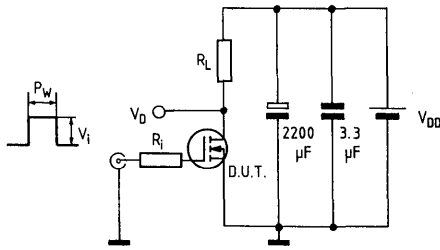
Normalized on resistance vs temperature



Source-drain diode forward characteristics



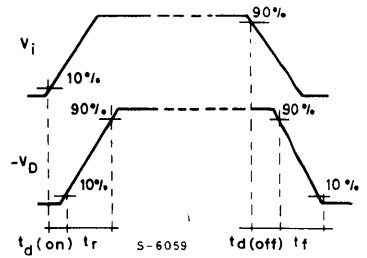
Switching times test circuit for resistive load



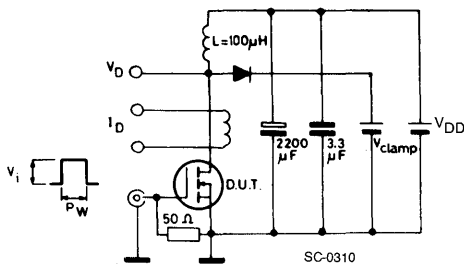
Pulse width $\leq 100 \mu\text{s}$

Duty cycle $\leq 2\%$

Switching time waveforms for resistive load

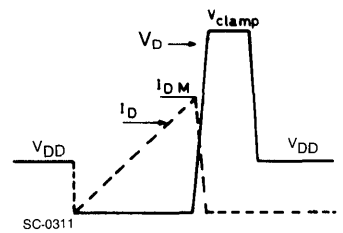


Clamped inductive load test circuit

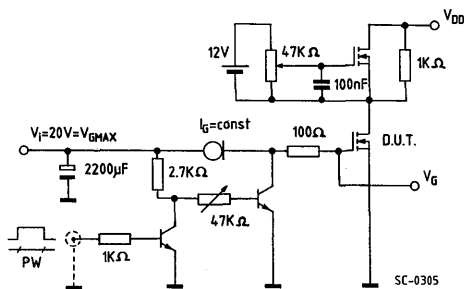


$V_i = 12 \text{ V}$ - Pulse width: adjusted to obtain specified I_{DM} , $V_{\text{clamp}} = 0.75 V_{(BR) \text{ DSS}}$.

Clamped inductive waveforms



Gate charge test circuit



PW adjusted to obtain required V_G

Body-drain diode t_{rr} measurement
Jedec test circuit

