SGM8904
Capless 2Vrms to 3Vrms Line Driver with Adjustable Gain

GENERAL DESCRIPTION

The SGM8904 is a 2Vrms to 3Vrms Pop&Click-less stereo line driver designed to allow the removal of the output dc-blocking capacitors for reduced component count and cost. The device is ideal for single supply electronics where size and cost are critical design parameters.

The SGM8904 is capable of driving 3Vrms into a 2.5kΩ load with 5V supply voltage. The device has single input and uses external gain setting resistors, that supports a gain range of ±1V/V to ±10V/V. The use of external gain resistors also allows the implementation of a 2nd order low pass filter to compliment DAC's and SOC converters. The SGM8904 has build-in shutdown control for Pop&Click-free on/off control.

Using the SGM8904 in audio products can reduce component count compared to traditional methods of generating a 3Vrms output. The SGM8904 doesn't require a power supply greater than 5V to generate its $8.5V_{PP}$ output, nor does it require a split rail power supply. The SGM8904 integrates its own charge pump to generate a negative supply rail that provides a clean, pop&click-less ground biased 3Vrms output.

The SGM8904 is available in Green MSOP10 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Capless Structure**
  - **Eliminates Pop/Clicks**
  - **Eliminates Output DC-Blocking Capacitors**
  - **Provides Flat Frequency Response DC to 20kHz**
- **Low Noise and THD**
  - **Typical SNR = 107dB**
  - **Typical V_N = 8μVrms**
  - **Typical THD+N = 0.001% (f = 1kHz)**
- **2Vrms Output Voltage into 2.5kΩ Load with 3.3V Supply Voltage**
- **3Vrms Output Voltage into 2.5kΩ Load with 5V Supply Voltage**

APPLICATIONS

Set-Top Box
LCD TV
Blue-Ray DVD-Players
Home Theater in a Box

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKAGE OPTION
SGM8904	MSOP10	SGM8904YMS10G/TR	SGM8904YMS10	Tape and Reel, 3000

ABSOLUTE MAXIMUM RATINGS

Supply Voltage.....-0.3V to 6V
Input Voltage.....V_{SS} - 0.3V to V_{DD} + 0.3V
Minimum Load Impedance (R_L) .....>600Ω
EN to GND.....-0.3V to V_{DD}+ 0.3V
Operating Temperature Range.....-40℃ to +85℃
Junction Temperature.....150℃
Storage Temperature..... -65℃ to +150℃
Lead Temperature (soldering, 10s).....260℃

ESD Susceptibility
HBM.....4000V
MM.....400V

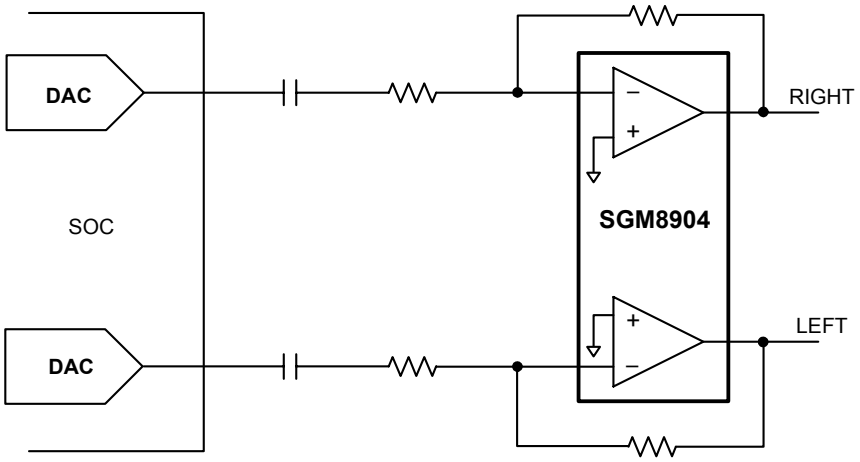
NOTE:
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

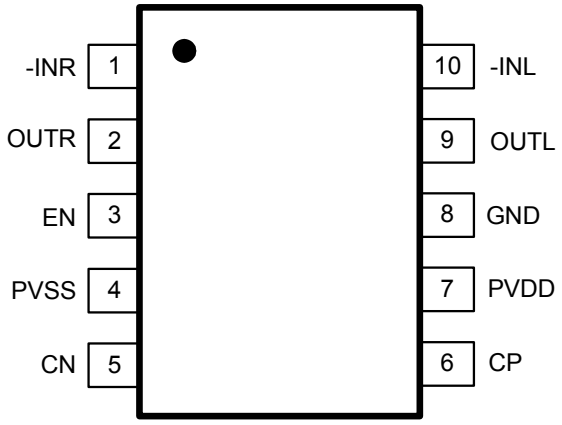
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SGMICRO reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact SGMICRO sales office to get the last datasheet.

TYPICAL OPERATION CIRCUIT



PIN CONFIGURATION (TOP VIEW)



MSOP10

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	-INR	Right channel OPAMP negative input
2	OUTR	Right channel OPAMP output
3	EN	Enable input, active high
4	PVSS	Negative supply voltage output
5	CN	Charge pump flying capacitor negative terminal
6	CP	Charge pump flying capacitor positive terminal
7	PVDD	Positive supply
8	GND	Ground
9	OUTL	Left channel OPAMP output
10	-INL	Left channel OPAMP negative input

ELECTRICAL CHARACTERISTICS

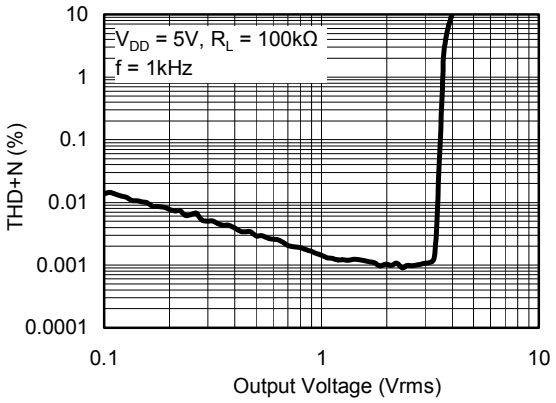
(T_A = 25℃, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS					
Output Offset Voltage ($\|V_{OS}\|$)	V_{DD} = 3V to 5V		1.2	5	mV
Supply Rejection Ratio (PSRR)	V_{DD} = 3V to 5V		90		dB
High-Level Output Voltage(V_{OH})	V_{DD} = 3.3V, R_L = 2.5kΩ	3.18			V
Low-Level Output Voltage (V_{OL})	V_{DD} = 3.3V, R_L = 2.5kΩ			-3.1	V
High-Level Input Current (EN) ($\|I_{IH}\|$)	V_{DD} = 5V, V_I = V_{DD}			1	μA
Low-Level Input Current (EN) ($\|I_{IL}\|$)	V_{DD} = 5V, V_I = 0V			1	μA
Supply Current (I_{DD})	V_{DD} = 3.3V, No load, EN = V_{DD}	8.5	11.3		mA
	V_{DD} = 5V, No load, EN = V_{DD}		12	15.5	
	Shutdown mode, V_{DD} = 3V to 5V		0.1	0.2	
OPERATING CHARACTERISTICS (V_{DD} = 3.3V, R_L = 2.5kΩ, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{fb} = 20kΩ)					
Output Voltage (Outputs In Phase) (V_O)	THD = 1%, V_{DD} = 3.3V, f = 1kHz	2.05			Vrms
	THD = 1%, V_{DD} = 5V, f = 1kHz	3.05			
	THD = 1%, V_{DD} = 5V, f = 1kHz, R_L = 100kΩ	3.1			
Total Harmonic Distortion Plus Noise (THD+N)	V_O = 2Vrms, f = 1kHz		0.001		%
	V_O = 2Vrms, f = 6.8kHz		0.004		
Crosstalk	V_O = 2Vrms, f = 1kHz		73		dB
Output Current Limit (I_O)	V_{DD} = 3.3V		20		mA
Input Resistor Range (R_{IN})		1	10	47	kΩ
Feedback Resistor Range (R_{FB})		4.7	20	100	kΩ
Slew Rate			8		V/μs
Maximum Capacitive Load			220		pF
Noise Output Voltage (V_N)	A-weighted, BW = 20kHz		8		μVrms
Signal to Noise Ratio (SNR)	V_O = 3Vrms, THD+N = 0.1%, BW = 20kHz A-weighted		107		dB
Unity Gain Bandwidth (G_{BW})			5.4		MHz
Open-Loop Voltage Gain (A_{VO})			120		dB
Charge Pump Frequency (F_{CP})		330	410	500	kHz
SHUTDOWN PIN					
Input High Voltage (V_{INH})		1.2			V
Input Low Voltage (V_{INL})				0.6	V
RECOMMENDED OPERATING CONDITIONS					
DC Supply Voltage (V_{DD})		3		5.5	V

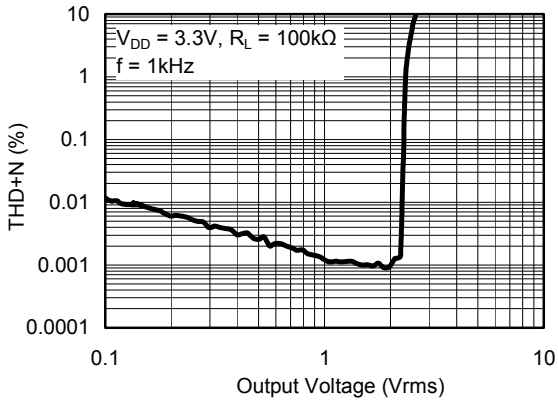
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, T_A = 25℃, R_L = 2.5kΩ, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ (unless otherwise noted).

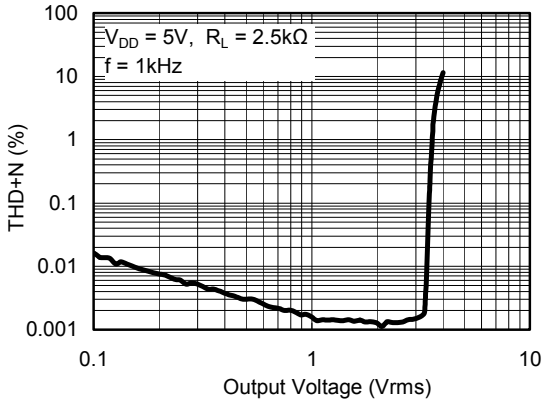
THD+N vs. Output Voltage



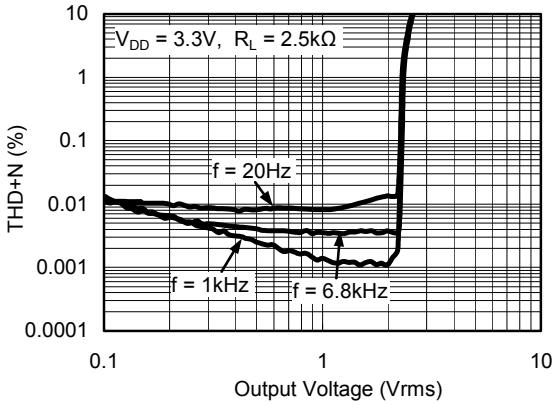
THD+N vs. Output Voltage



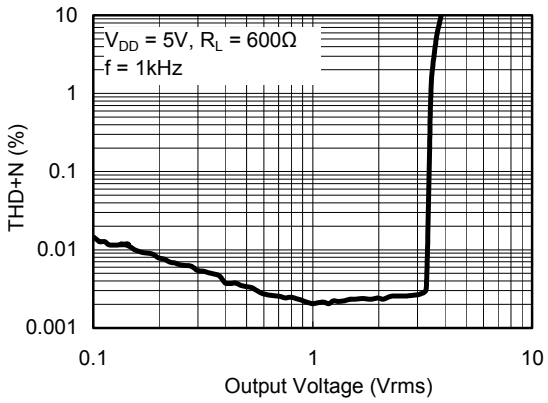
THD+N vs. Output Voltage



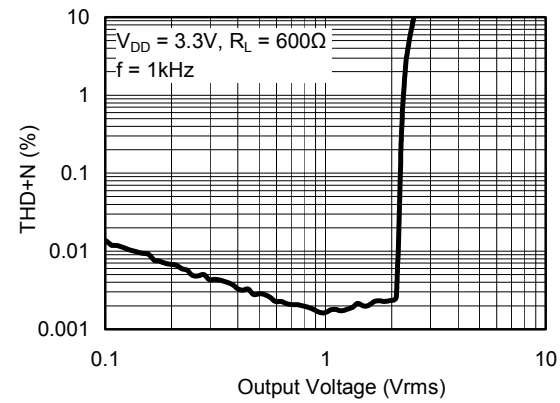
THD+N vs. Output Voltage



THD+N vs. Output Voltage



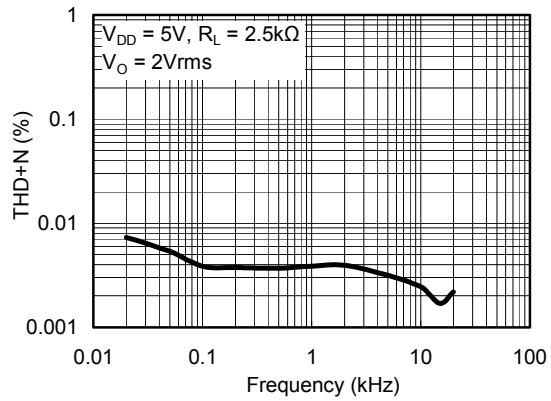
THD+N vs. Output Voltage



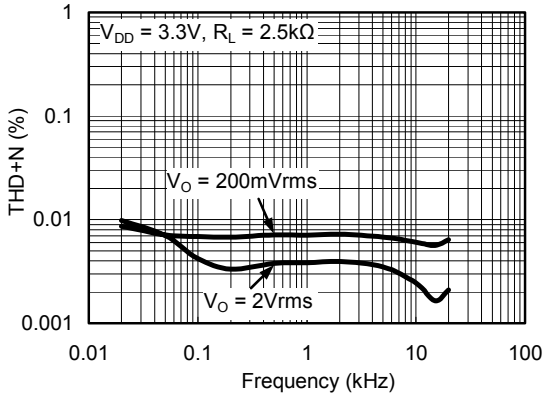
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 3.3V, T_A = 25℃, R_L = 2.5kΩ, $C_{(PUMP)}$ = $C_{(PVSS)}$ = 1μF, C_{IN} = 10μF, R_{IN} = 10kΩ, R_{FB} = 20kΩ (unless otherwise noted).

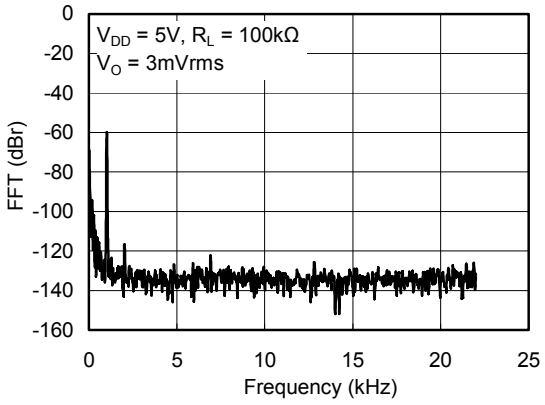
THD+N vs. Frequency



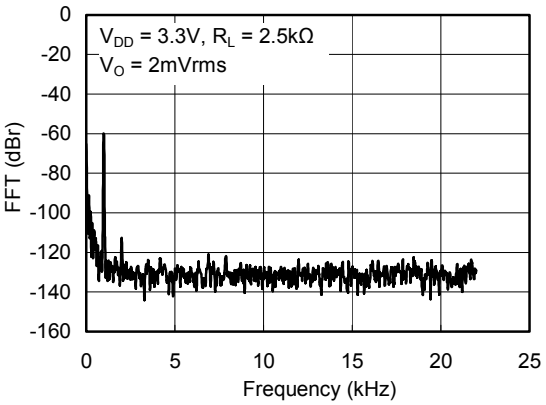
THD+N vs. Frequency



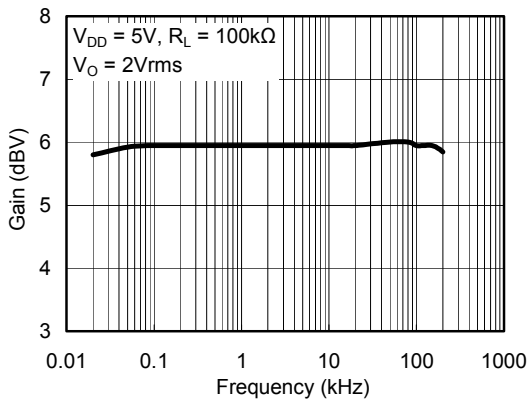
FFT vs. Frequency



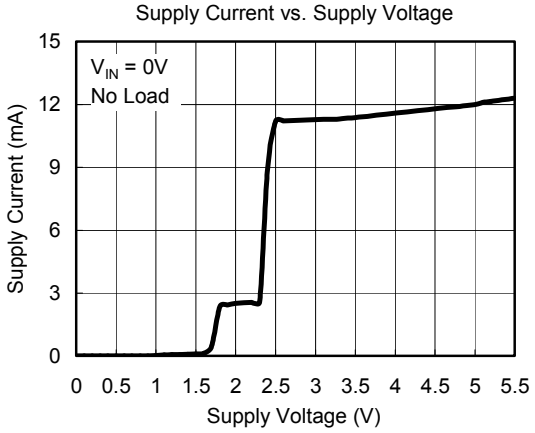
FFT vs. Frequency



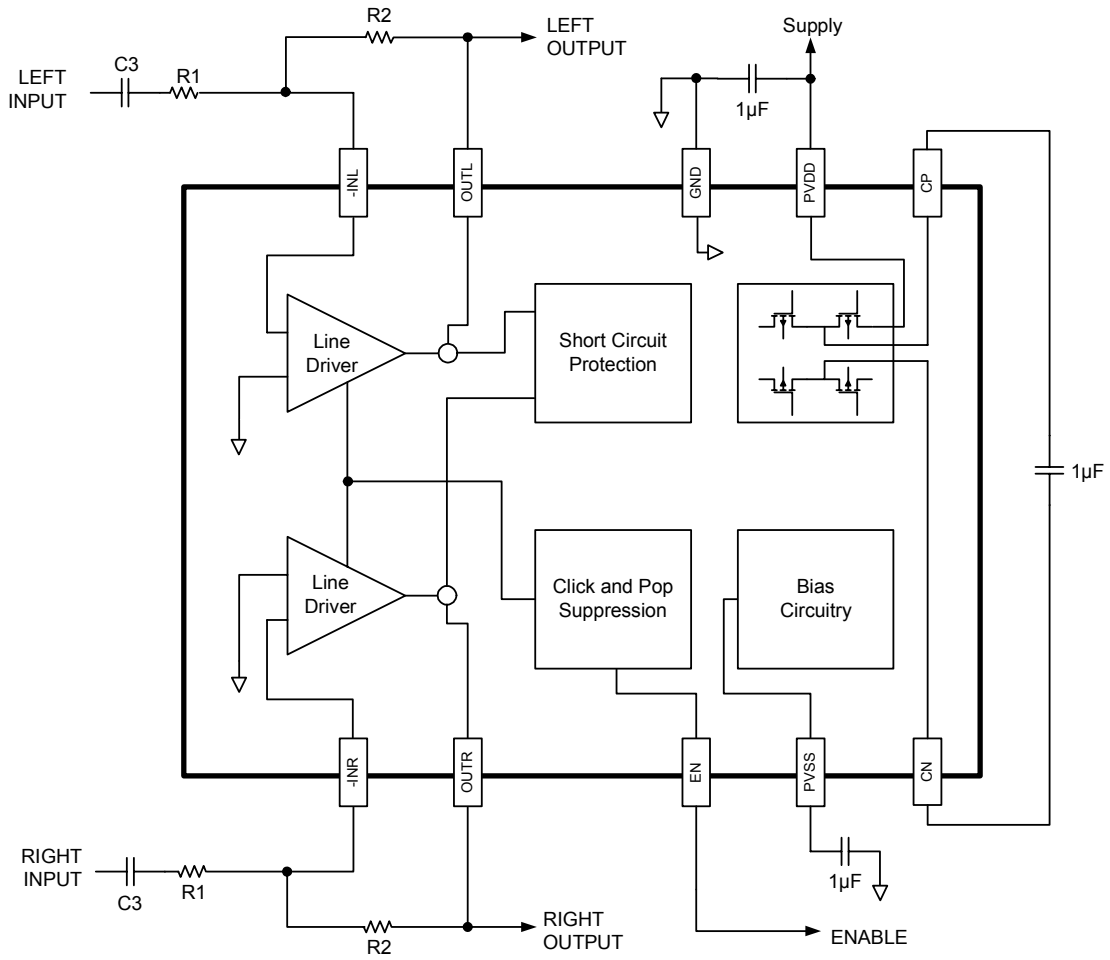
Gain vs. Frequency



Supply Current vs. Supply Voltage



APPLICATION CIRCUIT



APPLICATION INFORMATION

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1μF is typical. Capacitor values that are smaller than 1μF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The SGM8904 is a capless Line Driver amplifier that require adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the SGM8904 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM8904. These capacitors block the DC portion of the audio source and allow the SGM8904 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1, then the frequency and/or capacitance can be determined when one of the two values are given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \qquad (1)$$

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{SD}$ (EN) (shutdown pin) low during power supply ramp up and down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high, this way proper precharge of the ac-coupling is performed, and pop-less power-up is achieved. Figure 1 illustrates the preferred sequence.

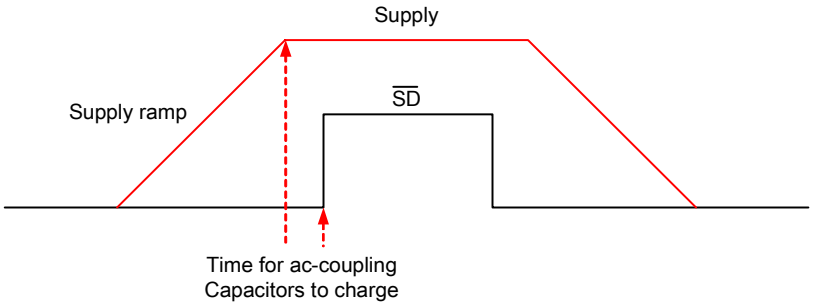


Figure 1. Power-Up Sequence

Capacitive Load

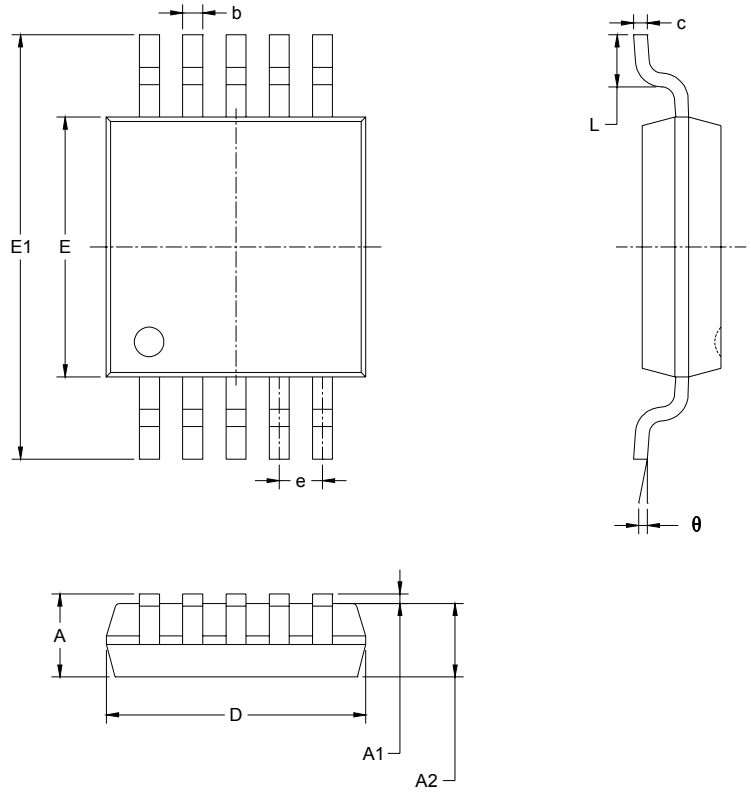
The SGM8904 has the ability to drive a high capacitive load up to 220pF directly, higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

Gain-Setting Resistors

The gain setting resistors, R_{IN} and R_{FB}, must be placed close to the input pins to minimize the capacitive loading on these input pins and to ensure maximum stability of the SGM8904.

PACKAGE OUTLINE DIMENSIONS

MSOP10



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°